Migration from S29PL127J to S29GL128S

About this document

Scope and purpose

AN240400 describes the differences and potential issues when migrating from Infineon S29PL127J Floating Gate to the S29GL128S MIRRORBIT™ NOR flash devices. It discusses affected device features, timing parameters, as well as packages.

Intended audience

This application note is intended for users and system designers planning to migrate from the Floating Gate S29PL127J to the MIRRORBIT™ S29GL128S as a replacement.

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1 Introduction

Infineon S29PL127J is 3.0 V-only Page Mode and Simultaneous Read/Write Flash memory device manufactured on the Floating Gate (FG) 110 nm process technology whereas Infineon S29GL128S (128 Mbit) is 3.0 volt-only Page Mode flash memory manufactured with 65 nm MIRRORBIT™ Eclipse technology.

This document outlines the product differences that require attention when migrating from S29PL127J to S29GL128S flash.

Feature comparisons are shown is Section 2. Feature differences are mentioned in Section 3. Differences in power-on-reset (POR) timing are discussed in Section 4. Differences in DC and AC specifications are detailed in Section 5. Differences in footprint and packaging are discussed in Section 6.

2 Feature comparison

The 65 nm MIRRORBIT™ S29GL128S flash provides significantly improved program and erase performance for 3 V parallel NOR applications, while maintaining basic hardware pin out connection and software compatibility to allow use in existing designs that use S29PL127J. Table 1 compares these features between S29PL127J and S29GL128S.

Table 1 S29PL127J and S29GL128S feature comparison

	S29PL127J	S29GL128S
Process node	110 nm (FG)	65 nm MIRRORBIT™
Access time	60 ns, 65 ns, 70 ns, 80 ns	90 ns, 100 ns
Simultaneous read/write operation	✓	N/A
Wireless (–25°C to +85°C)	✓	N/A
Industrial (–40 to +85°C)	✓	✓
Industrial Plus (–40 to +105°C)	N/A	✓
Automotive, AEC-Q100 Grade 3 (–40 to +85°C)	✓	✓
Automotive, AEC-Q100 Grade 2 (–40 to +105°C)	N/A	✓
100,000 erase cycles typical per sector minimum	N/A	✓
1,000,000 erase cycles typical per sector	✓	N/A
Uniform sectors (128 KB)	N/A	✓
Flex Bank (4-bank) architecture	✓	N/A
Twenty-year data retention typical	✓	✓
Data bus width	x16 only	x16 only
Asynchronous	✓	✓
Read page mode	✓	✓
Read page size	8 words	16 words
Maximum write buffer size [1]	N/A	512 bytes
Secured Silicon Region	256 bytes	512 bytes
Status via status register	N/A	✓
Automatic ECC	N/A	✓
Versatile I/O	✓	✓
WP# (Write Protect)	✓	✓
56-pin TSOP (TS056)	✓	✓
80-ball fine-pitch BGA (VBG080, 11 mm x 8 mm)	✓	N/A
56-ball fine-pitch BGA (VBU056, 7 mm x 9 mm)	N/A	✓
64-Ball fortified ball grid array (LAA064, 13 mm x 11 mm)	N/A	✓
64-Ball fortified ball grid array (LAE064, 9 mm x 9 mm)	N/A	✓

[1] GL128S allows 2-byte, 32-byte, 64-byte, 128-byte, and 256-byte write buffer size; no software changes required. Use the full 512-byte write buffer for better write performance; slight S/W change is required.

3 Feature differences

3.1 Write buffer

The write buffer is designed to reduce the overall system programming time when programming the device. The host system issues a Write to Buffer command, fills the write buffer with data, and then issues the programming command.

Depending on the device design, a write buffer can store up to 512 bytes. The write buffer also allows 2-byte, 32-byte, 64-byte, 128-byte, and 256-byte write buffer sizes. The write buffer allows a maximum of 256 words/512 bytes to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. S29PL127J does not support the write buffer feature.

3.2 Status register

The S29GL128S status register contains the status and control bits that can be read or set by specific commands, and supports status register reads as an alternative method (to data polling) to determine the embedded operation status. The status register feature is not supported on S29PL127J flash memory devices.

The 16-bit status register is accessed via a two-cycle operation consisting of: (1). Read Status Register command (adrs : 555h / Data 70h); followed immediately by: (2). Read Cycle command (adrs : don't care / data : RD) of the targeted sector address. Utilization of the status register is advantageous because unlike legacy data polling, the software does not need to track active address regions or compare sequential polling read values to determine the embedded algorithm status. See the S29GL128S datasheet [2] for command summary and definitions.

One status register access provides all the information necessary to determine the flash state. A Clear Status Register command is available to reset the last completed embedded operation portion of the status register. The use of the status register is optional. S29PL127J has DQ7 data polling or DQ6 toggle method to monitor device status, but does not support the status register feature.

For more details on status register implementation and bit definition, see the S29GL128S datasheet [2].

3.3 Versatile I/O

The maximum output voltage level driven by and input levels acceptable to the device are determined by the VIO power supply. This supply allows the device to drive and receive signals to and from other devices on the same bus having interface signal levels different from the device core voltage. S29GL128S and S29PL127J both support Versatile I/O feature.

See the S29GL128S datasheet [2] for details of implementation of the Versatile I/O feature.

3.4 WP# (Write Protect)

The Write Protect feature provides a hardware method of protecting the higher two and lower two sectors.

If WP# = V_{IL}, the lowest or highest address sector is protected from program or erase operations independent of any other Advanced Sector Protection configuration. Whether it is the lowest or highest sector depends on the device ordering option (model) selected. If WP# = V_{IH}, the lowest or highest address sector is not protected by the WP# signal but it may be protected by other aspects of Advanced Sector Protection configuration. WP# has an internal pull-up; when unconnected, WP# is at V_{IH}. S29GL128S and S29PL127S both support WP#.

See the S29GL128S [2] and S29PL127J [1] datasheets for details.

3.5 Automatic ECC

The S29GL128S flash supports the automatic ECC feature that has internal hardware ECC with single-bit error correction. This feature can help improve user data integrity stored in flash. This feature is executed by flash internally; no change needs to be done when migrating from S29PL127J flash. This feature is transparent to the user. See the S29GL128S datasheet [2] for details of the automatic ECC feature.

3.6 Manufacturer ID and Device ID

Table 2 Manufacturer and Device ID

	S29PL127J	S29GL128S
Manuf. ID	01h	01h
Cycle-1	227Eh	227Eh
Cycle-2	2220h	2221h
Cycle-3	2200h	2201h

3.7 CFI register

Table 3 provides a listing of all the Common Flash Memory Interface (CFI) register values that are different for S29GL128S as compared to S29PL127J flash families. Software can access the CFI register to determine device-specific features such as array size, command set, page size, and programming time; and use these values to self-configure for optimal performance.

Table 3 CFI register differences

CFI register	S29PL127J	Data	S29GL128S	Data
Typical timeout per single write 2^N µs	1Fh	0003h	1Fh	0008h
Typical timeout for min. size buffer write 2^N µs (00h = not supported)	20h	0000h	N/A	N/A
Typical timeout for full-chip erase 2^N ms (00h = not supported)	22h	0000h	22h	000Fh
Max. timeout for byte/word program 2^N times typical	23h	0004h	N/A	N/A
Max. timeout for buffer write 2^N times typical	24h	0000h	24h	0002h
Max. timeout per individual block erase 2^N times typical	25h	0004h	25h	0003h
Flash device interface description (refer to CFI publication 100)	28h	0001h	N/A	N/A
Max. number of byte in multi-byte write = 2^n (00h = not supported)	2Ah	0000h	2Ah	0009h
Number of erase block regions within device 01h = uniform device; 02h = boot device	2Ch	0003h	2Ch	0001h
Erase block region 1 information (refer to the CFI specification or CFI publication 100)	2Dh 2Fh	0007h 0020h	2Dh 30h	007Fh 0002h
Erase block region 2 information	31h	00FDh	31h	0000h

Feature differences

CFI register	S29PL127J	Data	S29GL128S	Data
Erase block region 3 information (refer to CFI publication 100)	35h	0007h	35h	0000h
Sector temporary unprotect 00 = Not Supported, 01 = Supported	48h	0001h	48h	0000h
Sector protect/unprotect scheme Advanced Sector Protection	49h	0007h	49h	0008h
Simultaneous operation 00 = Not supported X = Number of sectors in bank	4Ah	00E7h	4Ah	0000h
ACC (Acceleration) supply minimum 00h = Not supported, D7-D4: Volt, D3-D0: 100 mV	4Dh	0085h	4Dh	0000h
ACC (Acceleration) supply maximum 00h = Not supported, D7-D4: Volt, D3-D0: 100 mV	4Eh	0095h	4Eh	0000h
Top/bottom boot sector flag 00h = Uniform device 01h = Both top and bottom boot with Write Protect 02h = Bottom boot device 03h = Top boot device 04h = Unif. Bottom address sector - WP Protect 05h = Unif. Top address sector - WP Protect	4Fh	0001h	4Fh	0004h or 0005h

4 Power-on reset (POR) and warm reset timing

At power on, the flash requires more time in the reset state to self-configure than it does during a warm reset. Table 4, Figure 1, and Figure 2 provide details of the power-on reset and warm reset timing requirements for the S29GL128S flash.

Table 4 Power-on and warm reset timing requirements

Parameter	Description	Type	S29L127J	S29GL128S
t_{VCS}	V_{CC} setup time to first access	Min.	50 µs	300 µs
t_{VIOS}	V_{IO} setup time to first access	Min.	N/A	300 µs
t_{RPH}	RESET# LOW to CE# LOW	Min.	N/A	35 µs
t_{RP}	RESET# LOW to RESET# HIGH	Min.	500 ns	200 ns
t_{RH}	RESET# HIGH to CE# LOW	Min.	50 ns	50 ns
t_{CEH}	CE# HIGH to CE# LOW	Min.	N/A	20 ns

The durations to the first memory access after power on (t_{VCS}) are different between S29PL127J and S29GL128S devices. However, S29GL128S devices do require CE# to remain HIGH for at least t_{CEH} prior to CE# falling edge which initiates the first access. This t_{CEH} is not a requirement for S29PL127J devices.

The warm reset durations are different between S29PL127J and S29GL128S. S29PL127J takes approximately 550 ns (t_{RP} +t_{RH}) to complete a warm reset, whereas S29GL128S devices require 250 ns (t_{RP} +t_{RH}) to complete the same warm reset. t_{CEH} is a requirement for S29GL128S devices which was not a requirement for S29PL127J devices.

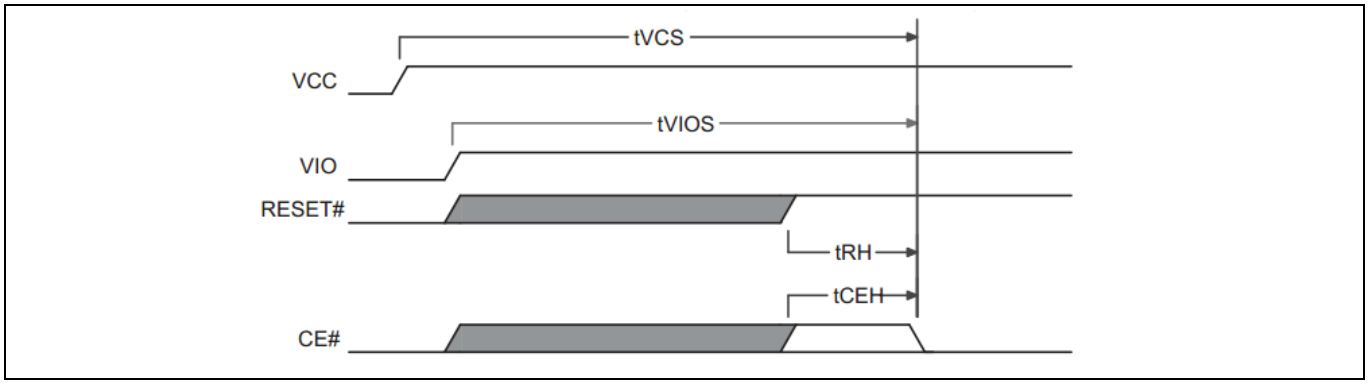

Figure 1 S29GL128S - power-up reset timing

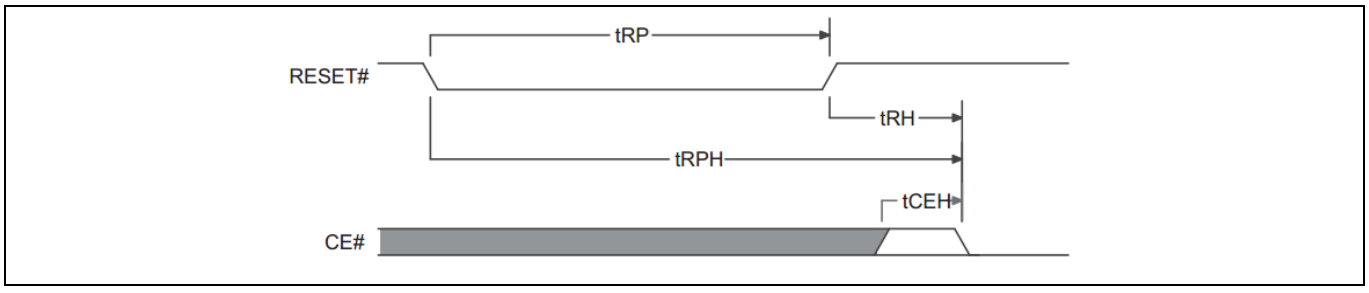

Figure 2 S29GL128S - warm reset timing

Power-on reset (POR) and warm reset timing

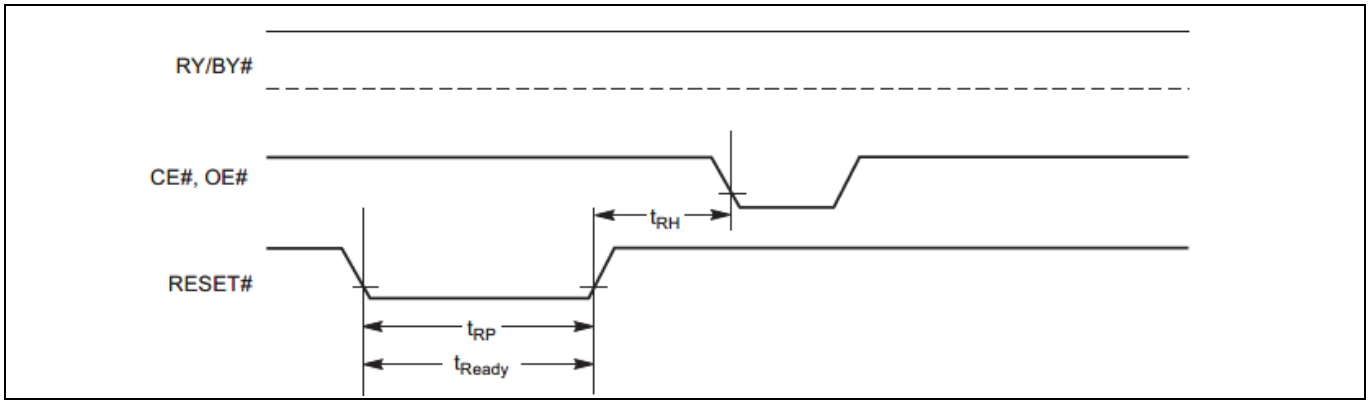

Figure 3 S29PL127J reset timings (not during embedded algorithms)

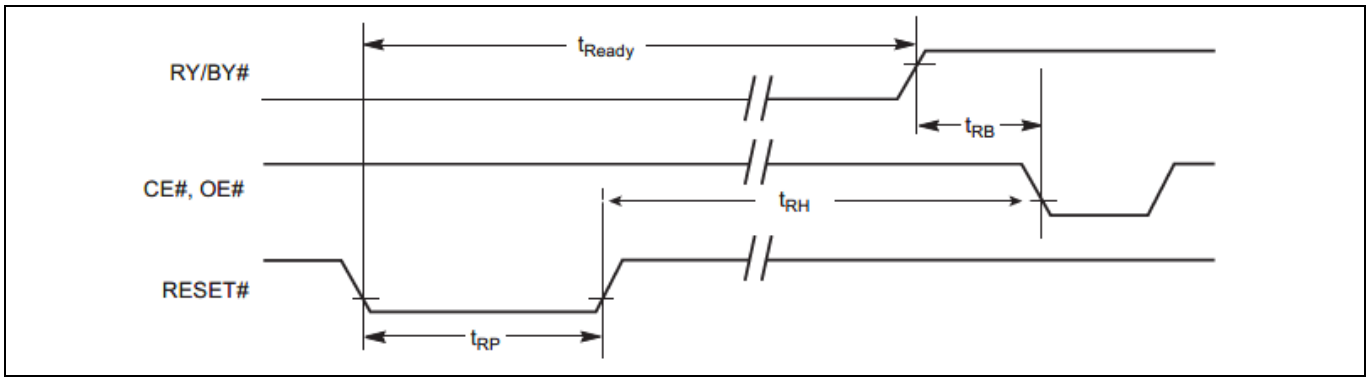

Figure 4 S29PL127J reset timings (during embedded algorithms)

5 DC and AC parameter differences

The differences in DC parameters will not cause any issue during migration.

Table 5 DC specification differences (–40°C to +85°C)

Parameter	Description	Type	S29PL127J	S29GL128S
PL-J --- GL-S	**Power usage**			
ICC9 --- ICC2	Active page read current at 10 MHz	Typ.	10 mA	9 mA
		Max.	15 mA	25 mA
ICC3 --- ICC4	VCC standby current	Typ.	0.2 µA	70 µA
		Max.	5 µA	100 µA
ICC4 --- ICC5	VCC reset current	Typ.	0.2 µA	10 mA
		Max.	5 µA	20 mA
ICC5 --- ICC6	Automatic sleep mode	Typ.	0.2 µA	3 mA
		Max.	5 µA	6 mA
	Logic levels			
VIL	Input LOW voltage	Min.	–0.4 V	–0.5 V
		Max.	0.4 V	0.3 x VIO
VIH	Input HIGH voltage	Min.	VIO–0.4	0.7 x VIO
		Max.	VIO+0.4	VIO + 0.4

Table 6 provides side-by-side comparisons of AC parameter specification differences between S29GL128S and S29PL127J (without the reset timing parameter differences documented in Table 4). All parameters should be reviewed against actual application implementations to ensure a successful migration.

For applications that utilize the Erase Suspend and/or Program Suspend features, it is important to review the system software ramifications of S29GL128S having a longer latency between issuance of the suspend and resume commands and the flash updating status and completing the transition between modes.

Note that all table specifications apply to the fastest speed option (90 ns for S29GL128S and 55 ns for S29PL127J), industrial temperature rated device with V_{CC} = V_{IO} = 2.7–3.6 V. See individual datasheets for performance specifications for other operating conditions.

Table 6 AC specification differences (–40°C to +85°C)

Parameter	Description	Type	S29PL127J	S29GL128S
Async read				
$t_{RC}/t_{ACC}/t_{CE}$	Read cycle time (ns)	Min.	80, 70, 65, 60, 55	90
t_{PACC}	Page access time (ns)	Min.	30, 25, 20	15
t_{DF}	Chip Enable to output High-Z	Max.	16 ns	15 ns
t_{DF}	Output Enable to output High-Z	Max.	16 ns	15 ns
Async WRITE				
t_{WC}	Write cycle time (ns)	Min.	80, 70, 65, 60, 55	60
t_{DS}	Data setup time (ns)	Min.	25, 30	30
t_{WP}	Write pulse width (ns)	Min.	35	25

DC and AC parameter differences

Parameter	Description	Type	S29PL127J	S29GL128S
t_{WPH}	Write pulse width HIGH (ns)	Min.	20 (t_{ACC} = 55nS), 25 (t_{ACC} = 60 nS–80 nS)	20
t_{CP}	CE# pulse width (ns)	Min.	35 (t_{ACC} = 55 nS), 40 (t_{ACC} = 60 ns–80 ns	25
t_{CPH}	CE# pulse width HIGH (ns)	Min.	20 (t_{ACC} = 55 nS), 25 (t_{ACC} = 60 nS–80 nS)	20
Suspend/resume				
t_{ESL}	Erase Suspend/Erase Resume	Max.	35 µs	40 µs
t_{PSL}	Program Suspend/Program Resume	Max.	35 µs	40 µs
t_{ERS}	Erase Resume to next Erase Suspend	Typ.	N/A	100 µs
t_{PRS}	Program Resume to next Program Suspend	Typ.	N/A	100 µs
Erase and programming performance				
	Sector erase time	Typ.	0.5 s	275 ms
	Chip erase time	Typ.	135 s	N/A
	Single word programming time	Typ.	6 µs	125 µs
	Total write buffer program time [1]	Typ.	N/A	340 µs
	Total accelerated effective write buffer program time per word	Typ.	N/A	1.33 µs
	Chip program time for a full write buffer operation	Typ.	50.4 s	N/A

[1] The S29PL127J does not support Write Buffer programming.

6 Packaging compatibility

S29PL127J package offerings:

- 80-ball fine pitch BGA (VBG080, 11 mm × 8 mm)
- 56-pin TSOP (TS056, 20 mm × 14 mm)

S29GL128S package offerings:

- 56-pin TSOP (TS056)
- 56-ball fortified ball grid array (VBU056, 9 mm × 7 mm)
- 64-ball fortified ball grid array (LAA064, 13 mm × 11 mm)
- 64-ball fortified ball grid array (LAE064, 9 mm × 9 mm)

Table 7 Package compatibility

Package type	S29PL127J	S29GL128S
56-pin TSO56	Available	Available
56-ball fortified BGA (VBU056)	N/A	Available
80-ball fine-pitch BGA (VBG080)	Available	N/A
64-ball fortified BGA (LAA064)	N/A	Available
64-ball fortified BGA (LAE064)	N/A	Available

7 Conclusion

For applications that do not require Simultaneous READ/WRITE operation, the S29GL128S is a suitable migration path from S29PL127J. The parameters and enhanced features make migration easy with minimal to no issues.

S29PL127J has flexible bank architecture consisting of four banks:

- Bank A: PL127J -16 Mbit (8 KB × 8 and 64 KB × 31)
- Bank B: PL127J - 48 Mbit (64 KB × 96)
- Bank C: PL127J - 48 Mbit (64 KB × 96)
- Bank D: PL127J -16 Mbit (8 KB × 8 and 64 KB × 31)

S29GL128S has uniform sector architecture with a sector size of 128 KB. See the S29GL128S [2] and S29PL127J [1] datasheets for detailed information.

References

[1] S29PL127J 128 Mb flash datasheet, 002-00615, Rev. *F, August 20, 2019.

[2] S29GL128S 128 Mb MIRRORBIT™ flash datasheet, 001-98285 Rev. *U, June 25, 2024.

Revision history

Document revision	Date	Description of changes
**	2024-10-23	Initial release

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