Design and layout guide for CYRS17B/CYEL17B flash Quad devices

About this document

Scope and purpose

This document describes system PCB layout recommendations for optimizing signal layout and power supply lines to prevent signal integrity problems when using CYRS17B/CYEL17B families of flash Quad SPI devices.

Intended audience

This document is intended for all technical experts using CYRS17B/CYEL17B flash Quad SPI devices from Infineon for a PCB design.

Table of contents

About this document **1**
Table of contents **2**
1 Introduction **3**
1.1 Signals 3
2 Signal integrity and impedance control **7**
3 Signal routing guidelines **8**
3.1 Maximum total length 8
3.2 Length matching 9
3.3 Signal spacing 9
3.4 Termination 9
4 Package diagrams **10**
4.1 Package connection 10
4.2 Package drawings 12
4.3 Land pattern recommendations 14
5 Power delivery guidelines **15**
5.1 Decoupling capacitor recommendations 16
6 Test points and oscilloscope measurements **17**
References **18**
Revision history **19**
Disclaimer **20**

1 Introduction

This document provides general design recommendations for a PCB that uses CYRS17B/CYEL17B family flash products. These guidelines include recommendations for both signal routing and power delivery to the device.

To achieve the best performance, the PCB design must provide an impedance- and loss-controlled environment, support a low-impedance power delivery system, and control the electromagnetic interference (EMI).

This document serves as an initial reference for PCB designs using CYRS17B/CYEL17B flash products. It does not eliminate the need to perform signal integrity and power delivery simulations. Use Infineon-provided IBIS models as well as IBIS models from controller vendors for signal timing and crosstalk simulations. You should verify actual characteristics empirically on prototype and validation build units.

If a design cannot meet the recommendations provided herein, perform detailed simulations to determine whether deviations from the recommendations affect the bus performance.

As a flash user, you may already be familiar with the basic operations in NOR flash devices: Read, Program, and Erase. The CYRS17B/CYEL17B families provide many other features to satisfy the diverse needs of different users. First seek to understand the datasheet before reading this document, especially if you are not familiar with CYRS17B/CYEL17B devices in general.

The CYRS17B/CYEL17B products are built on an advanced 40-nm Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) process technology.

1.1 Signals

The CYRS17B / CYEL17B flash Quad SPI devices are 3.0 V NOR flash memories with Serial Peripheral Interface (SPI) (1-1-1), Quad (1-4-4), and Quad Peripheral Interface (QPI) (4-4-4). These interfaces serially transfer transactions, reducing the number of interface connection signals descriptions and schematic.

Table 1 summarizes the I/O found on CYRS17B/CYEL17B Quad SPI devices: not all are present on any given package. See product-specific datasheets listed in References to determine the I/O connections that are available for a device and for additional information regarding their function and operation.

Introduction

Table 1 Signal descriptions

Signal	Type	Mandatory/ optional	Description
CS#	Input	Mandatory	Chip Select (CS#). All bus transactions are initiated with a HIGH-to-LOW transition on CS# and terminated with a LOW-to-HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the Active mode. When CS# is driven HIGH, the device enters the Standby mode, unless an internal embedded operation is in progress. All other input pins are ignored, and the output pins are put in High-Z state.
SCK	Input	Mandatory	Serial Clock (SCK) provides timing of the serial interface.
IO0/SI	Input/ output	Mandatory	IO0 input/output for Dual or Quad SPI protocol Serial Input (SI) for single SPI protocol
IO1/SO	Input/ output	Mandatory	IO1 input/output for Dual or Quad SPI protocol Serial Output (SO) for single SPI protocol
IO2/WP#	Input/ output (Weak pull-up)	Mandatory	IO2 input/output for Quad SPI protocol Write Protect (WP#) for single and dual SPI protocol. If write protection is enabled, the host system is required to drive WP# HIGH or LOW during write register commands. When the WP# function is available when the Quad mode is disabled (CR1V[1] = 0), the pin acts as an input only with no pull-up. So it is recommend that the system drive the input high when not using the WP# function.
IO3	Input/ output	Mandatory	IO3 input/output for Quad SPI protocol.
RESET#	Input (Weak pull-up)	Optional	Hardware Reset (RESET#). When LOW, the device will self-initialize and return to the array read state. IO[3:0] are placed into the High-Z state when RESET# is LOW. RESET# includes a weak pull-up, meaning that if RESET# is left unconnected, it will be pulled up to the HIGH state on its own.
INT#	Output (Open drain)	Optional	System Interrupt (INT#). When LOW, the device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output. The recommended pull-up resistor for the INT# outputs is 5 kΩ to 10 kΩ.
V_{DD}	Power supply	Mandatory	Core power supply.
V_{SS}	Power supply	Mandatory	Core ground.
V_{DDIO}	Power supply	Mandatory	I/O supply.
DNU	–	–	Do Not Use. Do not route any PCB trace to DNU pins.

Introduction

Signal	Type	Mandatory/ optional	Description
NC	–	–	Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection can safely be used for routing space for a signal on a printed circuit board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{DD}.

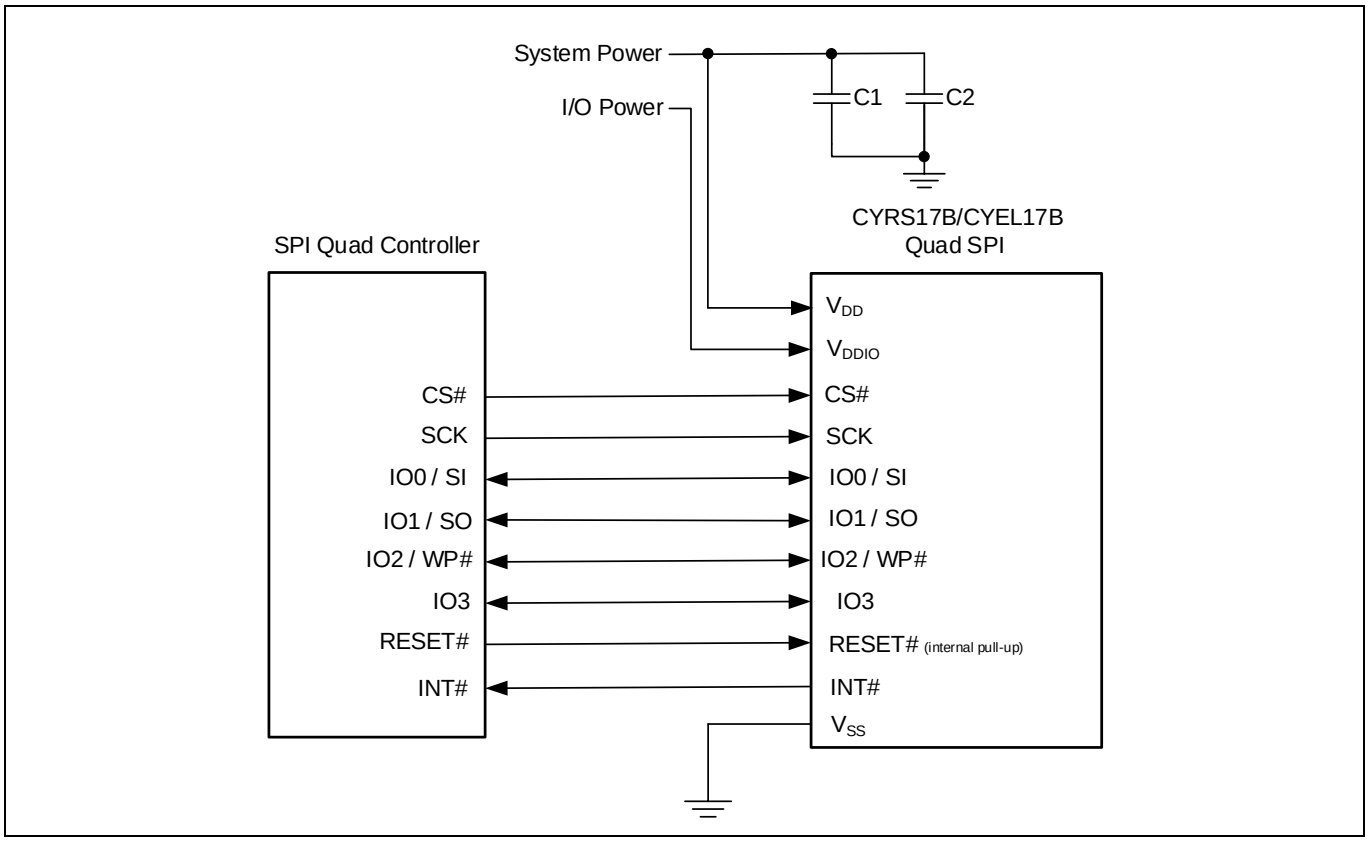


Figure 1 Quad SPI recommended schematic

Table 2 Recommended capacitor terminations

Parameter	Symbol	Recommended	Unit	Description
V_{DD} capacitor values[1]	C1	2 x 0.1	µF	Decoupling capacitors should be connected as close as possible to V_{DD} and V_{SS}.
	C2	2 x 1.0		

During signal routing, give priority to the signal groups to ensure that they maintain a high-quality signal. Table 3 ranks the signal integrity priority of the five groups, where '1' represents the highest priority and '5' represents the lowest.

[1] See section Power delivery guidelines for details.

Table 3 Signal Integrity Priority of Signal groups

Signal group	Pin names	Signal integrity priority
Clock	SCK	1
Data	IO0/SI, IO1/SO, IO2/WP#, IO3	2
Chip Select	CS#	3
Other controls	RESET#, INT#	4
Power/ground	V_{DD}, V_{DDIO}, V_{SS}	5

2 Signal integrity and impedance control

Infineon recommends the following actions to improve signal integrity and impedance control.

- Break out all signals on the top PCB layer, if the second layer is a ground plane. This will allow better impedance control and smaller impedance mismatch between breakout traces and traces outside the breakout area.
- Connect V_{DD} and V_{DDIO} to the nearest power plane through vias that are located as close to the target power ball/pin as possible. Traces from the land pad to the vias should be as thick as possible.
- Connect V_{SS} to the nearest ground plane through vias that are located as close to the target ground ball/pin as possible. Traces from the land pad to the vias should be as thick as possible.
- Use a smaller trace width (between 4 mil and 6 mil) and space the adjacent traces approximately three trace widths apart to achieve a 50-ohm impedance. The impedance of data traces depends on the PCB stack-up and the trace width. Use either microstrip or stripline interconnects so long as the continuous trace impedance is 50 ohms (±10 percent) throughout the routing path.
- Use buried vias and as few vias as possible to reduce impedance discontinuities due to additional capacitive loading arising from through-hole vias. Any via attached to a trace will alter the signal delay of that trace.
- Route all signal groups on the same signal layer and in the same signal configuration, either all microstrip or all stripline.

3 Signal routing guidelines

The following guidelines define the recommended trace width and trace spacing, total length limitation, and length matching requirements to achieve optimal signal integrity and timing margins. These recommendations assume point-to-point routing between the host controller and the SONOS flash memory. If this is not the case, select the topology type to follow star, T, or daisy chain. Infineon recommends star or T topology with appropriate termination resistors determined from IBIS simulations. Consider performing signal integrity simulations using Infineon-provided IBIS models to determine guidelines tailored to your specific application (including lower frequency for a particular interface).

- Determine the exact values of signal trace width and trace spacing based on the trace impedance requirement.
- Make the V_{SS} plane serve as a primary reference or return path for all signals. The power layer should only serve as a secondary signal reference option where a solid, continuous ground reference is present.
- Avoid gaps or voids in reference planes to minimize or eliminate return current discontinuity.
- Avoid routing traces at the edge of the reference plane.
- When routing data signals, route the longest signals first. This allows adjustment for signals with shorter lengths.
- Isolate the ground return path of analog signals from digital noise whenever possible.
- Keep all recommended signal routing lengths equal to the distance from package pin (source) to package pin (destination) by considering package length compensation.
- Use signal integrity tools to estimate actual trace velocities and path delays to validate the electrical properties depending on the dielectric material. Infineon determines electrical properties of signal routing by assuming that the dielectric material is FR4. With this assumption, 1 inch equals approximately166 ps.

3.1 Maximum total length

- The total load capacitance, which directly affects signal integrity, defines the absolute maximum length of signals with respect to their reference plane.
  - The total load capacitance should remain below the load capacitance (C_L) value listed in the datasheet.
  - Total load capacitance includes the following:
    - Total trace length capacitance (~3.3 pF/inch with FR4 assumption)
    - Maximum pin capacitance associated with any parasitic capacitance of connected devices such as connectors and series resistors
    - Maximum pin capacitance of the controller package.
- The Read/Write operation timing requirements bound the total length of clock, control, and data signal routing lines, as stated in the product datasheet. Perform a channel timing simulation to ensure that the system meets these critical timing requirements.
- The recommended practice is to begin with AC timing equations for key timing parameters provided on the CYRS17B/CYEL17B families of flash Quad SPI devices and controller datasheets ([1], [2]) for the flash interface.

3.2 Length matching

- Length matching refers to trace lengths from the memory package pin to the signal pin of the controller. Length matching must include the effective electrical length of any vias.
- Table 4 provides signal skew recommendations for various signal groups. It is important to note the signal polarities (rising-edge and falling-edge triggers) as well as the lead and lag timing to determine whether a specific control signal should always lead or lag compared to another signal or data bus.

Table 4 Length match recommendations for Signal groups

Signal group	Length match recommendation for 133 MHz
IO [0:3] to IO [0:3]	±30 mils
SCK/SCK# to IO[0:3]	±200 mils
SCK/SCK# to CS#	±1500 mils
SCK/SCK# to DS	±1500 mils
RESET# to CS#	±2000 mils

- Avoid routing these signals adjacent to higher-frequency signals to minimize noise from crosstalk.

3.3 Signal spacing

- The center-to-center trace spacing should be greater than three times ‘H’ within a signal group is, where H is the dielectric height between the signal and ground reference layer.
- The center-to-center trace spacing between signal groups should be greater than three times the trace width. In addition, the center-to-center trace spacing between flash signals and other interface signals should be greater than three times the trace width as well. Figure 2 provides a visualization of the recommended signal trace spacing.

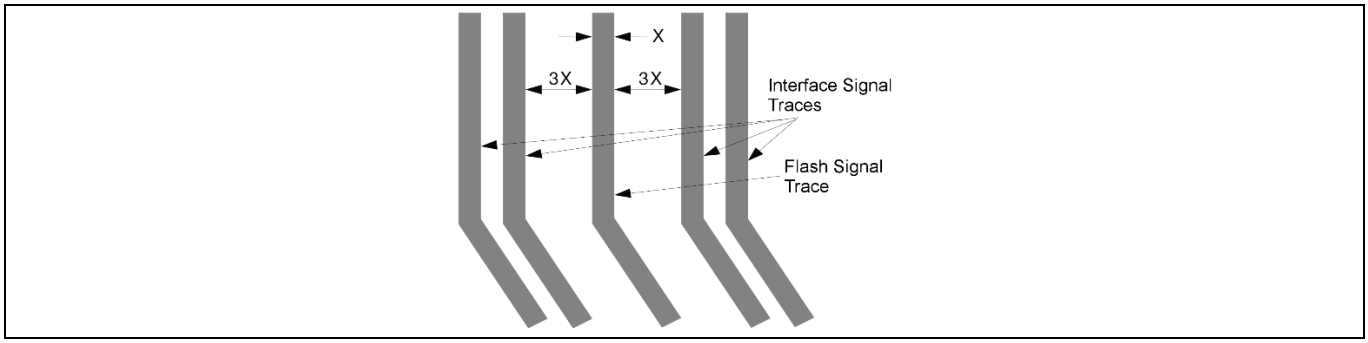


Figure 2 Recommended signal trace spacing on the PCB

3.4 Termination

Review the drive strength/impedance of the controller I/O as well as transmission line routing to determine whether series termination is required on these lines. Drive strength for all three (fab process corner, voltage, and temperature [PVT]: typical, minimum, and maximum corners) can be determined by reviewing the IBIS IV/VT curves.

4 Package diagrams

4.1 Package connection

Quad SPI devices are provided in 68-lead ceramic quad flatpack and 100-lead thin quad flatpack packages. The package height is device-dependent.

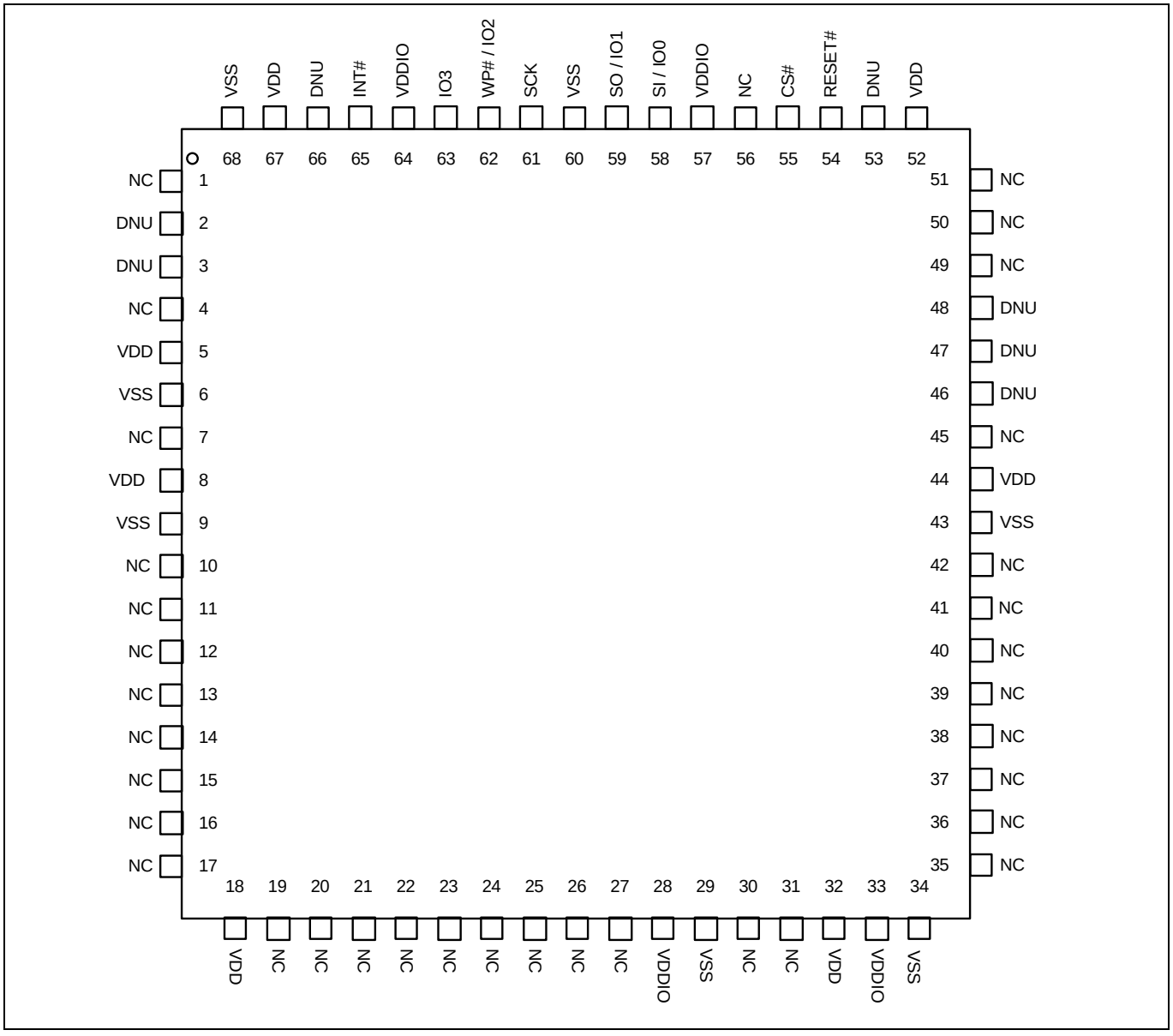


Figure 3 68-lead ceramic quad flatpack (68-QFP), top view

Package diagrams

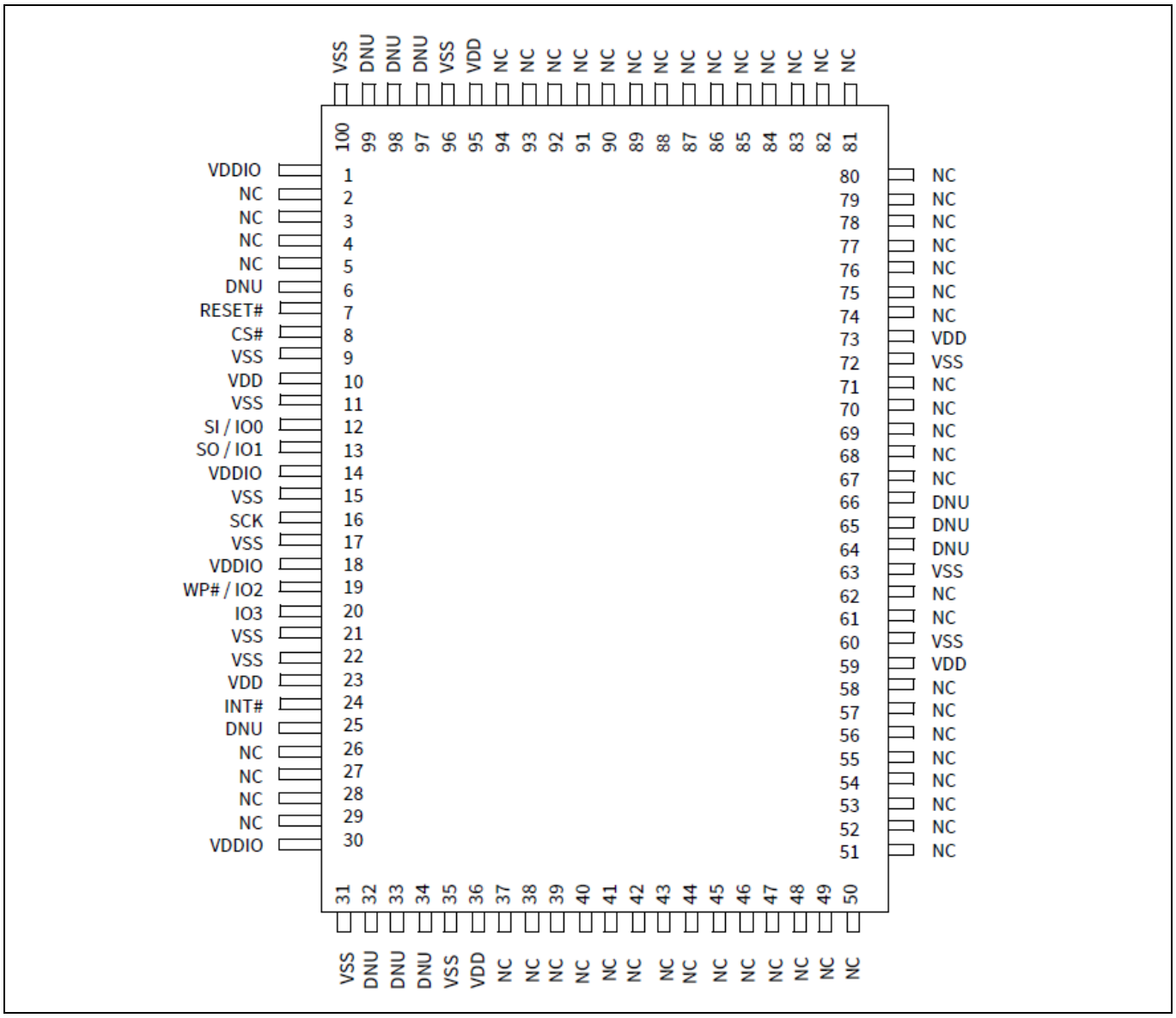
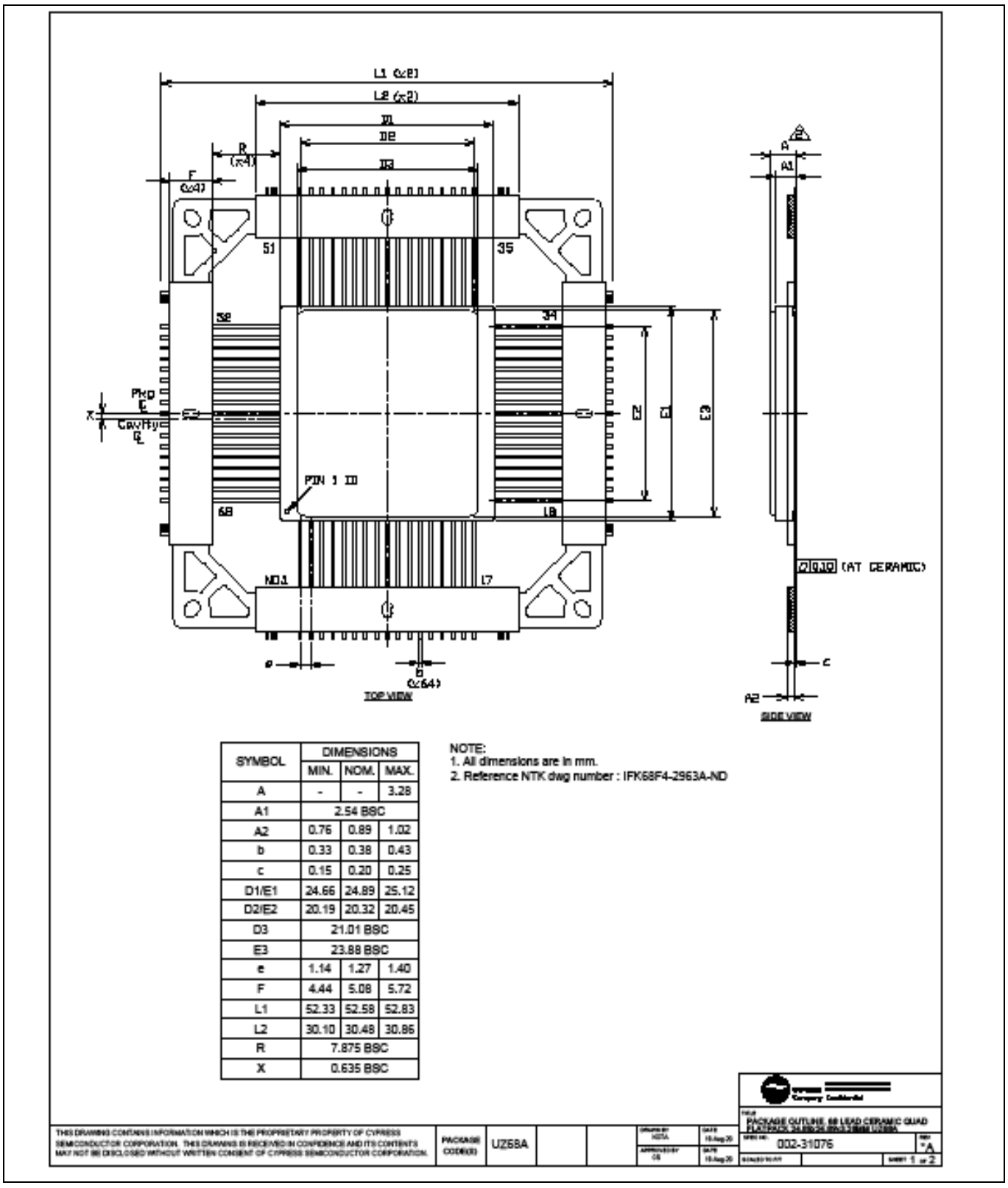


Figure 4 100-lead thin quad flatpack (100-TQFP), top view

4.2 Package drawings

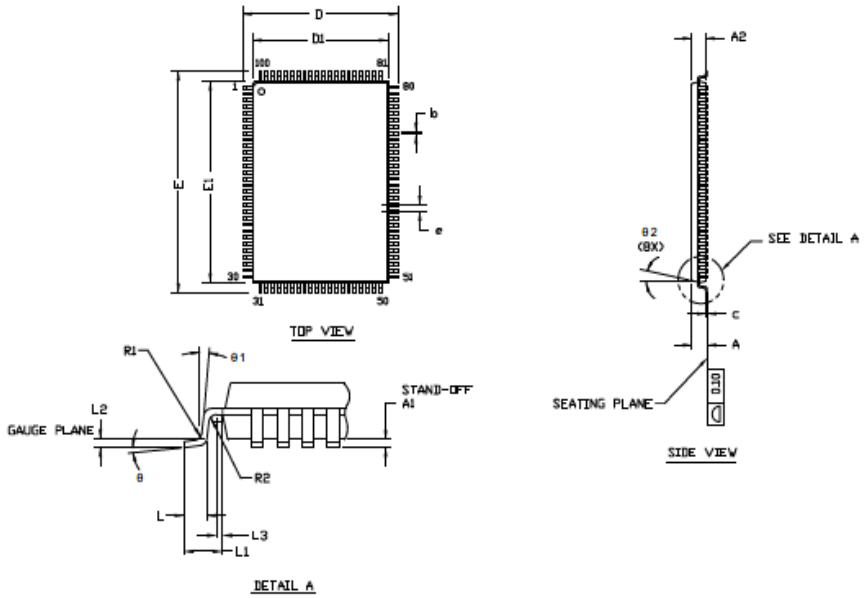
Applicable package drawings are provided in each CYRS17B/CYEL17B flash datasheet. These drawings are included herein. See the product datasheet ([1], [2]) for the latest package outline information.



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	3.28
A1	2.54 BSC		
A2	0.76	0.89	1.02
b	0.33	0.38	0.43
c	0.15	0.20	0.25
D1/E1	24.66	24.89	25.12
D2/E2	20.19	20.32	20.45
D3	21.01 BSC		
E3	23.88 BSC		
e	1.14	1.27	1.40
F	4.44	5.08	5.72
L1	52.33	52.58	52.83
L2	30.10	30.48	30.86
R	7.875 BSC		
X	0.635 BSC		

Figure 5 68-lead ceramic quad flatpack (68UZ)

Package diagrams



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
R1	0.08	—	0.20
R2	0.08	—	0.20
θ	0°	—	7°
θ1	0°	—	—
θ2	11°	12°	13°
c	—	—	0.20
b	0.22	0.30	0.38
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
L3	0.20	—	—
e	0.65 TYP		

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
3. JEDEC SPECIFICATION NO. REF: MS-026.

Figure 6 100-lead thin quad flatpack (100AZ)

4.3 Land pattern recommendations

Applicable PCB land pattern recommendations for a 100-lead thin quad flatpack is provided here in Figure 7.

Note: *Ceramic QFP packages are shipped to the customer prior to trim and form. Customer completes the trim and form operation and mounts the package on their PCB. Therefore, SMT recommendations could vary based on customer process and PCB. For this reason, the SMT recommendation for these packages is not provided.*

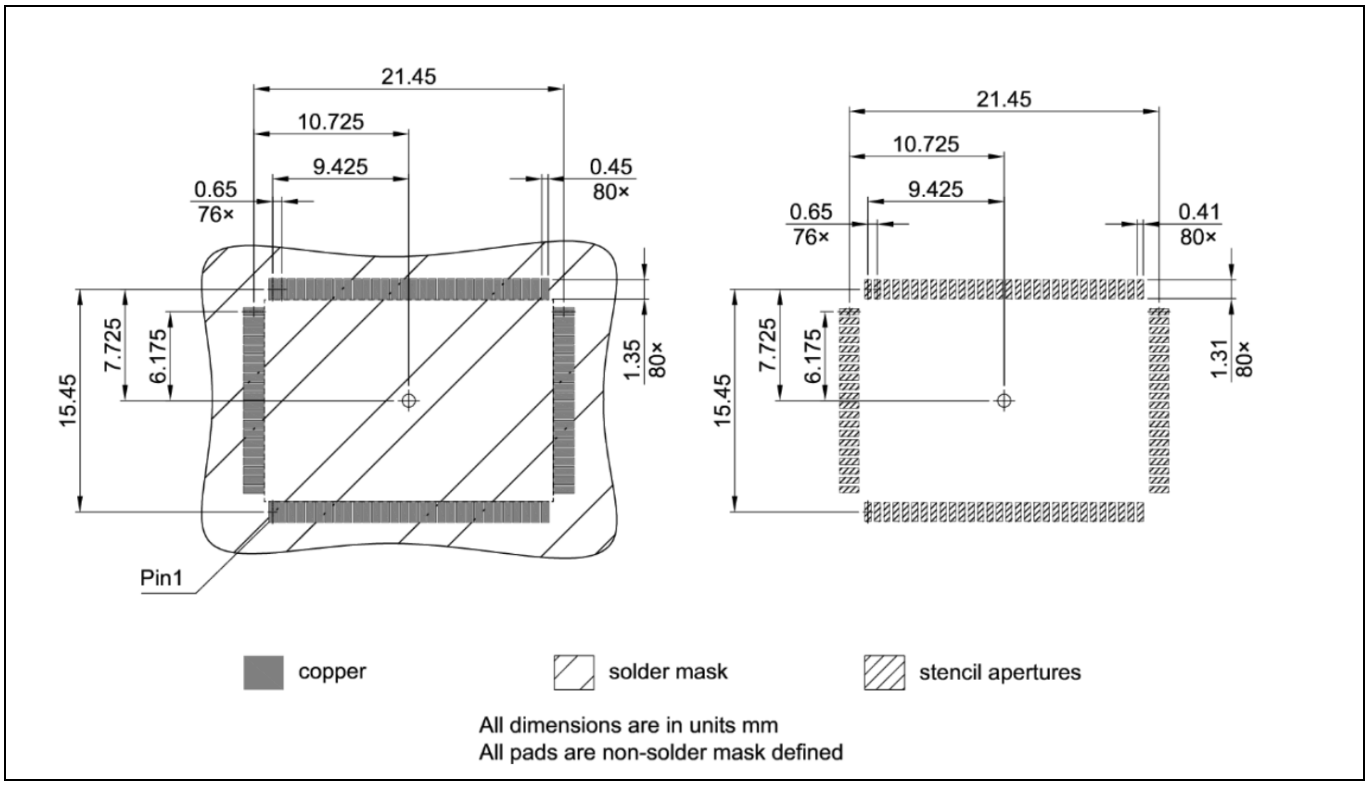


Figure 7 100AZ proposed land pattern

5 Power delivery guidelines

The following power delivery guidelines will help ensure that there are no power issues within the system.

- Connect each V_{SS} pin to a solid ground plane with its own unique via to improve IR drop.
- Connect V_{DD} (and V_{DDIO}) pins/balls to a supply plane with its own unique via to improve IR drop.
- Gaps between power planes should be at least 20 mil where possible. A gap of at least 80 mil should exist between power islands on the same layer if possible. The air gap between power islands must be greater than 40 mil, preferably as much as 100 mil.
- Power islands, such as V_{DD} island, should be at least 250-mil wide at the narrowest point to avoid bottlenecks.
- Maintain a minimum trace width of 20 mil for all supply traces, except at the package breakout area where vias tie the supply to the nearest supply plane. Route the supply and ground traces (or planes) close to each other to avoid large inductive loops.
- Keep the supply trace lengths less than or equal to 400-mil and keeping the trace widths greater than or equal to 20 mil.
- Use trace widths greater than 20 mil to maintain low impedance from the voltage regulator to the flash voltage supply pins/balls as well as from the voltage regulator to the controller flash interface supply pins/balls.
- If the voltage regulator is not on the same PCB as the flash package when using a module configuration, maintain the lowest possible impedance on traces to V_{DD} and V_{SS}. Wider traces can help to ensure a lower impedance.
- If there is a connector between the host controller and flash device, use a G: S/P: G type connector configuration where ‘S’ refers to signal, ‘G’ refers to V_{SS}, and ‘P’ refers to V_{DD}.
- It is best to add V_{DD} and V_{SS} test points as close as possible to each flash package and next to the voltage regulator. These test points allow the measurement of V_{DD}-V_{SS} and V_{DDIO}-V_{SS} waveforms at both VRM and the package.

5.1 Decoupling capacitor recommendations

- Place the PCB decoupling capacitors as close to the package as possible.
- Select decoupling capacitors that have low equivalent series inductance (ESL) and equivalent series resistance (ESR).
- V_{DD} and V_{SS} trace routing from the capacitor should be as wide as possible to avoid inductive and resistive effects.
- A minimum two 1-µF 0402 ceramic capacitors should be placed between V_{DD} and V_{SS} near each side of the package.
- In addition to decoupling capacitors, two 0.1-µF 0402 ceramic capacitors should be placed as close to the package as possible between V_{DD} and V_{SS}.
- Recommends using X7R or X5R capacitors with a rated voltage greater than or equal to at least two times V_{DD} max.
- The decoupling capacitor trace length should remain short and should have a unique via, not shared with another decoupling capacitor. Figure 8 presents good and poor examples of decoupling capacitor routing techniques.

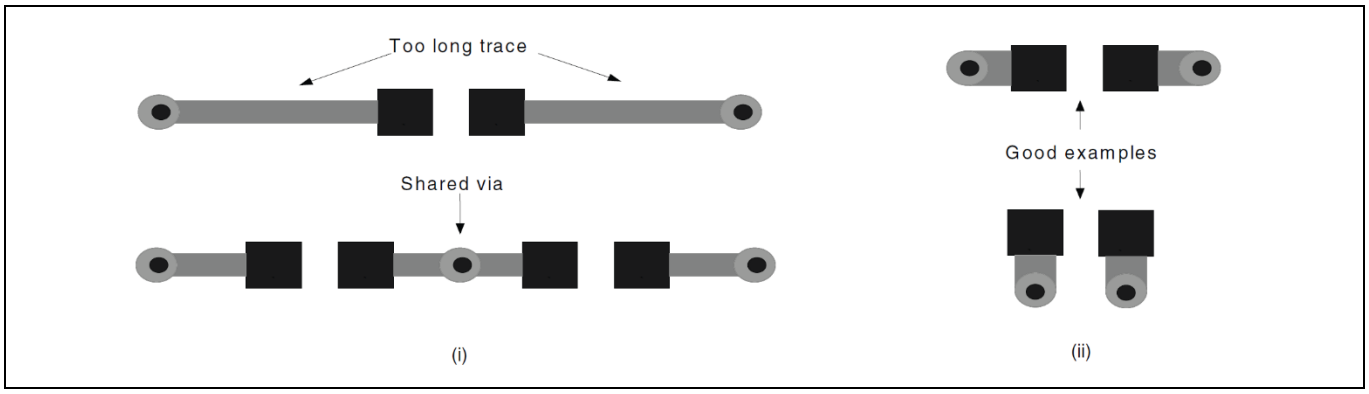


Figure 8 Decoupling capacitor routing techniques: (i) Poor routing examples, (ii) Good routing examples

6 Test points and oscilloscope measurements

You should perform signal quality, timing, and power delivery characterization using industry-standard digital signal evaluation techniques. The statements below outline a few of those techniques.

- Test points should be as close as possible to the controller and the SEMPER™ NOR Flash package pins for IO[7:0] signals. In addition, the test points should be located as close as possible to the SEMPER™ NOR Flash memory package pin for the remaining the signals.
- Measure meaningful signals as close to the flash memory device as possible when the controller is driving. When the flash memory device is driving, the opposite is true.
- While creating a test pad, the stub (extra inductance and capacitance) resulting from the test pad should be minimized. It is better to probe at the breakout via rather than creating test pad stubs. In addition, in the case of 4-layer PCBs with through-hole vias, probe signals at the bottom of the PCB on the through-hole vias if possible.
- While performing scope measurements, use a 3-GHz or greater bandwidth scope and low-impedance probes. This will provide a more accurate representation of the waveform transition (such as the rising and the falling portion of the waveform).
- Always measure V_{DD}-V_{SS} at the controller, the voltage regulator, next to the connector (either side), and at the flash memory. This needs to be performed prior to making any signal measurements to ensure that the supply is not noisy, which will affect the signal timing. In addition, these measurements establish the IR drop from regulator to controller or the regulator to the flash device.
- While measuring signals, it is a good idea to set the trigger on the most common switching signals, such as CS# or CK.

References

Contact Infineon Support to obtain these documents.

[1] CYRS17B datasheets

- 002-30115: CYRS17B512, 512 Mb (64 MB) serial NOR flash, SPI/QSPI, 3.3 V, Radiation hardened
- 002-38837: CYRS17B01G, 1 Gb (128 MB) serial NOR flash, Dual-Quad, 3.0 V, Radiation tolerant

[2] CYEL17B datasheet

- 002-39759: CYEL17B512, 512 Mb radiation tolerant NOR flash, Serial (QSPI), 3.3 V

Revision history

Document revision	Date	Description of changes
**	2024-06-27	Initial release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-06-27

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2024 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

002-40090 Rev. **

Important notice

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.