Migrating from S26KL-S/S26KS-S HYPERFLASH™ to S26HL-T/S26HS-T SEMPER™ flash with HYPERBUS™

About this document

Scope and purpose

This application note provides guidelines for migration from 65-nm KL/KS-S HYPERFLASH™ product family to 45-nm HL/HS-T SEMPER™ flash product family. It describes the similarities and the differences to facilitate a seamless conversion.

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1 Introduction

This document provides guidelines for migrating from S26KL/KS-S HYPERFLASH™ family of products to S26HL/HS-T SEMPER™ family of products. It discusses all known issues that may be encountered when facilitating this conversion.

S26KL/KS-S HYPERFLASH™ devices are 3.0-V/1.8-V NOR flash memories with the HYPERBUS™ interface and are built on 65-nm MIRRORBIT™ process technology. S26HL/HS-T SEMPER™ flash devices are also 3.0-V/1.8-V NOR flash memories with HYPERBUS™ and Legacy (x1) SPI interfaces, but are built on an advanced 45-nm MIRRORBIT™ process technology. Among the advances are higher bandwidth through higher frequency (400 MB/s – 200 MHz), interface data integrity through interface CRC, and enhanced endurance/retention through endurance flex architecture (partitioned memory array employing wear leveling). See S26HL/HS-T datasheets for a full description of new features.

2 Feature comparison

S26HL/HS-T supports a superset of the S26KL/KS-S feature set. Table 1 summarizes the feature similarities and differences. New feature set summary discusses these differences in more detail.

Table 1 Feature comparison

Feature/parameter	S26HL/HS-T	S26KL/KS-S
Technology node	45-nm MIRRORBIT™	65-nm MIRRORBIT™
Architecture	NOR flash	NOR flash
Density	512 Mb, 01 Gb	512 Mb
Interface width	x1, x8	x8
Supply voltage	1.70 V – 2.00 V 2.70 V – 3.60 V	1.70 V – 1.95 V 2.70 V – 3.60 V
Read (DDR) bandwidth (1.8 V)	400 MB/s (200 MHz)	333 MB/s (166 MHz)
Read (DDR) bandwidth (3.0 V)	332 MB/s (166 MHz)	200 MB/s (100 MHz)
Program buffer size	256 B or 512 B	512 B
Erase sector size	4 KB and 256 KB	4 KB or 256 KB
Parameter sector size	4 KB	4 KB
Number of parameter sectors	32	8
Secure Silicon Region (SSR)	1024 B	1024 B
Advanced Sector Protection (ASP)	Yes	Yes
Suspend/Resume	Erase/Program	Erase/Program / Memory Array CRC
Addressing	HYPERBUS™ - 6 bytes SPI – 3 or 4 bytes	HYPERBUS™ - 6 bytes
Hardware reset	Yes	Yes
Industrial temperature	–40°C to +85°C	–40°C to +85°C
Industrial plus	–40°C to +105°C	–40°C to +105°C
Automotive AEC-Q100 grade-3 temp.	–40°C to +85°C	–40°C to +85°C
	–40°C to +105°C	–40°C to +105°C
Automotive AEC-Q100 grade-2 temp. Automotive AEC-Q100 grade-1 temp.	–40°C to +125°C	–40°C to +125°C
Deep Power Down	Yes	Yes
Device identification	Yes	Yes
Common flash interface	No	Yes
Serial Flash Discoverable Parameters (SFDP)	Yes	No
Unique identification	Yes	No

(table continues...)

Table 1 (continued) Feature comparison

Feature/parameter	S26HL/HS-T	S26KL/KS-S
AutoBoot	Yes	No
Memory array CRC	Yes	Yes
Interface CRC	Yes	No
Endurance flex architecture	Yes	No
Error Correcting Code (ECC – SECDED)	Yes	Yes
Packages 512 Mb 1 Gb	24-ball BGA (6×8 mm, 5×5 ball) 24-ball BGA (8x8 mm, 5x5 ball)	24-ball BGA (6×8 mm, 5×5 ball)
Legacy single SPI boot mode	Yes	No

3 New feature set summary

This section summarizes the new features in S26HL/HS-T devices. For details, see the device datasheet.

3.1 Serial Flash Discoverable Parameter (SFDP)

Serial Flash Discoverable Parameter (SFDP) is a JEDEC standard that provides a consistent method of describing the functional and feature capabilities of serial flash devices using a standard set of internal parameter tables. These parameter tables are queried by the host system software to enable adjustments needed to accommodate divergent features from multiple vendors.

Infineon supports SFDP in all its SPI NOR flash devices.

3.2 AutoBoot

The HYPERBUS™ protocol requires three clock cycles (48 bits) of command and address shifting to initiate a read command. To read the boot code, the host memory controller or processor must supply the read command from a hardwired state machine or from the internal ROM code. The AutoBoot feature allows the host memory controller to receive boot code from an S26HL/HS-T device immediately after the end of reset, without having to send a read command. This saves three clock cycles and simplifies the logic needed to initiate the reading of the boot code.

3.3 Interface CRC

One of the most critical aspects of communication between a host and a slave device is ensuring the integrity of the information transferred. Cyclic redundancy check (CRC) is an error-detecting code commonly used in devices to detect unintentional changes to raw data. A slaved device enabled with interface CRC calculates a fixed-length binary sequence, known as a CRC checksum, for each block of transferred data (host to slave or slave to host). The host device must also calculate its own CRC checksum on the same transferred data block. If the host calculated CRC checksum does not match the checksum generated by the slave, it indicates that the transferred block incurred a data error; the host device can now take corrective action such as requesting the data block to be sent again.

S26HL/HS-T supports the interface CRC functionality. It calculates the CRC checksum of all interface data (instruction, address, and data) and stores the checksum in a register that the host can access. This enables the host to take appropriate actions in the event of an error.

3.4 Endurance flex architecture

Flash devices, when subjected to a high number of program/erase cycles, can potentially suffer from degraded data retention and/or shortened device lifespan. The endurance flex architecture technology in S26HL/HS-T devices allow the user to configure the memory array as either high-endurance and/or long-retention partitions to enhance reliability. To enhance program/erase cycling in high-endurance partitions, wear leveling is employed, which evenly distributes program/erase cycles over the sectors included in the high-endurance partitions.

3.5 Legacy (x1) SPI Boot mode

S26HL/HS-T SEMPER™ flash devices support the Legacy (x1) single SPI (1S-1S-1S) interface mode with a limited set of instructions to read SFDP, to enable access of the memory array (boot code reading), device configuration, and transitioning to the HYPERBUS™ interface mode.

***Note**: See the device datasheet for details on supported SPI instructions.*

4 Command set comparison

Table 2 summarizes the supported commands for each device. Differences are discussed in subsequent sections.

Table 2 Command set comparison

Transaction	Description	Cycles	S26HL/HS-T	S26KL/KS-S
RDMARY_1_0	A Read transaction allows reading out the memory array data at the given address and places it on DQ[7:0].	1	Yes	Yes
ENSPIM_3_0	The Enter SPI transaction changes the device interface from HYPERBUS™ to Legacy (x1) SPI.	3	Yes	No
SRASOE_1_0	The Software Reset/ASO Exit transaction returns the device to reading memory array data mode when device is in ASO. It also clears SR0[5,4,3,1,0] when the device is not busy or is in the middle of a transaction sequence or in an ASO.	1	Yes	Yes
ENTDPD_3_0	The Enter Deep Power Down Mode transaction moves the device into the lowest power consumption mode.	3	Yes	Yes
RDVSTR_2_0	The Read Status Register transaction allows the Status Register contents to be read with data placed on DQ[7:0].	2	Yes	Yes
CLVSTR_1_0	The Clear Status Register Failure Flags transaction resets all failure flags being reported.	1	Yes	Yes
PRNPOR_4_0	The Program Non-Volatile POR Timer Register transaction programs the value which is multiplied by t_{POR_CK} (25 to 42 µs) into the 16-bit POR Time Register to define the length of extension to the RSTO# pulse beyond t_{VCS} with data placed on DQ[7:0].	4	Yes	Yes
RDNPOR_4_0	The Read Non-Volatile POR Timer Register transaction allows reading the contents of the 16-bit POR Time Register and places it on DQ[7:0].	4	Yes	Yes
PGVINC_4_0	The Program Volatile Interrupt Configuration Register transaction programs the 16-bit Interrupt Configuration register with the data placed on DQ[7:0].	4	Yes	Yes
RDVINC_4_0	The Read Volatile Interrupt Configuration Register transaction allows reading the contents of the 16-bit Interrupt Configuration register and places it on DQ[7:0].	4	Yes	Yes
PGVINS_4_0	The Program Volatile Interrupt Status Register transaction programs the 16-bit Interrupt Status register with the data placed on DQ[7:0].	4	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description	Cycles	S26HL/HS-T	S26KL/KS-S
RDVINS_4_0	The Read Volatile Interrupt Status Register transaction allows reading the contents of the 16-bit Interrupt Status register and places it on DQ[7:0].	4	Yes	Yes
PGVCR1_4_0	The Program Volatile Configuration Register 1 transaction programs the 16-bit Volatile Configuration register 0 with the data placed on DQ[7:0].	4	Yes	Yes
PGVCR2_4_0	The Program Volatile Configuration Register 2 transaction programs the 16-bit Volatile Configuration register 1 with the data placed on DQ[7:0].	4	Yes	Yes
RDVCR1_4_0	The Read Volatile Configuration Register 1 transaction allows reading the contents of the 16-bit Volatile Configuration register 0 and places it on DQ[7:0].	4	Yes	Yes
RDVCR2_4_0	The Read Volatile Configuration Register 2 transaction allows reading the contents of the 16-bit Volatile Configuration register 1 and places it on DQ[7:0].	4	Yes	Yes
PGNCR1_4_0	The Program Non-Volatile Configuration Register 1 transaction programs the 16-bit Non-Volatile Configuration register 0 with the data placed on DQ[7:0].	4	Yes	Yes
PGNCR2_4_0	The Program Non-Volatile Configuration Register 2 transaction programs the 16-bit Non-Volatile Configuration register 1 with the data placed on DQ[7:0].	4	Yes	Yes
ERNC12_3_0	The Erase Non-Volatile Configuration Registers 1 and 2 transaction erases the contents of the two 16-bit Non-Volatile Configuration registers (0, 1).	3	Yes	Yes
RDNCR1_4_0	The Read Non-Volatile Configuration Register 1 transaction allows reading the contents of the 16-bit Non-Volatile Configuration register 0 and places it on DQ[7:0].	4	Yes	Yes
RDNCR2_4_0	The Read Non-Volatile Configuration Register 2 transaction allows reading the contents of the 16-bit Non-Volatile Configuration register 1 and places it on DQ[7:0].	4	Yes	Yes
PGWORD_4_0	The Program Word transaction programs the data word (0s) supplied on DQ[7:0] in the addressed memory array.	4	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description	Cycles	S26HL/HS-T	S26KL/KS-S
LDBUFR_6_0	The Load Write Buffer transaction loads up to 256/512 bytes of data (0s) supplied on DQ[7:0] in the write buffer.	6	Yes	Yes
PGBFCM_1_0	The Program Write Buffer Confirm transaction tells the device to program the data loaded into the write buffer into the addressed memory array.	1	Yes	Yes
RSTWBA_3_0	The Reset Write to Buffer Abort transaction resets the Write Buffer Abort Status Flag (WRBFAB - STRV[3]) in the Status register.	3	Yes	Yes
ERCHIP_6_0	The Erase Chip transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array.	6	Yes	Yes
ERSCTR_6_0	The Erase Sector transaction sets all the bits of an addressed 256 KB sector or a 4 KB sector to 1 (all bytes are FFh).	6	Yes	Yes
BLKCHK_1_0	The Blank Check transaction confirms whether the selected Flash Memory Array sector is fully erased. ERSERR (STRV[5]- Bit 5 of the Status Register) will be cleared to 0 if the sector is erased and set to 1 if not erased.	1	Yes	Yes
EVERST_1_0	The Evaluate Erase Status transaction verifies that the last erase operation on the addressed sector was completed successfully. If the selected sector was successfully erased, the SESTAT (STRV[5]- Bit 0 of the Status Register) is set to 1.	1	Yes	Yes
SPERSE_1_0	The Suspend Erase transaction allows the system to interrupt an erase operation.	1	Yes	Yes
RSERSE_1_0	The Resume Erase transaction allows the system to resume an erase operation.	1	Yes	Yes
SPPROG_1_0	The Suspend Program transaction allows the system to interrupt a program operation.	1	Yes	Yes
RSPROG_1_0	The Resume Program transaction allows the system to resume a program operation.	1	Yes	Yes
IDSFE1_3_1	The ID/Unique ID/SFDP ASO Entry 1 transaction allows reading Device ID, Unique ID, and SFDP parameters. This entry transaction uses the Sector Address (SA) in the command to determine which sector will be overlaid.	3	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
IDSFE2_1_1	ASO Secure Silicon Region	The ID/Unique ID/SFDP ASO Entry 2 transaction allows reading Device ID, Unique ID, and SFDP parameters. This entry transaction uses the Sector Address (SA) in the command to determine which sector will be overlaid.	1	Yes	Yes
RDIDSF_1_1		The Read ID/Unique ID/SFDP transaction allows reading the Device IF, Unique ID, and SFDP parameters at the given address and places it on DQ[7:0].	1	Yes	Yes
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	Yes
SSRENT_3_1		The Secure Silicon Region ASO Entry transaction allows accessing the Secure Silicon Region. This entry transaction uses the Sector Address (SA) in the command to determine which sector will be overlaid.	3	Yes	Yes
RD_SSR_1_1		The Read Secure Silicon Region transaction allows reading the Secure Silicon Region data at the given address and places it on DQ[7:0].	1	Yes	Yes
PG_SSR_4_1		The Program Secure Silicon Region Word transaction programs the data word (0's) supplied on DQ[7:0] in the addressed Secure Silicon region.	4	Yes	Yes
LDBSSR_5_1		The Load Secure Silicon Region Buffer transaction loads up to 256/512 bytes of data (0's) supplied on DQ[7:0] in the write buffer.	5	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
PGCSSR_1_1		The Program Secure Silicon Region Buffer Confirm transaction tells the device to program the data loaded into the write buffer into the addressed Secure Silicon region.	1	Yes	Yes
RSWSSR_3_1		The Reset Write to Buffer Abort transaction resets the Write Buffer Abort Status Flag (WRBFAB - STRV[3]) in the Status register.	3	Yes	Yes
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	Yes
ASPENT_3_1	ASO Advanced Sector Protection	The Advanced Sector Protection ASO Entry transaction allows accessing the Advanced Sector Protection configuration register. This entry transaction does not use a sector address from the entry transaction to overlay. The ASP Configuration Register appears at word location 0 in the device address space	3	Yes	Yes
PGOASP_2_1		The Program One-Time-Programmable Advanced Sector Protection Register transaction programs the 16-bit OTP ASP configuration register with the data placed on DQ[7:0].	2	Yes	Yes
RDOASP_1_1		The Read One-Time-Programmable Advanced Sector Protection Register transaction allows reading the contents of the 16-bit OTP ASP configuration register using device address 0 and places it on DQ[7:0].	1	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	Yes
PWDENT_3_1	ASO Password	The Password ASO Entry transaction allows accessing the 64-bit password. This entry transaction does not use a sector address from the entry transaction to overlay. The Password appears at word locations 0 to 3 in the device address space.	3	Yes	Yes
PGNPWD_2_1		The Program Non-Volatile Password transaction programs the 64-bit Password with data placed on DQ[7:0].	2	Yes	Yes
RDNPWD_1_1		The Read Non-Volatile Password transaction allows reading the contents of the 64-bit Password using device address 0 to 3 and places it on DQ[7:0].	1	Yes	Yes
ULNPWD_7_1		The Unlock Non-Volatile Password transaction allows entering the 64-bit Password on DQ[7:0] to unlock the device for access.	7	Yes	Yes
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
PPBENT_3_1	ASO Persistent Protection Bits	The Persistent Protection Bits ASO Entry transaction allows accessing the Persistent Protection bits (PPB) associated with sectors. This entry transaction does not use a sector address from the entry transaction to overlay. The PPB bit for a sector appears in bit 0 of all word locations in the sector.	3	Yes	Yes
PGNPPB_2_1		The Program Non-Volatile Persistent Protection Bits transaction programs the PPB bit corresponding to a sector with data placed on DQ[7:0]. The PPB bit for a sector appears in bit 0 of all word locations in the sector.	2	Yes	Yes
ERNPPB_2_1		The Erase Non-Volatile Persistent Protection Bits transaction erases all the PPB bits.	2	Yes	Yes
RSWPPB_3_1		The Reset Write to Buffer Abort transaction resets the Write Buffer Abort Status Flag (WRBFAB - STRV[3]) in the Status register caused by a PPB program failure.	3	Yes	Yes
RDNPPB_1_1		The Read Non-Volatile Persistent Protection Bits transaction allows reading the PPB bit corresponding to a sector and places it on DQ[7:0]. The PPB bit for a sector appears in bit 0 of all word locations in the sector.	1	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
PRTSTS_2_1		The Sector Protection Status transaction provides the protection status of the addressed sector. Data out during a SA Protection Status Read indicates whether the indicated sector is protected in bits 0–2: Bit 0 – Indicates whether the indicated sector is protected (0 = protected, 1 = unprotected).Bit 1 – Protected using the sector's DYB bit (0 = protected, 1 = unprotected). Bit 2 – Protected using the sector's PPB bit (0 = protected, 1 = unprotected). Bits 3 through 15 are all 1s.	2	Yes	Yes
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	Yes
PPLENT_3_1	ASO PPB Lock	The Persistent Protection Lock ASO Entry transaction allows accessing the global Persistent Protection Lock bit. This entry transaction does not use a sector address from the entry transaction to overlay. The global Persistent Protection Lock bit appears in bit 0 of all word locations in the device.	3	Yes	Yes
CLVPPL_2_1		The Clear Volatile Persistent Protection Lock transaction clears the global Persistent Protection Lock bit.	2	Yes	Yes
RDVPPL_1_1		The Read Volatile Persistent Protection Lock transaction allows reading the global Persistent Protection Lock bit and places it on DQ[7:0]. The PPL bit appears in bit 0 of all word locations in the sector.	1	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	Yes
DYBENT_3_1	ASO Dynamic Protection Bits	The Dynamic Protection Bits ASO Entry transaction allows accessing the Dynamic Protection bits (DYB) associated with sectors. This entry transaction does not use a sector address from the entry transaction to overlay. The DYBB bit for a sector appears in bit 0 of all word locations in the sector.	3	Yes	Yes
STVDYB_2_1		The Set Volatile Dynamic Protection Bit transaction sets the DYB bit corresponding to a sector with data placed on DQ[7:0]. The DYB bit for a sector appears in bit 0 of all word locations in the sector.	2	Yes	Yes
CLVDYB_2_1		The Clear Volatile Dynamic Protection Bit transaction clears the DYB bit corresponding to a sector with data placed on DQ[7:0]. The DYB bit for a sector appears in bit 0 of all word locations in the sector.	2	Yes	Yes
RDVDYB_1_1		The Read Volatile Dynamic Protection Bit transaction allows reading the DYB bit corresponding to a sector and places it on DQ[7:0]. The DYB bit for a sector appears in bit 0 of all word locations in the sector.	1	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
PRTSTS_2_1		The Sector Protection Status transaction provides the protection status of the addressed sector. Data out during a SA Protection Status Read indicates whether the indicated sector is protected in bits 0–2: Bit 0 – Indicates whether the indicated sector is protected (0 = protected, 1 = unprotected).Bit 1 – Protected using the sector's DYB bit (0 = protected, 1 = unprotected).Bit 2 – Protected using the sector's PPB bit (0 = protected, 1 = unprotected).Bits 3 through 15 are all 1s.	2	Yes	Yes
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	Yes
ECCENT_3_1	ASO Error Correction Codes	The Error Correction (ECC) ASO Entry transaction allows accessing the error correction action (ECC status) of any half-page of the Flash Memory Array.	3	Yes	Yes
RDECST_1_1		The Read Error Correction (ECC) Status transaction provides the ECC Status value for the addressed half-page on DQ[7:0]. A single word of status is displayed at any word location within a half-page.	1	Yes	Yes
RDADTL_2_1		The Read Address Trap Register Lower Word transaction provides the lower 16-bits of the error correction action (ECC) related address value stored in the Address trap register (32-bits) on DQ[7:0].	2	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
RDADTU_2_1		The Read Address Trap Register Upper Word transaction provides the upper 16-bits of the error correction action (ECC) related address value stored in the Address trap register (32-bits) on DQ[7:0].	2	Yes	Yes
RDCONT_2_1		The Read ECC Count Value Register transaction provides the ECC count of the number of error correction actions on DQ[7:0].	2	Yes	Yes
CLRECC_1_1		The Clear ECC Error Status Failure Flags transaction resets all failure flags and interrupts being reported.	1	Yes	Yes
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	Yes
ICRCEN_3_1	ASO Interface CRC	The Interface CRC Register ASO Entry transaction allows accessing the contents of the Interface CRC register. Exiting Interface CRC Register ASO clears the Interface CRC register.	3	Yes	No
RDICRC_1_1		The Read Volatile Interface CRC Register transaction provides the contents of the Interface CRC register on DQ[7:0]. Addresses 0x00 and 0x01 define the lower and upper 16-bit Interface CRC register values.	1	Yes	No
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	No

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
DICREN_3_1	ASO Data Integrity CRC	The Data Integrity CRC Register ASO Entry transaction allows accessing the Data Integrity CRC checksum. While Data Integrity CRC calculation is not suspended, Data Integrity CRC ASO overlays the entire Flash memory array. When the CRC calculation is suspended, the flash memory array is visible for reading.	3	Yes	Yes
LDSTAD_1_1		The Load Start Address transaction loads the Data Integrity CRC beginning address location.	1	Yes	Yes
LDENAD_1_1		The Load End Address transaction loads the Data Integrity CRC ending address location.	1	Yes	Yes
SP_DIC_1_1		The Suspend Data Integrity CRC transaction allows the system to interrupt the Data Integrity CRC calculation operation.	1	Yes	Yes
RDCMRY_1_1		The Read Memory Array during Data Integrity CRC suspend transaction allows reading out the memory array data at the given address and places it on DQ[7:0].	1	Yes	Yes
RS_DIC_1_1		The Resume Data Integrity CRC transaction allows the system to resume the suspended Data Integrity CRC calculation operation.	1	Yes	Yes
RDDICL_2_1		The Read Data Integrity CRC Register Lower Word transaction provides the lower 16-bits of the Data Integrity CRC checksum on DQ[7:0].	2	Yes	Yes
RDDICU_2_1		The Read Data Integrity CRC Register Upper Word transaction provides the upper 16-bits of the Data Integrity CRC checksum on DQ[7:0].	2	Yes	Yes

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	Yes
ATBNEN_3_1	ASO AutoBoot	The AutoBoot Non-Volatile Register ASO Entry transaction allows accessing the AutoBoot Register. This entry transaction does not use a sector address from the entry transaction.	3	Yes	No
PGNATB_2_1		The Program Non-Volatile AutoBoot Register transaction programs the 16-bit Non-Volatile AutoBoot register with data placed on DQ[7:0].	2	Yes	No
RDATBN_1_0		The Read Non-Volatile AutoBoot Register transaction allows reading the contents of the 32-bit Non-Volatile AutoBoot register and places it on DQ[7:0]. Addresses 0x00 and 0x01 define the lower and upper 16-bit AutoBoot register values.	1	Yes	No
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	No
SECTEN_3_1	ASO Sector Erase Count	The Sector Erase Count Volatile Register ASO Entry transaction allows accessing the Sector Erase Count Register. This entry transaction does not use a sector address from the entry transaction.	3	Yes	No
LDSRAD_2_1		The Load Sector Address transaction loads the sector address whose erase count is desired.	2	Yes	No

(table continues...)

Table 2 (continued) Command set comparison

Transaction	Description		Cycles	S26HL/HS-T	S26KL/KS-S
RDSECV_1_0	ASO Endurance Flex	The Read Volatile Sector Erase Count Register transaction allows reading the contents of the 16-bit Volatile Sector Erase Count register and places it on DQ[7:0].	1	Yes	No
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	No
ENX_EN_3_1		The Endurance Flex Pointer Selection (Partitions) One-Time-Programmable Register ASO Entry transaction allows accessing the Endurance Flex Pointer registers. This entry transaction does not use a sector address from the entry transaction.	3	Yes	No
PGOENX_2_1		The Program One-Time-Programmable Endurance Flex Registers [4:0] transaction programs the One-Time-Programmable Endurance Flex registers [3:0] with data placed on DQ[7:0]. Addresses 0x00, 0x01, 0x02, 0x03, and 0x04 define the four Endurance Flex register values.	2	Yes	No
RDOENX_1_1		The Read One-Time-Programmable Endurance Flex Registers [4:0] transaction reads the One-Time-Programmable Endurance Flex registers [3:0] and places it on DQ[7:0]. Addresses 0x00, 0x01, 0x02, 0x03, and 0x04 define the four Endurance Flex register values.	1	Yes	No
ASOEXT_1_1		The ASO Exit transaction returns the device to reading memory array data mode when device is in an ASO. If any of the ASO Entry commands were issued, an ASO Exit command must be issued to reset the device into Read mode.	1	Yes	No

4.1 Serial flash discoverable parameters

S26HL/HS-T supports Serial flash discoverable parameters (SFDP) in addition to manufacturer/device identification and Common Flash Interface (CFI) tables as in S26KL/KS-S. SFDP is defined by JEDEC (JEDEC-216B) and consists of a header table, which identifies the SFDP parameters. Table 3 provides the address map overview for both device families.

Table 3 S26HL/HS-T and S26KL/KS-S SFDP, ID, CFI Address map overview

Starting word address	S26HL/HS-T	S26KL/KS-S
(SA) + 0000h to 0000Fh	–	Device ID
(SA) + 0010h to 00079h	–	CFI Data
(SA) + 0000h	SFDP	–
(SA) + 0800h	Device ID	–

4.2 Unique identification

S26HL/HS-T provides a 64-bit unique number for each device. S26KL/KS-S does not support unique identification. Table 4 shows the address map for unique identification for S26HL/HS-T.

Table 4 S26HL/S-T Unique ID address map overview

Starting word address	S26HL/HS-T	S26KL/KS-S
(SA) + 0200h	Unique ID	–

4.3 Status and Configuration Registers

The working state of S26HL/HS-T and S26KL/KS-S devices is set by internal configuration registers. Status registers, on the other hand, provide the device's status during embedded algorithmic operations. Table 5 summarizes the supported registers for each device.

Table 5 Status and Configuration Register set comparison

Register type	S26HL/HS-T	S26KL/KS-S	Identical?
Status Register	Yes	Yes	Yes
Configuration Register 1	Yes	Yes	No
Configuration Register 2	Yes	–	N/A

See the device datasheets to know about the type and functionality of each configuration/status bit.

4.4 ECC Status Registers

S26HL/HS-T and S26KL/KS-S devices both have ECC-protected memory cores and provide registers for ECC status reporting. Table 6 summarizes the supported registers for each device.

Table 6 ECC Register set comparison

Register type	S26HL/HS-T	S26KL/KS-S	Identical?
ECC Status	Yes	Yes	No
Address Trap Register	Yes	Yes	Yes

(table continues...)

Table 6 (continued) ECC Register set comparison

Register type	S26HL/HS-T	S26KL/KS-S	Identical?
ECC Count Register	Yes	Yes	Yes

See the device datasheets to know about the type and functionality of each register bit.

4.5 Data Protection Registers

S26HL/HS-T and S26KL/KS-S devices both support Advanced Sector Protection (ASP) data protection against erase/program operations. Table 7 summarizes the supported registers for each device.

Table 7 ASP Register set comparison

Register type	S26HL/HS-T	S26KL/KS-S	Identical?
Advanced Sector Protection Register	Yes	Yes	No
Password Register	Yes	Yes	Yes
PPB Lock Register	Yes	Yes	Yes
PPB Access Register	Yes	Yes	Yes
DYB Access Register	Yes	Yes	Yes

See the device datasheets to know about the type and functionality of each register bit.

4.6 AutoBoot Registers

S26HL/HS-T supports the AutoBoot feature where the host master controller executes boot code immediately after the end of reset (POR, hardware reset, software reset, default recovery), without sending a read instruction. S26KL/KS-S does not support AutoBoot. Table 8 summarizes the supported registers for each device.

Table 8 AutoBoot Register set comparison

Register type	S26HL/HS-T	S26KL/KS-S	Identical?
AutoBoot Register	Yes	–	N/A

See the device datasheets to know about the type and functionality of each register bit.

4.7 Sector Erase Count Registers

S26HL/HS-T supports the Sector Erase Count (SEC) feature, which provides the capability to read the number of times each sector has been erased. The SEC command outputs the number of successful erase cycles for the addressed sector. S26KL/KS-S does not support SEC. Table 9 summarizes the supported registers for each device.

Table 9 SEC Register set comparison

Register type	S26HL/HS-T	S26KL/KS-S	Identical?
Sector Erase Count Register	Yes	–	N/A

See the device datasheets to know about the type and functionality of each register bit.

4.8 Interface CRC Registers

S26HL/HS-T supports the interface CRC (ICRC) feature where the device calculates a fixed-length binary sequence, known as the CRC checksum, for each block of interface data and puts it in the BCRC register for interface integrity. S26KL/KS-S does not support BCRC. Table 10 summarizes the supported registers for each device.

Table 10 BCRC Register set comparison

Register type	S26HL/HS-T	S26KL/KS-S	Identical?
Interface CRC Register	Yes	–	N/A

See the device datasheets to know about the type and functionality of each register bit.

4.9 Endurance flex architecture (wear-leveling) Registers

S26HL/HS-T supports the endurance flex architecture feature where data endurance is improved through wear leveling. Wear leveling spreads the program/erase cycles of the device evenly across all the sectors that are part of the wear-leveling pool in the device. S26KL/KS-S does not support endurance flex architecture. Table 11 summarizes the supported registers for each device.

Table 11 Endurance Flex Register set comparison

Register type	S26HL/HS-T	S26KL/KS-S	Identical?
Endurance Flex Register 0	Yes	–	N/A
Endurance Flex Register 1	Yes	–	N/A
Endurance Flex Register 2	Yes	–	N/A
Endurance Flex Register 3	Yes	–	N/A
Endurance Flex Register 4	Yes	–	N/A

See the device datasheets to know about the type and functionality of each register bit.

5 Hardware comparison

5.1 Hardware reset

The behavior of the hardware reset pin (RESET#) in S26HL/S-T is different from S26KL/KS-S. In S26HL/HS-T, RESET#, once initiated, a hardware reset has the same sequence as a power-on reset (POR). In S26KL/KS-S, the RESET# behavior is a subset of the POR sequence – in other words, all blocks are not initialized.

5.2 DC parameters

Table 12 compares DC parameters for S26HL/HS-T and S26KL/KS-S. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all parameter differences for any potential impacts.

Table 12 DC parameters comparison

		S26HL/HS-T			S26KL/KS-S			
Param	**Description/Test conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
V_{IH}	Input voltage HIGH threshold, GPIO, CMOS Configuration	V_{CCQ} × 0.65	–	V_{CCQ} × 1.15	V_{CCQ} × 0.7	–	V_{CCQ} + 0.4	V
V_{IL}	Input voltage LOW threshold, GPIO, CMOS Configuration	V_{CCQ} × _ 0.15	–	V_{CCQ} × 0.35	-0.50	–	V_{CCQ} × 0.3	V
V_{OH}	Output High Voltage Conditions: @ -0.1 mA	V_{CCQ} – 0.2	–		V_{CCQ} - 0.2	–	–	V
V_{OL}	Output Low Voltage Conditions: @ 0.1 mA	–	–	0.20	–	–	V_{CCQ} * 0.15	V
I_{LI}	Input Leakage Current Conditions: V_{CCQ}=MAX, V_{IN}=V_{IH} or V_{SS}, CS#=V_{IH} ,@ 125C	–	–	±4	–	–	–	µA
I_{LO}	Output Leakage Current Conditions: V_{CC}Q=MAX, VIN=VIH or VSS, CS#=V_{IH}, @ 125C	–	–	±4	–	–	–	µA
I_{CC1}	V_{CC} Active Read Current (core current only, I/O switching current is not included)CS# = V_{IL}, DDR @200 MHz, V_{CC} = 1.95 V	–	156	173	–	130	180	mA
I_{CC1}	V_{CC} Active Read Current (core current only, I/O switching current is not included)CS# = V_{IL}, DDR @166 MHz, V_{CC} = 3.6 V	–	75	130	–	80	100	mA

(table continues...)

Table 12 (continued) DC parameters comparison

		S26HL/HS-T			S26KL/KS-S			
Param	**Description/Test conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
I_{IO1}	V_{CCQ} Active Read Current of I/OsCS# = V_{IL}, @200 MHz, V_{CCQ} = 1.95 V, C_{LOAD} = 15 pF	–	–	–	–	80	100	mA
I_{IO1}	V_{CCQ} Active Read Current of I/OsCS# = V_{IL}, @200 MHz, V_{CCQ} = 3.6V, C_{LOAD} = 15 pF	–	–	–	–	80	100	mA
$I_{CC\ 2}$	Active Page Program CurrentConditions: CS#=V_{IH}, V_{CC} = max	–	50	58	–	60	100	mA
I_{CC4}	Active Sector Erase (256 KB)Conditions: CS#=V_{IH}, V_{CC} = max	–	50	55	–	60	100	mA
I_{SB1}	Standby Current (–40°C to +85°C)Conditions: CS#=V_{IH}, RESET#=V_{IH}, All I/Os=V_{IH} or V_{SS}	–	14/11	113	–	25	100	µA
I_{SB2}	Standby Current –40°C to +105°C)Conditions: CS#=V_{IH}, RESET#=V_{IH}, All I/Os=V_{IH} or V_{SS}	–	14 / 11	188	–	25	300	µA
I_{SB3}	Standby Current –40°C to +125°C)Conditions: CS#=V_{IH}, RESET#=V_{IH}, All I/Os=V_{IH} or V_{SS}	–	14/11	340	–	25	300	µA
I_{DPD1}	Deep Power Down Current (–40°C to +85°C)Conditions: CS#=V_{IH}, CS#=V_{IH}, RESET#=V_{IH}, All I/Os=V_{IH} or V_{SS}	–	2.2/1.3	18	–	30	50	µA
I_{DPD2}	Deep Power Down Current (–40°C to +105°C)Conditions: CS#=V_{IH}, CS#=V_{IH}, RESET#=V_{IH}, All I/Os=V_{IH} or V_{SS}	–	2.2/1.3	18	–	95	150	µA

(table continues...)

Table 12 (continued) DC parameters comparison

		S26HL/HS-T			S26KL/KS-S			
Param	**Description/Test conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
I_{DPD3}	Deep Power Down Current (–40°C to +125°C)Conditions: CS#=V_{IH}, CS#=V_{IH}, RESET#=V_{IH}, All I/Os=V_{IH} or V_{SS}	–	2.2/1.3	31	–	150	250	µA
I_{RESET}	Reset Current Conditions: CS#=VIH, All I/Os=V_{IH} or V_{SS}	–	–	80	–	10	20	mA
$I_{CLKSTOP1}$	Active Clock Stop Mode V_{CC} = 1.95 V Conditions: CS#=VIH, IO3/ RESET#=V_{IH}, All I/Os=V_{IH} or V_{SS}	–	–	–	–	6	12	mA
$I_{CLKSTOP2}$	Active Clock Stop Mode V_{CC} = 3.6 V Conditions: CS#=VIH, IO3/ RESET#=V_{IH}, All I/Os=V_{IH} or V_{SS}	–	–	–	–	6	12	mA

5.3 Pin capacitance values

Table 13 compares pin capacitance values for S26HL/HS-T and S26KL/KS-S. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impacts.

Table 13 Pin capacitance values comparison

		S26HL/HS-T			S26KL/KS-S			
CAP parameters	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
CI	Input capacitance (CK, CK#, CS#, PSC, PSC#)	–	3	7.5	3.5	–	4.5	pF
CID	Delta input capacitance (CK, CK#, CS#, PSC, PSC#)	–	–	–	–	–	0.25	pF
CO	Output capacitance (RWDS)	–	6.5	7.5	5	–	6	pF
CIO	I/O pin capacitance (DQx)	–	6.5	7.5	5	–	6	pF
CIOD	I/O pin capacitance Delta (DQx)	–	–	–	–	–	0.8	pF
COP	INT#, RSTO# pin capacitance	–	6.5	7.5	5	–	6	pF
CIP	WP#, RESET# pin capacitance	–	6.5	7.5	6.5	–	9	pF

5.4 AC parameters

Table 14 compares AC parameters for S26HL/HS-T and S26KL/KS-S. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impacts.

Table 14 AC parameter comparison

		S26HL/HS-T			S26KL/KS-S			
AC parameters	**Description/Test conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
f_{SCK}	SPI clock frequency	0	–	166/200	-	–	166	MHz
P_{SCK}	SCK period	$1/f_{SCK}$	–	–	6	–	–	ns
t_{CSHI}	Chip Select HIGH between transactions	7.5	–	–	6	–	–	ns
t_{CSS}	CS# Active Setup Time (w.r.t SCK)	4	–	–	3	–	–	ns
t_{DSV}	Data Strobe Valid	–	–	5	-	–	12	ns
t_{IS} (t_{SU})	Input Data Setup Time (w.r.t SCK)	0.6/0.5	–	–	0.6	–	–	ns
t_{IH} (t_{HD})	Input Data Hold Time (w.r.t SCK)	0.6/0.5	–	–	0.6	–	–	ns
t_{ACC}	Read Initial Access Time	–	–		-	–	96	ns
t_{DQLZ}	Clock to DQs Low Z	0	–		0	–	–	ns
t_{CKD} (t_V)	CK transition to DQ Valid	2	–	7.25/5.45	1	–	5.5	ns
t_{CKDI}	CK transition to DQ Invalid		–	7.5/6	0	–	4.6	ns
t_{CKDS}	CK transition to RWDS valid	2	–	7.25/5.45	1	–	5.5	ns
t_{DSS}	RWDS transition to DQ Valid	–0.4	–	0.4	-0.45	–	0.45	ns
t_{DSH}	RWDS transition to DQ Invalid	–0.4	–	0.4	-0.45	–	0.45	ns
$t_{CSH\ 0}$	Chip Select Hold After CK Falling Edge	4	–	–	0	–	–	ns
t_{DSZ}	Chip Select Inactive to RWDS High-Z	–	–	7.5/6	–	–	6	ns
t_{OZ}	Chip Select Inactive to DQ High-Z	–	–	7.5/6	–	–	6	ns

5.5 Embedded algorithms performance

Table 15 compares embedded algorithm parameters for S26HL/HS-T and S26KL/KS-S. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impacts.

Table 15 Embedded algorithm performance parameter comparison

		S26HL/HS-T			S26KL/KS-S			
Embedded parameters	**Description/Test conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
t_W	Non-volatile Register Write Time	–	44	357.5	–	–	–	ms
$t_{PP}1$	Page Programming Time (256 bytes)	–	480	1700	–	–	–	µs
$t_{PP}2$	Page Programming Time (512 bytes)	–	570	1700	–	475	2000	µs
$t_{SE}1$	Sector Erase Time (4K bytes)	–	42	335	–	240	725	ms
$t_{SE}2$	Sector Erase Time (256K bytes) Endurance flex architecture enabled	–	773	5869	–	930	2900	ms
$t_{BE}1$	Bulk Erase Time (512 Mbit)	–	201	696	–	220	462	s
$t_{EES}1$	Evaluate Erase Status Time (4-KB Sector)	–	45	51	–	70	100	µs
$t_{EES}2$	Evaluate Erase Status Time (256-KB Sector)	–	45	56	–	70	100	µs
t_{DIS_SETUP}	ECRC Calculation Setup Time	–	17	–	–	10	–	µs
t_{SEC}	Sector Erase Count Time	–	55	63	–	–	–	µs
t_{ESL}	Erase Suspend/Resume	–	–		–	–	50	µs
t_{PSL}	Erase Suspend/Resume	–	–		–	–	50	µs
t_{CSL}	Data Integrity CRC Suspend/Resume	–	–		–	–	50	µs
t_{PSWD}	Setting the PPB Lock bit after the valid 64-bit password is given to the device	80	100	120	80	100	120	µs

6 Conclusion

Migration from S26KL/KS-S to S26HL/HS-T is straightforward and requires minimal accommodation to either system software or hardware. Moreover, once accommodations are made, if required, S26HL/HS-T SEMPER™ flash can enable use of higher-density devices with greater performance in existing systems.

References

[1] Infineon Technologies AG: *[512 Mbit (64 Mbyte)/256 Mbit (32 Mbyte)/128 Mbit (16 Mbyte), 1.8V/3.0V HYPERBUS™ family]*; available online

[2] Infineon Technologies AG: *[512-MB (64-MB), 1-GB (128-MB), HS-T (1.8-V), HL-T (3.0-V) SEMPER™ flash with HYPERBUS™ interface]*

Revision history

Document version	Date of release	Description of changes
**	2018-05-02	New Application Note
*A	2019-12-11	Updated Table 12, Table 13, and Table 14
*B	2021-03-16	Updated to Infineon template
*C	2022-05-06	Updated feature set, command set, hardware for S26HL-T
*D	2022-08-04	Updated the title
*E	2026-08-31	Template update; no content update.

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