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Spec No: 001-13842

Spec Title: RECOMMENDED USAGE OF BYTE ENABLES IN STANDBY MODE FOR 90 NM X16 MOBL(R) SRAM DEVICES - AN13842

Sunset Owner: Mamta Jatolia (MEMJ)

Replaced by: NONE

COMMENT: The issue described in the rest of this document has been fixed, and devices with this fix are in production. The table below shows the date code marking on the devices that contain the fix. The first two digits represent the year, and the next two represent the workweek. For example, 0826 refers to the twenty sixth workweek of year 2008. Devices with workweek on or after 0826 (like 0832, 0906 etc) contain the fix.
To know if you are affected by this issue, please feel free to create a Technical Support case on the website (www.cypress.com/support)

Device	**Fixed device from date code starting**
2 Mbit (CY62136EV30, CY62137EV30)	0826
2 Mbit (CY62136FV30, CY62137FV30, CY62137FV18)	1301
4 Mbit (CY62146E, CY62146EV30, CY62147EV30, CY62147EV18)	0826
8 Mbit (CY62157E, CY62157EV30, CY62157EV18)	0826
16 Mbit (CY62167E18, CY62167EV30, CY62167E)	0826

AN13842

Recommended Usage of Byte Enables in Standby Mode for 90 nm x16 MoBL® SRAM Devices

Author: Anuj Chakrapani
Associated Project: No
Associated Part Family: CY62136EV30, CY62137EV30, CY62136FV30, CY62137FV30, CY62137FV18, CY62146E, CY62146EV30, CY62147EV30, CY62147EV18, CY62157E, CY62157EV30, CY62157EV18, CY62167E18, CY62167EV30, CY62167E
Software Version: None
Related Application Notes: None

AN13842 provides recommendations for the usage of Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) in select Cypress MoBL® SRAMs. However, the issue responsible for the recommendations provided in this document has been fixed. Hence, Cypress devices with newer date code do not require you to implement these timing recommendations in your design. The nature of this fix is transparent to a user. If you were unaffected by this issue earlier, the fix will not affect you either. This fix does not affect any of the datasheet parameters or functionality of the devices.

If you have any queries about the content in this document, please contact us at www.cypress.com/support.

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Introduction

Cypress's 90-nm MoBL SRAM devices have best-in-class standby power. They are targeted for use in low power battery operated applications.

The following sections in this application note discuss the recommended usage of Byte enable pins ($\overline{BHE}$ and $\overline{BLE}$) in standby mode for these devices.

Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) Usage in Standby Mode

Cypress's 90 nm MoBL SRAM devices have been designed to meet low standby currents. The devices have a power management block that helps to keep the memory core at a low voltage. This ensures that the chip draws very minimal current in the standby mode (that is, when the chip is disabled). In standby mode, in the event of an external trigger condition, the internal power management blocks adjust themselves to ensure that the SRAM devices do not draw higher power. See the following section for this external trigger condition.

External Input Trigger Condition

In a long chip disable cycle controlled by chip enable ($\overline{CE}$) that is, over a time period T ≥ 1 µs, as shown in Figure 1, if both byte enables ($\overline{BHE}$ and $\overline{BLE}$) continuously toggle, then data is not guaranteed for the first subsequent active read/write operation. However, for the successive read/write operations after this first active cycle, data is guaranteed.

A suggested workaround is to keep the byte enables $\overline{BHE}$ and $\overline{BLE}$ fixed at CMOS levels (either below V_{IL} or above V_{IH} but strictly not toggling) in disable cycle as shown in Figure 2. In other words, if $\overline{BHE}$ and $\overline{BLE}$ transition with $\overline{CE}$ while entering into and exiting from the disable cycle, there is no effect on the power management block and data is guaranteed for the first read/write operation also.

Note that, if only $\overline{OE}$ and $\overline{WE}$ toggle in the standby mode, and $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ are fixed, this issue will not occur.

Figure 1. Read/Write Operation with $\overline{BHE}/\overline{BLE}$ Toggling During the Chip Disable Cycle

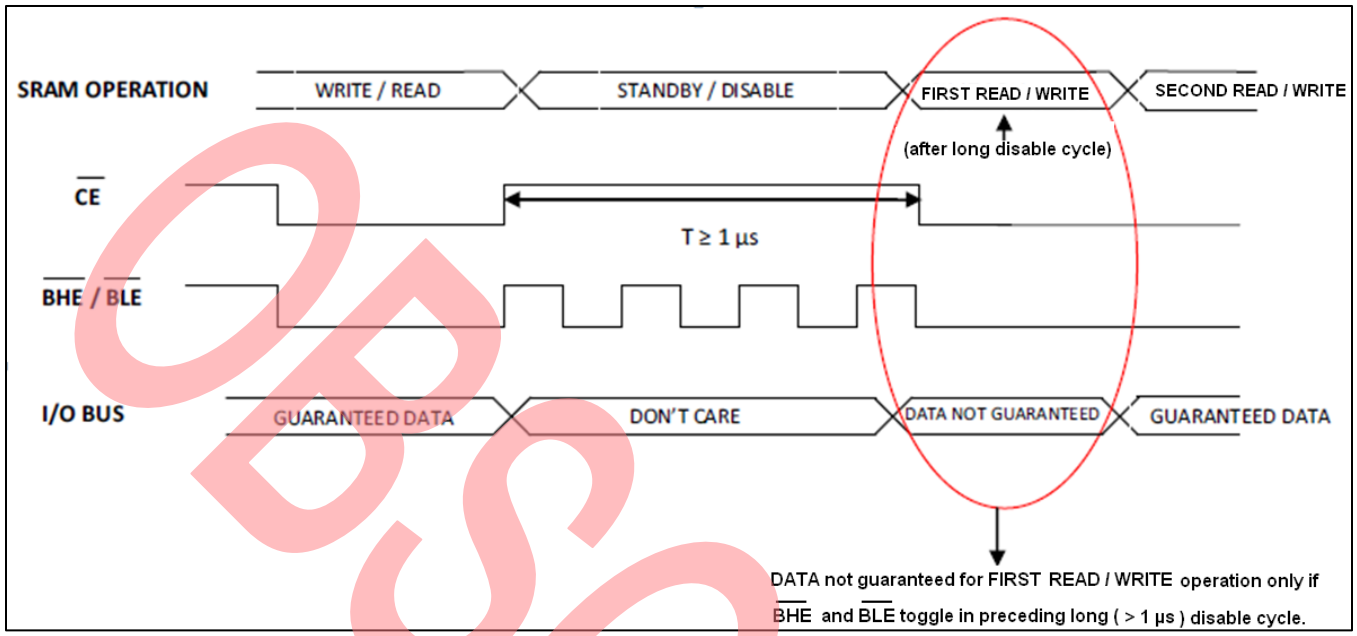
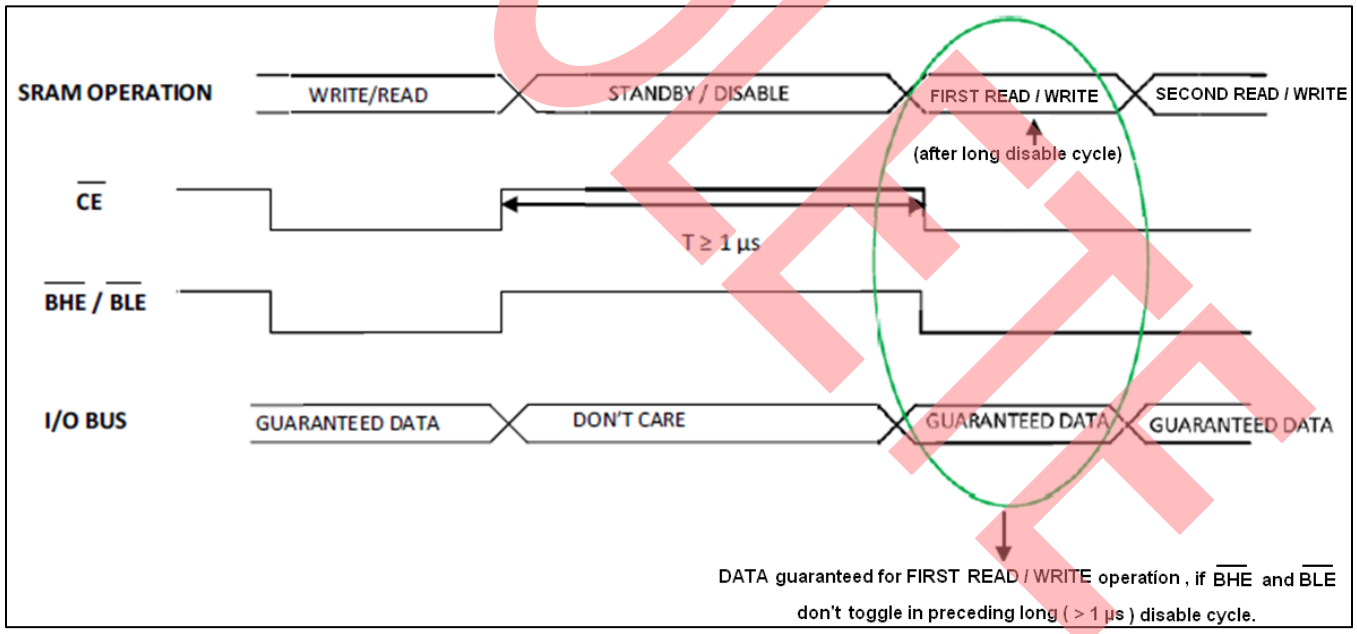


Figure 2. Read/Write Operation with $\overline{BHE}/\overline{BLE}$ Fixed at CMOS Levels (either below V_{IL} or above V_{IH}) During Chip Disable Cycle



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Summary

It is recommended to keep $\overline{BHE}$ and $\overline{BLE}$ signals fixed at any of the CMOS logic levels (instead of toggling), if the chip disable cycle is controlled by $\overline{CE}$. If you cannot implement this recommendation, contact Cypress Technical Support for the availability of alternate parts.

Document History

Document Title: Recommended Usage of Byte Enables in Standby Mode for 90 nm x16 MoBL® SRAM Devices - AN13842

Document Number: 001-13842

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	873086	NXR	See ECN	New application note
*A	1822034	NXR	12/12/07	Updated the template and information in the application note
*B	2604652	VKN	11/12/08	Added 2-Mbit parts CY62136EV30, CY62137EV30 and 16-Mbit parts CY62167E18, CY62167EV30, CY62167E on page 1
*C	3161419	PRAS	02/03/2011	Hyperlinks provided to all the parts specified in the Abstract section.
*D	3347247	AJU	08/17/2011	Changed Title Updated Abstract Removed section: BHE, BLE Levels in standby mode Updated section: Byte enables (BHE and BLE) usage in standby mode
*E	3516704	TAVA	02/03/2012	Updated template Modified title and minor text edits.
*F	3551222	TAVA	03/20/2012	Updated Figure 1 and Figure 2, and updated content to acknowledge the modification in the figures. Minor text edits.
*G	3941647	NILE	03/22/2013	Major rewrite of Abstract.
*H	4054168	AJU	07/24/2013	Removed instance of CY62126EV30 Obsolete application note

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