Getting started with 2ED2410-EM

Application note

About this document

Scope and purpose

This application note explains how to design-in Infineon EiceDRIVER™ APD 2ED2410-EM.

The set-up of external components based on practical considerations using datasheet [1] parameters is described, and tips on how to use this unique gate driver flexibility are provided.

Intended audience

This document is intended for all electrical and electronic engineers who need to replace relays and fuses effectively and simply so that they make a reliable and self-protected solid-state switch, based on a MOSFET and a shunt resistor.

***Note**:* *Values shown in this application note are measured under lab conditions and will vary for different cooling conditions and setups.*

***Note**:* *In this document, [PRQ-xxx] numbers refer to 2ED2410-EM datasheet [1] parameters.*

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1 Basic functions and mandatory external components

This chapter describes the minimum and most necessary components to operate the 2ED2410-EM.

2ED2410-EM is a high-side gate driver and therefore needs a power supply that elevates voltage above battery voltage to drive the MOSFETs. A *boost converter (BC)* supply is chosen, to have improved efficiency compared to a *charge pump (CP)*, and therefore, pulls less current from the car's battery. The diode (*D*) and switching element (*K1*) are implemented inside the chip and the inductor (*L*), output capacitor (C_{BC}) and resistor for current peak sense (R_{RS}) must be added externally.

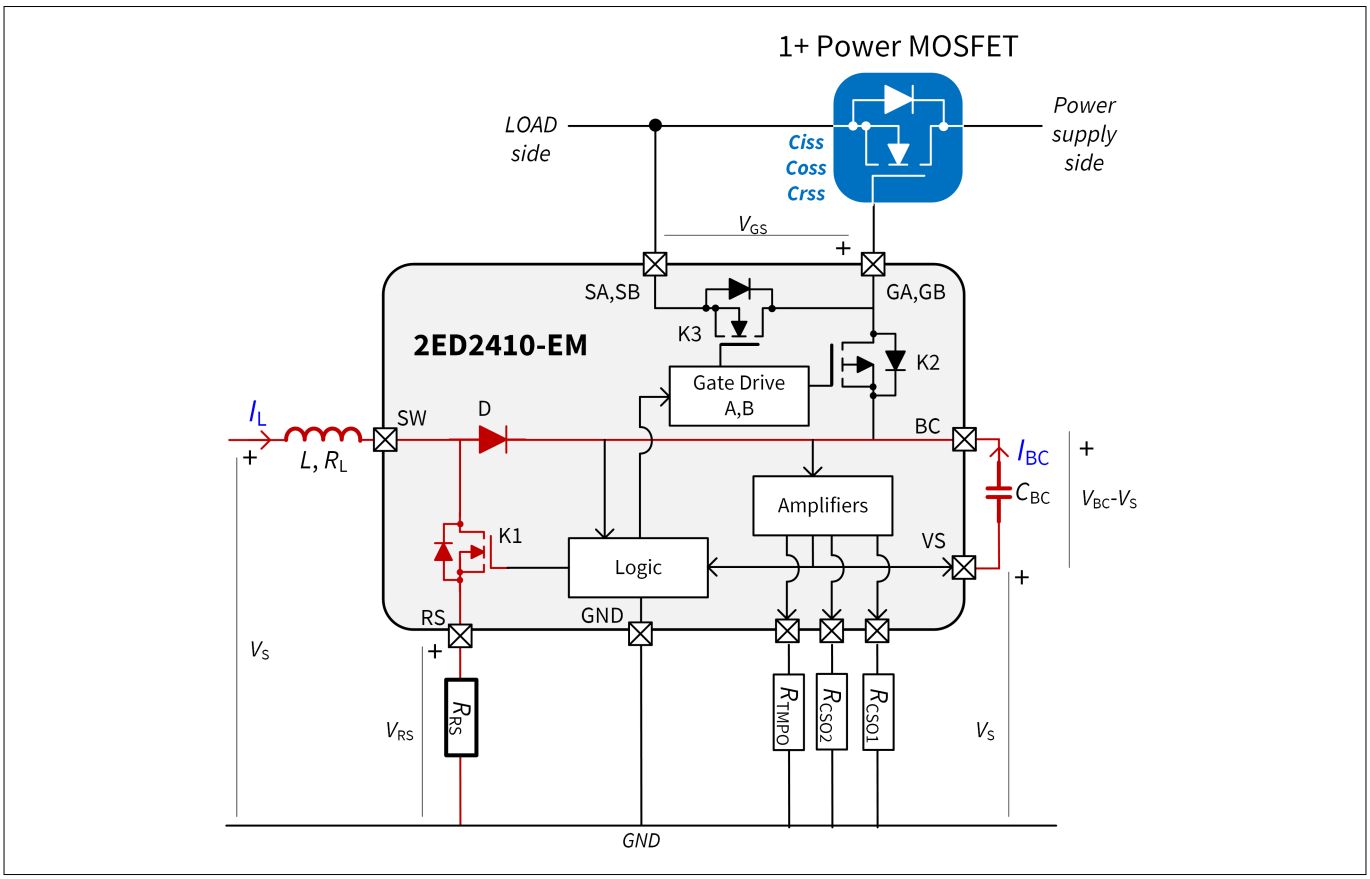


Figure 1 2ED2410-EM Boost converter supply concept with currents and voltages definition

1.1 Sizing C_{BC}

The C_{BC} capacitor is the output capacitor of the *BC*, normally used to filter the output on regular BCs.

Here, it is also used as a charge buffer for the external MOSFETs parasitic C_{iss} at turn-on. During turn-on, the charges are transferred from C_{BC} to the external MOSFET C_{iss}. This allows 2ED2410-EM to drive many MOSFETs in parallel, up to 100 nF, equivalent to C_{GS} per gate driver output. Therefore, it has to be ensured that during turn-on, the voltage of the C_{BC} capacitor does not drop below the boost converter "gate *undervoltage lockout (UVLO)*" limit. The range between "gate UVLO" [PRQ-140] and regulating output voltage of the BC $V_{BC(TH)}$ [PRQ-139] above battery voltage, is called $V_{BC(RG)}$ [PRQ-141].

Therefore, the MOSFET reference and the total number of MOSFETs driven by the driver must be known at this stage.

Assuming the charge is conserved between tank capacitor C_{BC} and the sum of the MOSFET C_{iss}, $C_{iss(TOT)}$, using Q=C*V,

$$C_{BC} \times \Delta V_{BC} = C_{iss(TOT)} \times V_{BC(TH)} \quad (1)$$

Given the minimum ΔV_{BC} we have to sustain with C_{BC}, is $V_{BC(RG)MIN}$ (Minimum of $V_{BC(RG)}$);

$$C_{BC(MIN)} = \frac{C_{iss(TOT)} \times V_{BC(TH)MAX}}{V_{BC(RG)MIN}} \quad (2)$$

As an example, using eight IAUT300N08S5N012 (four in parallel on each gate output), the computed $C_{BC(MIN)}$ is given by:

$$C_{BC(MIN)} = \frac{8 \times 1.625 \times 10^{-8} \times 14}{1.9} = 0.96 \quad \mu F \quad (3)$$

Therefore, a suitable capacitor for this application could be a 1 µF capacitor. Considering a 30% shift of capacitor value over lifetime as well as 20% ceramic capacitor accuracy, here it is necessary to use a 2.2 µF capacitor for C_{BC}.

The automated calculation can be found in the excel workbook, tab “Boost converter cap CBC”[2].

A regular turn-on is shown in Figure 2. When the MOSFETs are turned-on, the charges are taken from C_{BC}, and the BC pumps again to compensate the charged transferred to the MOSFET, hence the activation of RS (green). The activation is monitored by DG0 pin (pink) in ON mode.

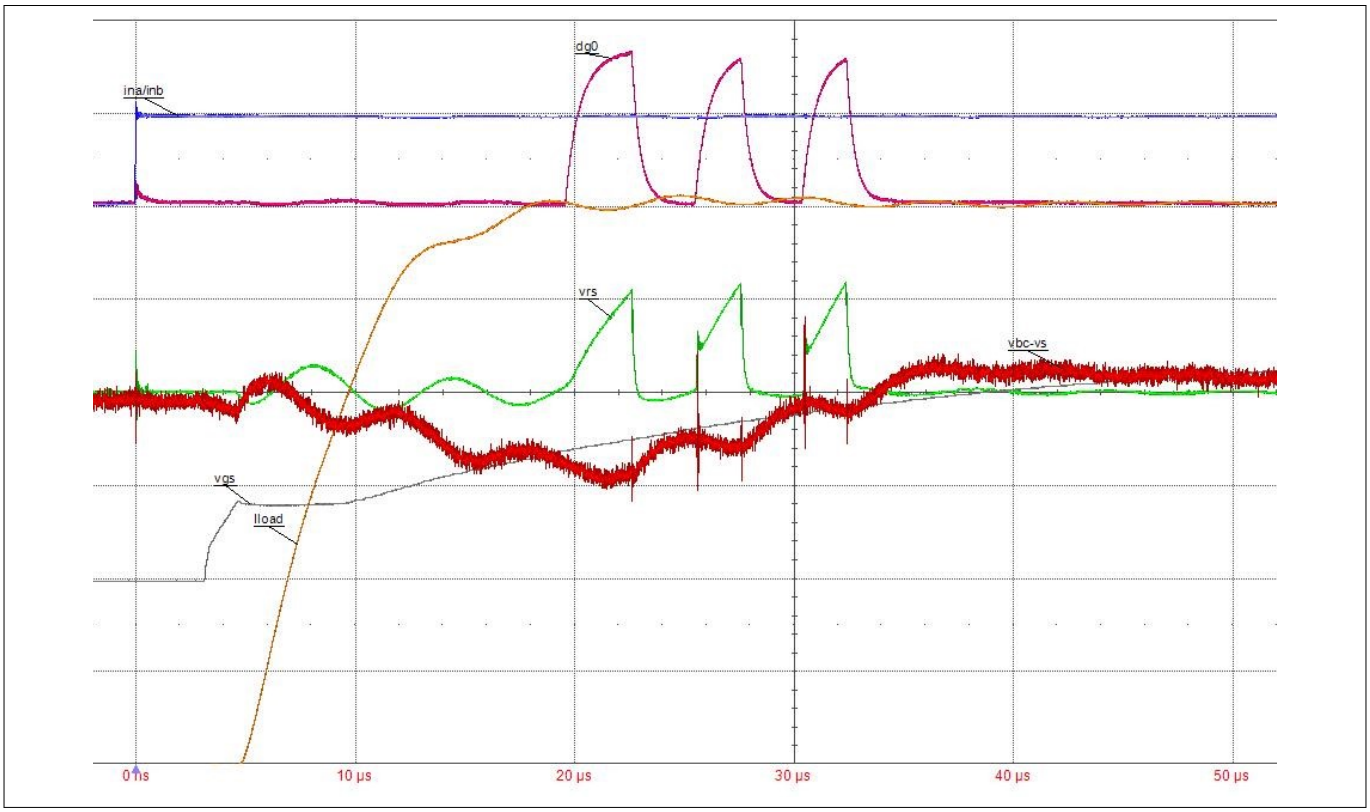


Figure 2 **Switching waveform from IDLE to ON mode [blue: INx; green: V_{RS}; red: V_{BC}-VS (AC mode) (BC output); pink: DG0; grey: gate-source on MOSFET; orange: LOAD current]**

1.2 Sizing *L* and R_{RS}

The *BC* is designed for very small duty cycles (<1%), open loop, and current peak control operation in discontinuous conduction mode.

Therefore, the most important parameter to observe is the $I_L = I_{peak}$ limitation in the switching element, K1 (refer to Figure 1), defined by the maximum of parameter I_{SW} [PRQ-16]. This condition $I_L < I_{SW}$ must be true at all temperatures over the application voltage range.

The current in the inductor is limited by the $V_{RS(TH)}$ *comparator (COMP)*, inside the driver (see Figure 3), which monitors the voltage across R_{RS}. Due to the delay in the loop ($t_{D\ (OFF)K1}$ [PRQ-155]), the inductor current exceeds the threshold set by: $V_{RS(TH)}$ [PRQ-147].

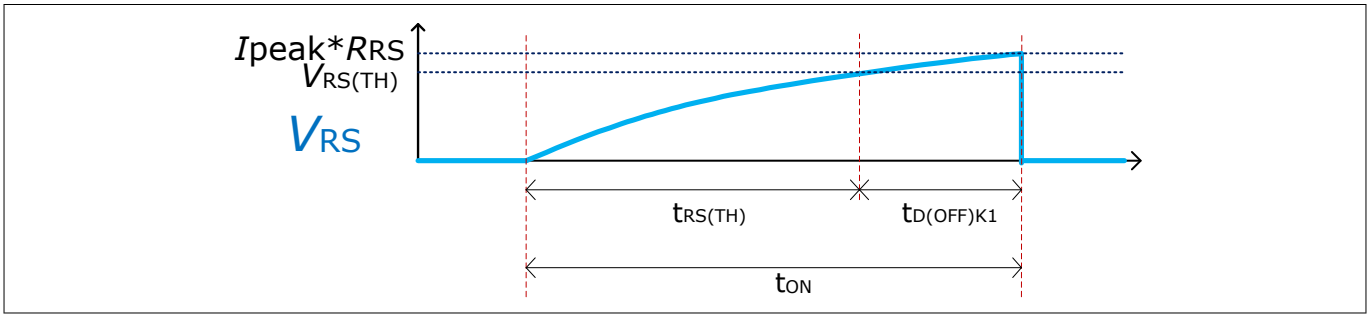


Figure 3 Switching waveform of boost converter, V_{RS} voltage

The current waveform in the inductor is not linear, but exponential because the sum of the resistor of K1, of the parasitic inductor of L (R_L) and R_{RS} are not negligible in the K1 short activation time frame.

Therefore, the time to reach $t_{RS(TH)}$ is computed by:

$$t_{RS(TH)} = -\frac{L}{R_{DS(ON)K1} + R_{RS} + R_L} \times \ln\left(1 - V_{RS(TH)} \times \frac{R_{DS(ON)K1} + R_{RS} + R_L}{R_{RS} \times V_S}\right) \quad (4)$$

Referring to Figure 3:

$$t_{ON} = t_{RS(TH)} + t_{D(OFF)K1} \quad (5)$$

Ideally, R_{RS} should be as low as possible. A high R_{RS} resistor would lower output current capability. In addition, the BC operating frequency could be in the audible range. By design of the I_{peak} detection loop, a minimum is given in the datasheet [1] $R_{RS(MIN)}$= 10 Ω [PRQ-138]. Additionally, the computed power must be sustained by the resistor R_{RS} across the whole application range, meaning I_{peak} must be computed for 18 V if the operating range expected in the application is 8 V to 18 V, for example.

$$P_{RRS} \geq I_{peak(V_{S(MAX)})}^2 \times R_{RS} \quad (6)$$

Therefore, from Equation (4), having chosen the R_{RS} value, the I_{peak} can be computed with the available inductor. As there are three unknowns in the equation, there is no simple way to compute the minimum inductor that can be used. It has to be ensured that the I_{peak} parameter is not violated over the application V_S range given that the characteristics of the inductor are used.

Therefore, the I_{peak} current can be solved by:

$$I_{peak} = \frac{V_S}{R_{DS(ON)K1} + R_{RS} + R_L} \times \left(1 - e^{-t_{ON} \times \frac{R_{DS(ON)K1} + R_{RS} + R_L}{L}}\right) \quad (7)$$

The automated calculation can be found in the workbook [2], tab “L, RS and driver consumption”.

Typically, an inductor between 100 µH and 470 µH can be selected with $R_{RS(MIN)}$. Where a 100 µH can be cost-optimized compared to a 470 µH inductor, the latter improves the efficiency and therefore will optimize the

current consumption from the battery. Also, choosing an inductor with a small parasitic series resistance R_L, will increase the BC efficiency and reduce the current drawn from the battery. See Quiescent current example for detailed quiescent current calculations.

To sum up, the choice of the inductor is driven by the I_{peak} and its optimization by three parameters:

1. The parasitic resistance of the coil
2. Current consumption of the driver in the application
3. Application target cost

1.3 Computing boost converter frequency

The gate outputs are supplied directly out of the gate driver through the PMOS of a push-pull (PMOS K2, see Figure 1). Therefore, in on-mode, the output of the *BC* is directly connected to the MOSFET gate through K2. Consequently, monitoring the boost frequency monitors the health of the gate source junction. Any leakage or short connection in the power MOSFET can be detected by a much higher frequency in the BC operation compared to normal.

The activation frequency depends on the BC current I_{BC}. The current seen by the BC is given in the datasheet [1]. Depending on the mode, the driver is in $I_{BC(IDLE)}$, $I_{BC(ON)}$, and $I_{BC(SAFESTATE)}$; which are PRQ-144, PRQ-145, and PRQ-146 respectively.

Assuming no leakage losses in C_{BC} capacitor, the charges going out of C_{BC} with an I_{BC} current over the period T of the BC is equivalent to the charges received from the inductor over that same period of time. Therefore, assuming the number of charges stays the same in and out C_{BC}, the time and current to transfer from L to C_{BC}, using Q=I*t, T can be computed easily:

$$T = \frac{t_{transfert} \times \frac{I_{peak}}{2}}{I_{BC}} \tag{8}$$

With

$$t_{transfert} = L \times \frac{I_{peak}}{\left(V_{BC(TH)} + V_{FBC}\right)} \tag{9}$$

equation (9) uses $V = L \times \frac{di}{dt}$ approximation, where V_{FBC} is the integrated BC diode (PRQ-148) and adds up to the BC output voltage.

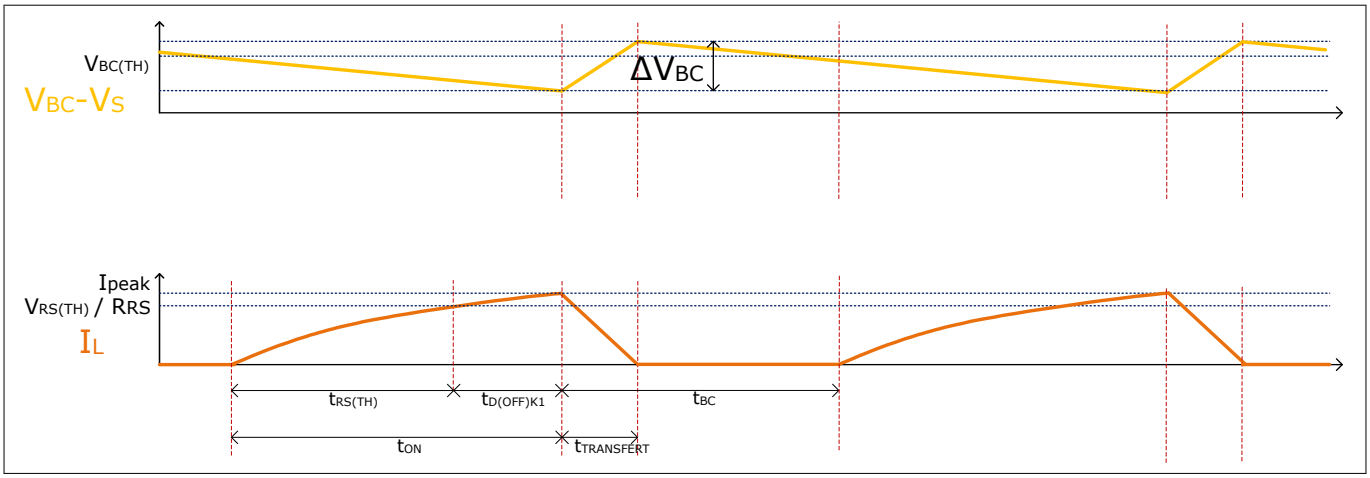


Figure 4 Boost converter theoretical waveform in discontinuous conduction mode (not to scale)

Note that I_{BC} varies with application temperature and therefore boost frequency varies with temperature.

The DG0 frequency can be simply monitored on pin DG0 in ON mode.

The automated calculations for expected boost converter frequency can be found in the excel workbook [2], tab “L, RS and driver consumption”.

1.4 Sizing R_{GATE} for gate-source leakage detection of MOSFET

In power distribution applications, power availability is a critical topic. The 2ED2410-EM driver connects the gate of an external MOSFET to the *BC* output, and therefore if a gate-source degradation occurs in one MOSFET, it could trigger gate *UVLO* protection. However, it also gives the opportunity to identify such a failure by sizing R_{GATE} properly without turning OFF the switch.

R_{GATE} can be sized so it limits the current to the maximum BC output current. As a result, the BC frequency will operate with greater frequency and can be easily monitored on pin DG0 in ON mode.

Since the BC frequency can be monitored by a *microcontroller*, it allows the car central computer unit to make power management decisions in case of a gate-source short detection on one MOSFET, such as turn-off of some non-essential load to reduce power losses through the remaining MOSFET.

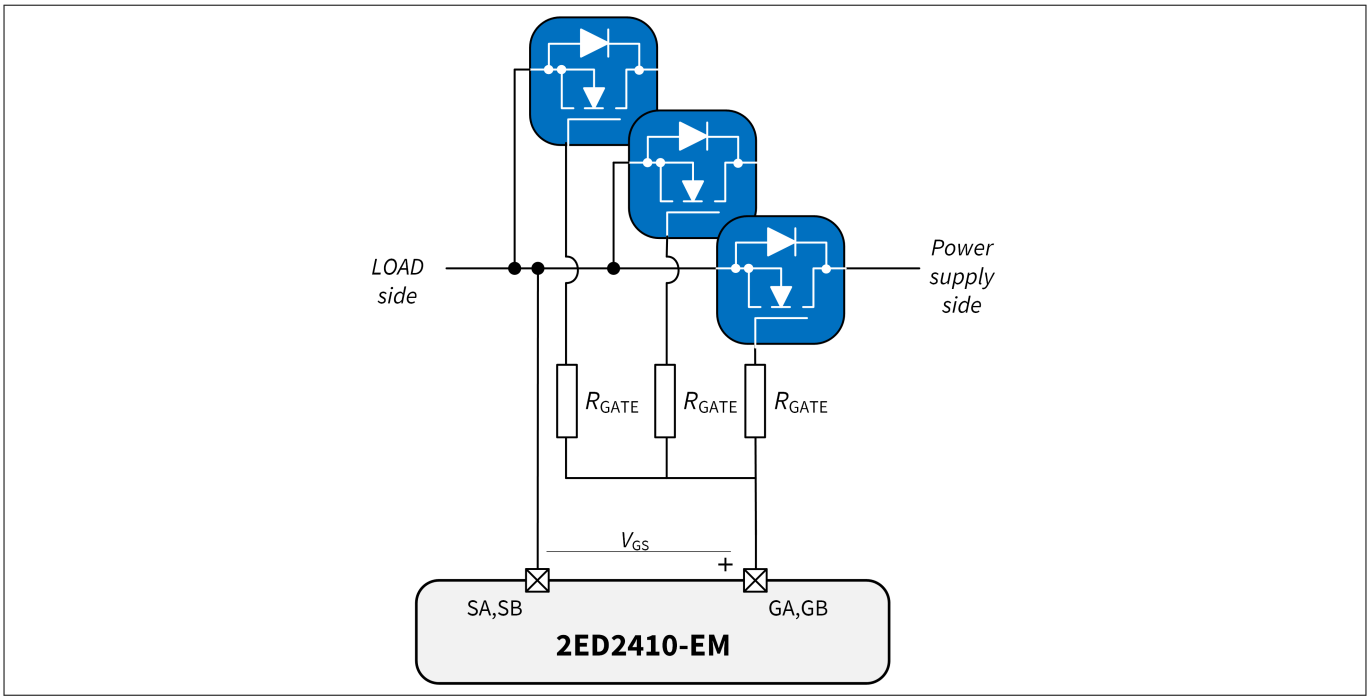


Figure 5 Schematic of principle to identify R_{GATE} in the application

The maximum current which can be delivered by the BC is computed by:

$$I_{BC(MAX),\,disc.} = \frac{\Delta I_{peak} \times t_{transfert}}{2 \times \left(t_{ON(K1)} + t_{BC}\right)} \tag{10}$$

This gives a minimum value for R_{GATE} according to:

$$R_{GATE(MIN)} = \frac{V_{BC(TH)}}{I_{BC(MAX)}} \tag{11}$$

The automated calculation can be found in the workbook [2], cell 51, tab “L, RS and driver consumption”.

***Note**: The minimum/maximum R_{GATE} is not discussed here. Of course, R_{GATE} values down to a few ohms can be used, especially for increased switch-off speed. Fast-off circuitry could be used between the gate driver and the MOSFET.*

1.4.1 Example in application

The figure below shows an example R_{GATE} designed to sustain gate-source short and shows the effects on the gate driver signals. It uses a 12 V demo board with ES samples.

It is clear that the *BC* frequency is increased in case of gate-source short and proper R_{GATE} value. As a result, the driver does not enter SAFESTATE but keeps the switch operating.

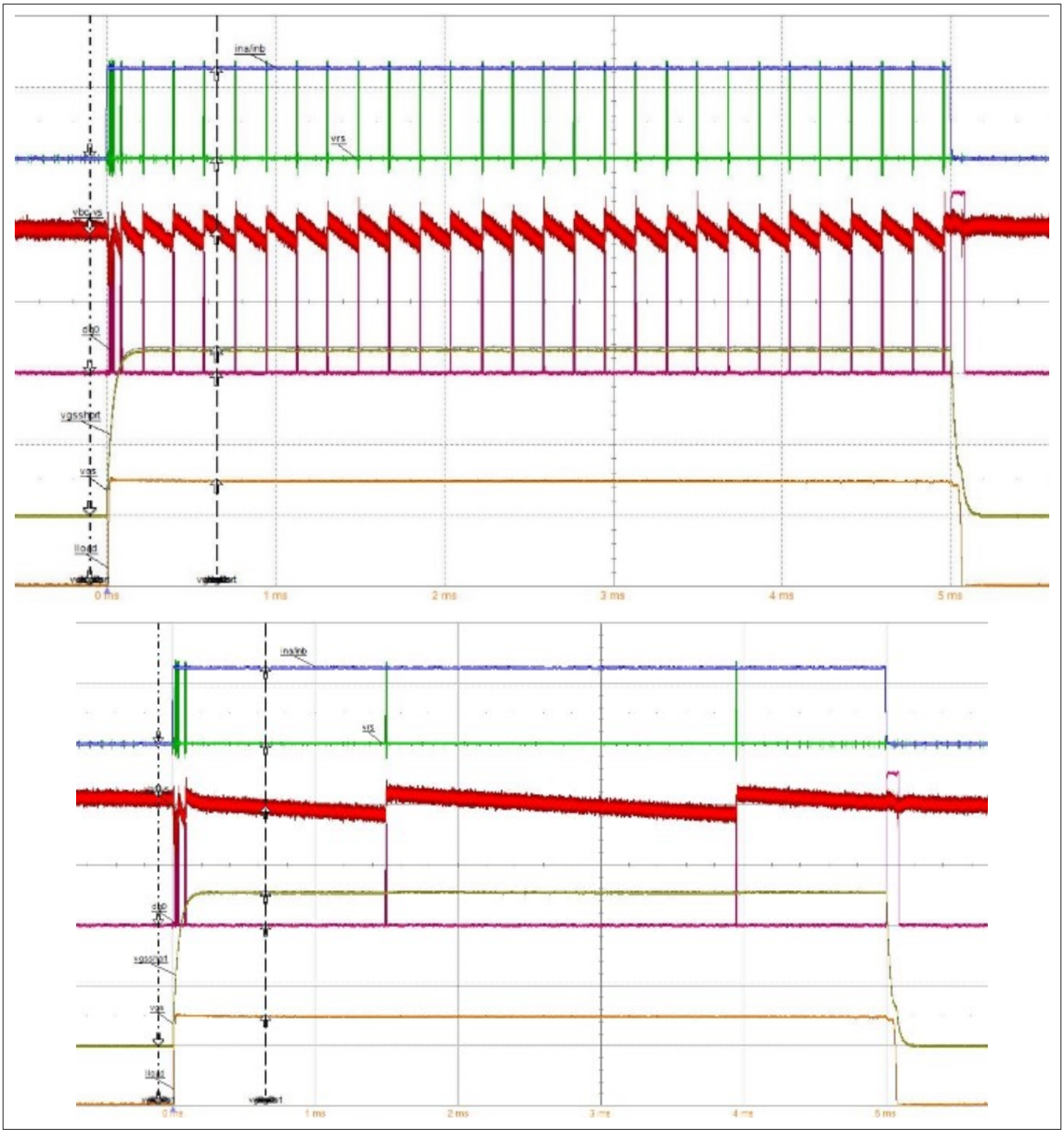


Figure 6 **R_{GATE} to prevent UVLO when gate-source short: with and without failure *[blue: INx; green: V_{RS}; red: V_{BC}-VS (boost converter output); pink: DG0; yellow: gate-source on MOSFET; orange: LOAD current]***

Top figure: With a shorted gate and adapted resistor so that gate *UVLO* is avoided and the switch is maintained ON.

Bottom figure: With no shorted gate, normal BC activity can be monitored out of the DG0 pin in on-mode.

1.5 Reverse battery behavior

This chapter describes the behavior of the driver when reverse battery is applied. Two cases are examined, common drain and common source MOSFET configuration.

***Note**: For a third case, single high-side MOSFET control, there is no protection: no turn-on mechanism of the MOSFET in reverse battery is implemented. Therefore, if reverse battery occurs in this configuration, MOSFET destruction may occur because of power dissipated with the inverse current in the MOSFET body diode.*

1.5.1 Common drain in reverse battery

The following figure describes the current leaking through the driver, in reverse battery at - 36 V, in common drain configuration. Refer to the diodes block diagram, see Chapter 1 in the datasheet [1].

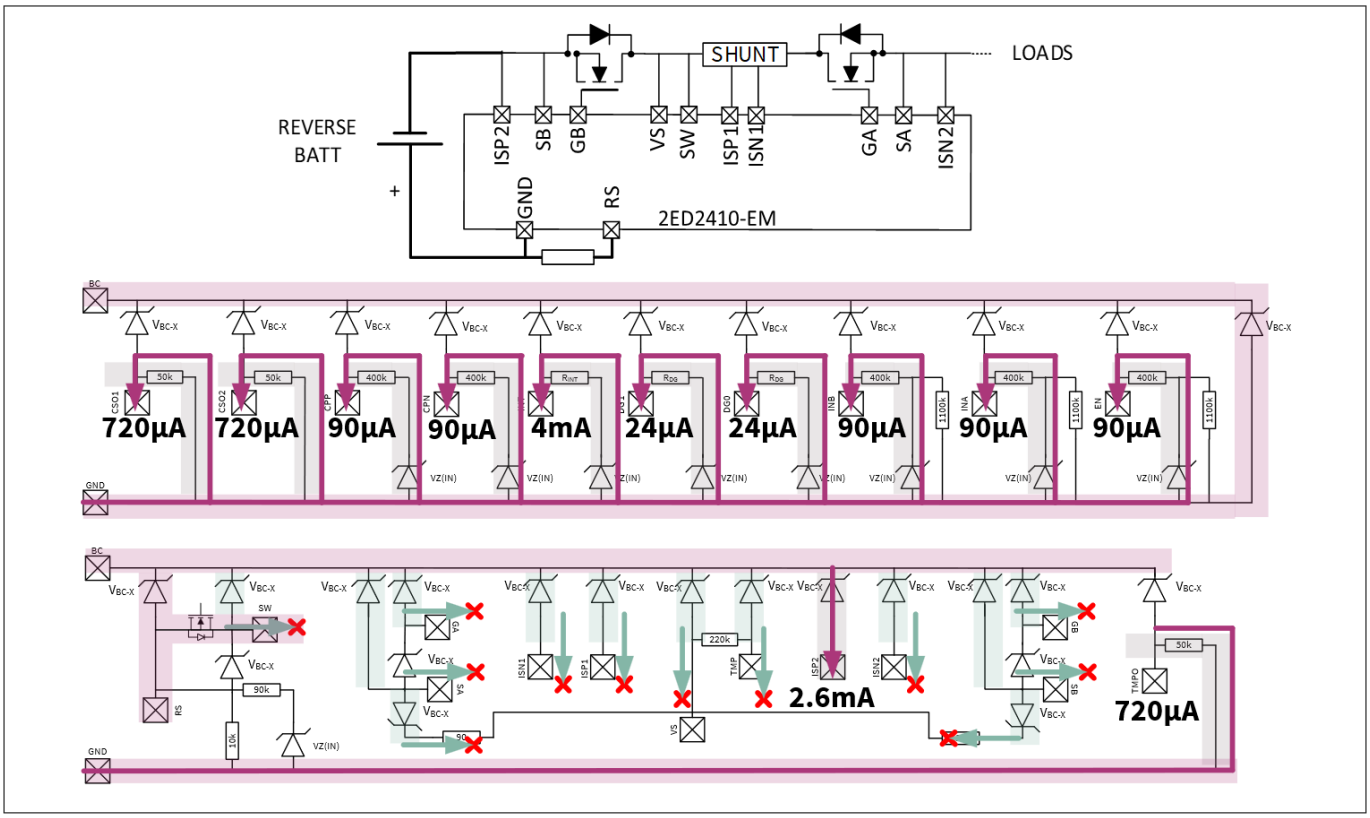


Figure 7 2ED2410-EM diodes diagram with typical leakages at -36 V in a common drain configuration

Due to the common drain structure, there is no current flowing back from load to battery. A 2-minute test was conducted with a reverse battery at -58 V, as can be seen in the figure below.

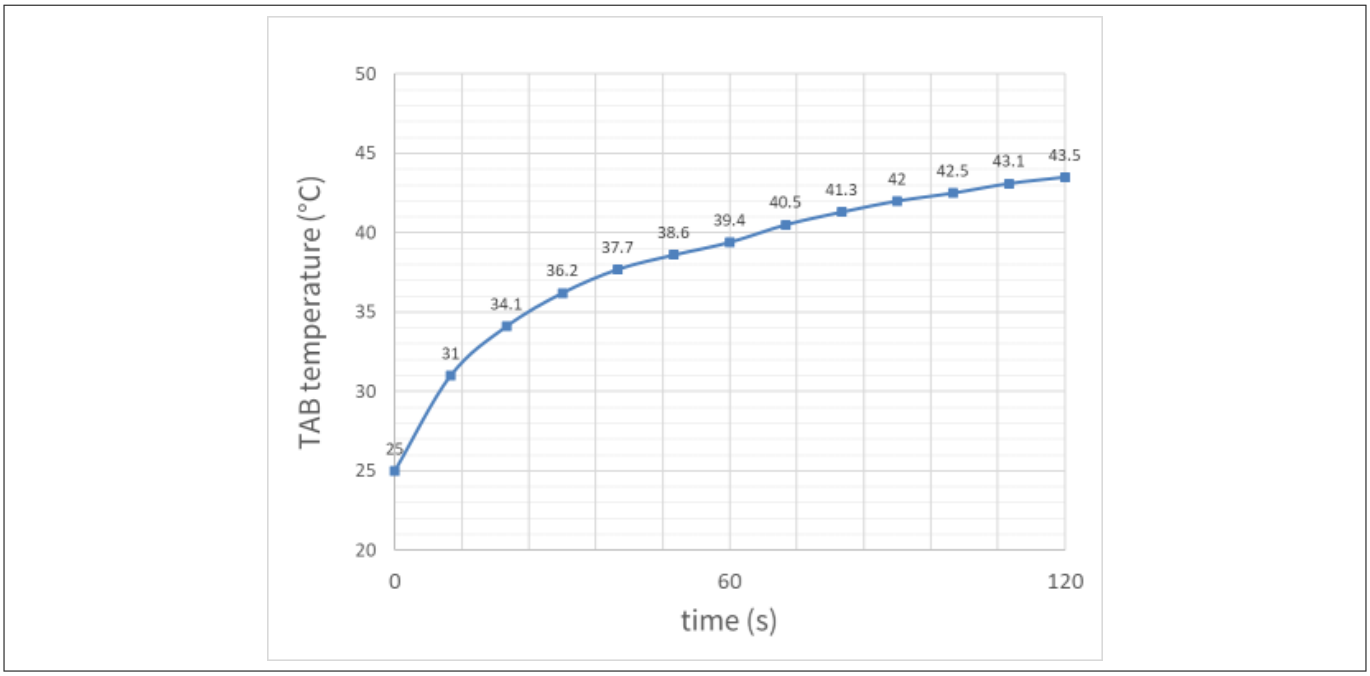


Figure 8 Driver TAB temperature under -58 V reverse battery

1.5.2 Common source in reverse battery

The following figure describes the current leaking through the driver, in reverse battery at -36 V, in common source configuration. Refer to the diodes block diagram, see Chapter 1 in the datasheet [1].

Due to the common source structure, current flows back from GND to battery mainly through RS to SW, the current being limited only by R_{RS} resistor. As a result, K1 MOSFET is likely to be destroyed because of the power dissipated in its body diode.

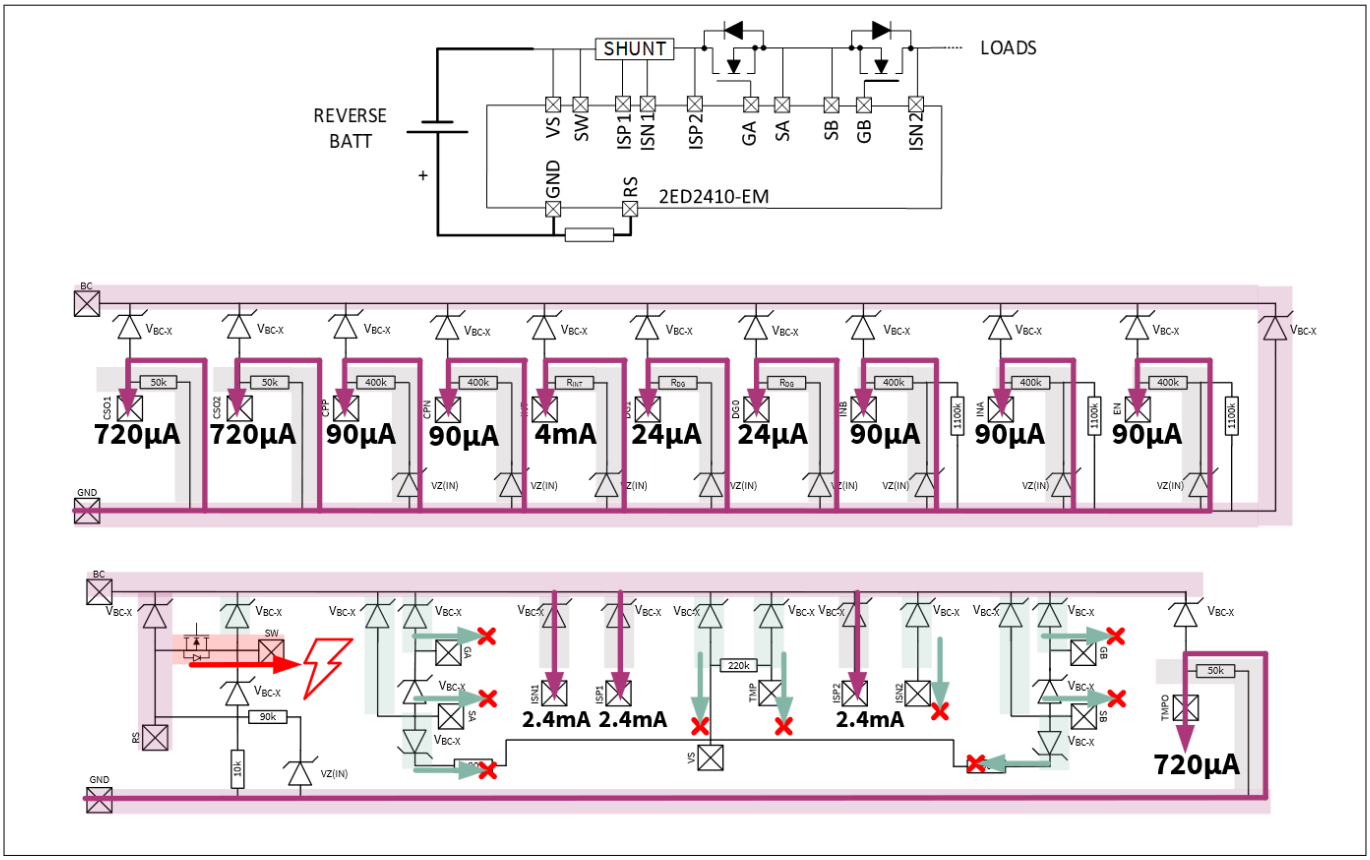


Figure 9 **2ED2410-EM diodes diagram with typical leakages at -36 V in a common drain configuration**

A diode must be used on SW to prevent inverse current during reverse battery.

This diode needs to have a sufficient rating to handle 200 mA, as per the 2ED2410-EM driver in the datasheet [1], PRQ-16. Ideally, the voltage drop across this diode is as small as possible, for example, a 0.3 V Schottky diode. The breakdown should be able to handle the expected worst case of reverse battery voltage where 100 V is recommended.

***Note**: The diode on VS reduces short-circuit performance in case of terminal short-circuit, for example VS<3 V.*

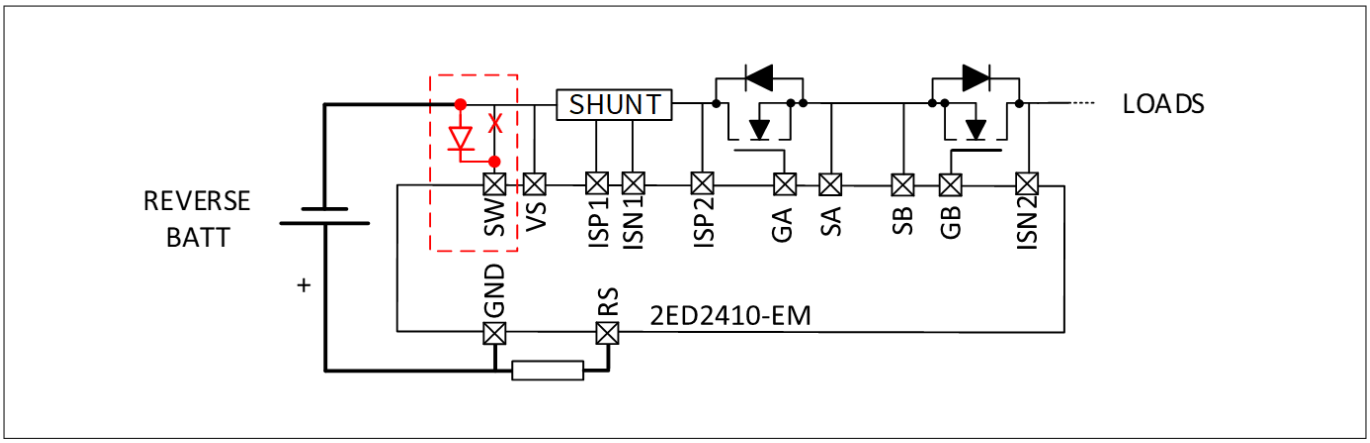


Figure 10 **Handling reverse battery and bi-directional switch with common source configuration**

***Note**: This protection for common source in reverse battery is also valid for single high-side MOSFETs to protect the driver, even though the external MOSFET would not be protected.*

2 What to do with non-used pins?

2ED2410-EM has several features and possibilities. After setting up the basics for driver operation, all functions may not be needed. Therefore, the non-used features can be disabled to save some current consumption or simplify routing on *printed circuit board (PCB)*. Disabling the non-used feature in the correct manner ensures correct driver operation. The table below shows how to connect the pins in order to disable the corresponding features.

Table 1

Pin #	Pin name	Pin type	How to connect a pin to disable the corresponding function
1	CSO1	I/O	GND (FLOAT can trigger random latch on CSO1 internal comparator)
2	CSO2	O	GND
3	CPP	I	GND (FLOAT can trigger random latch CPP)
4	CPN	I	EN (VS induces 'large' current consumption. GND can trigger random latch)
5	INT	O	FLOAT
6	DG1	O	FLOAT
7	DG0	O	FLOAT
8	INB	I	GND (FLOAT potential IBC increase, DPI sensitivity increased if SB GB floating, no IDLE mode)
9	INA	I	GND (FLOAT potential IBC increase, DPI sensitivity increased if SA GA floating, no IDLE mode)
10	EN	I	5 V (@GND driver will always remain in SLEEP mode. EN can also be connected to VS with 100 k+diode so driver is by default in IDLE mode as long as a power supply is connected > V_{zener}+V_{rev_diode} is present on VS pin, diode: cathode on VS.)
11	GND	I/O	GND (never leave open: can randomly activate boost converter, IC destruction)
12	RS	O	FLOAT (when using an external supply directly on BC, RS connection to GND could cause IC destruction)
13	SW	I	FLOAT (in case of boost supply converter disconnection and driver external supply directly on BC)
14	SA	O	FLOAT (if GA not used)
15	GA	I/O	FLOAT
16	ISN1	I	GND/VS
17	ISP1	I	VS/GND
18	VS	I/O	VS (FLOAT: BC is not regulated, external MOSFET gate destruction expected)
19	TMP	I	FLOAT
20	ISP2	I	GND/VS
21	ISN2	I	VS/GND
22	GB	I/O	FLOAT

(table continues...)

Table 1 (continued)

Pin #	Pin name	Pin type	How to connect a pin to disable the corresponding function
23	SB	O	FLOAT (if GB not used)
24	TMPO	O	FLOAT or GND
TAB	BC	O	Boost capacitor C_{BC} or external supply (see datasheet for V_{BC}-V_S functional range [PRQ-339]).

3 Enhanced functions and optional external components

***Attention**: The electrical diagrams in this chapter are circuit propositions that need optimization and verification by the customer in the real application. The objective is to show the possibilities offered by the 2ED2410-EM driver. Other circuits may achieve the same goals.*

3.1 Capacitive load pre-charge strategies

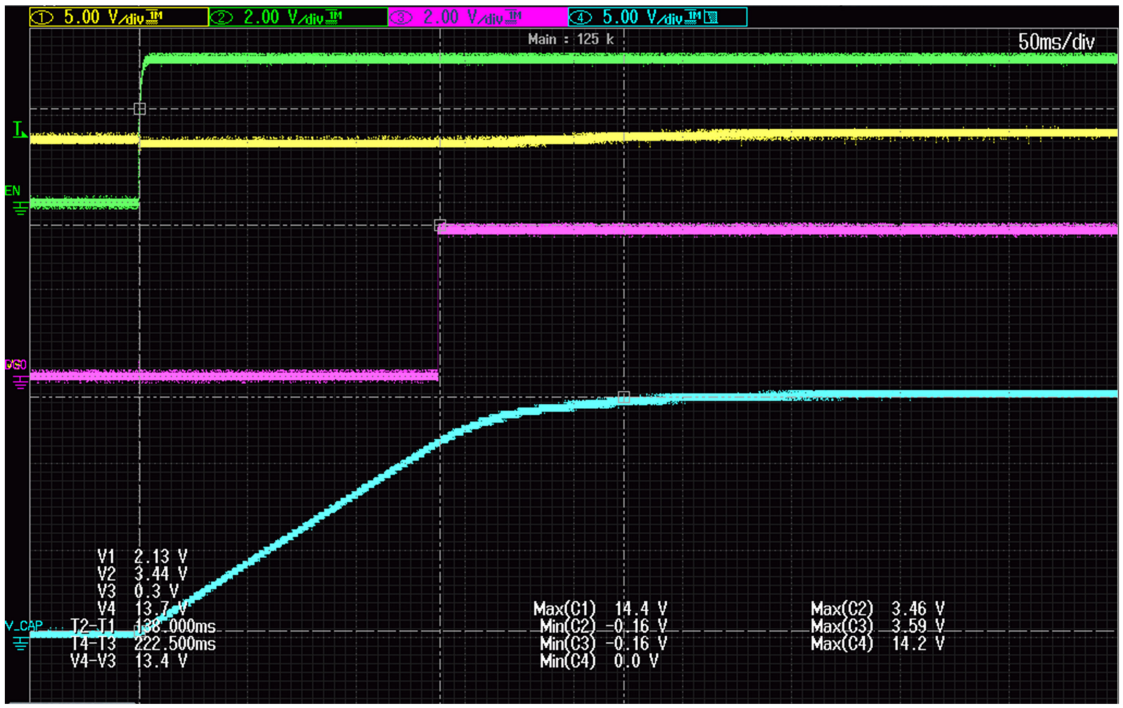
In this paragraph, simple circuits and their control options are discussed. The goal is to enable pre-charging board net circuit capacitances while making the best out of the 2ED2410-EM driver. The ability to pre-charge is mandatory in primary power distribution.

A 2ED2410-EM driver uses a boost converter as a supply and can be seen in Basic functions and mandatory external components. Therefore, this supply can be reused with a level shifter to drive a bypass circuit, including a current-limiter power-resistor, so that capacitances will be charged with a limited current. In this way 2ED2410-EM protections will not be triggered due to the current inrush at turn-on.

Several options are proposed for operating the pre-charge circuit and described in the example of power supply protection switch (PSP).

3.1.1 Internal low bypass current source (I_{SOURCE} feature)

The simplest option is to use the internal precharge current source of the 2ED2410 that does not require any external components. In IDLE mode, the driver typically delivers 15 mA per channel to pre-charge capacitive loads via the Sx pins. In this mode, it is possible to monitor the pre-charge status with DG0 and DG1 respectively for SA and SB. DGx is high when V_{SX} is within $V_{DS\_DIAG(TH)}$ range from VS voltage, meaning that the bypass-current is deactivated (see Chapter 6 and 7 in the datasheet [1]).



Channels	Signal name	Cal/Div	Channels	Signal name	Cal/Div
1	VS	5 V/div	3	DG0	2 V/div
2	EN	2 V/div	4	V_cap	5 V/div
			Time		50 ms/div

Figure 11 Low bypass current pre-charge waveform (C = 220 µF, V_{BAT} = 14 V)

With 1x15 mA, the time to charge the capacitor to V_{BAT} level is 222 ms. This timing can be reduced by two with 2x15 mA (2 source pins connected).

3.1.2 External pre-charge circuitry

An external path, in parallel with the power MOSFETs, allows for a fast pre-charge of capacitive loads. It can be implemented with a MOSFET and series power resistor limiting the pre-charge current (see Figure 12). The activation of the pre-charge is achieved in the following ways:

1. A *general purpose input output (GPIO)* from the controller drives the pre-charge on demand. This method is implemented in the evaluation board family EB 2ED2410 Z8F80306082
2. Tying the pre-charge circuit to EN pin As soon as the driver enters IDLE mode, pre-charge will be enabled as well. It has the advantage of saving one GPIO. In IDLE mode, it is possible to monitor the pre-charge status with DG0 or DG1
3. The driver is set to ON mode. It also saves one GPIO compared to option 1. It has the advantage of setting MOSFET B ON, so that there is no power dissipation in the body diode of MOSFET B compared to option 2. Additionally, protections from the driver are operational (including I-t wire protection) and measurements such as current sense can be used to check the pre-charge operation

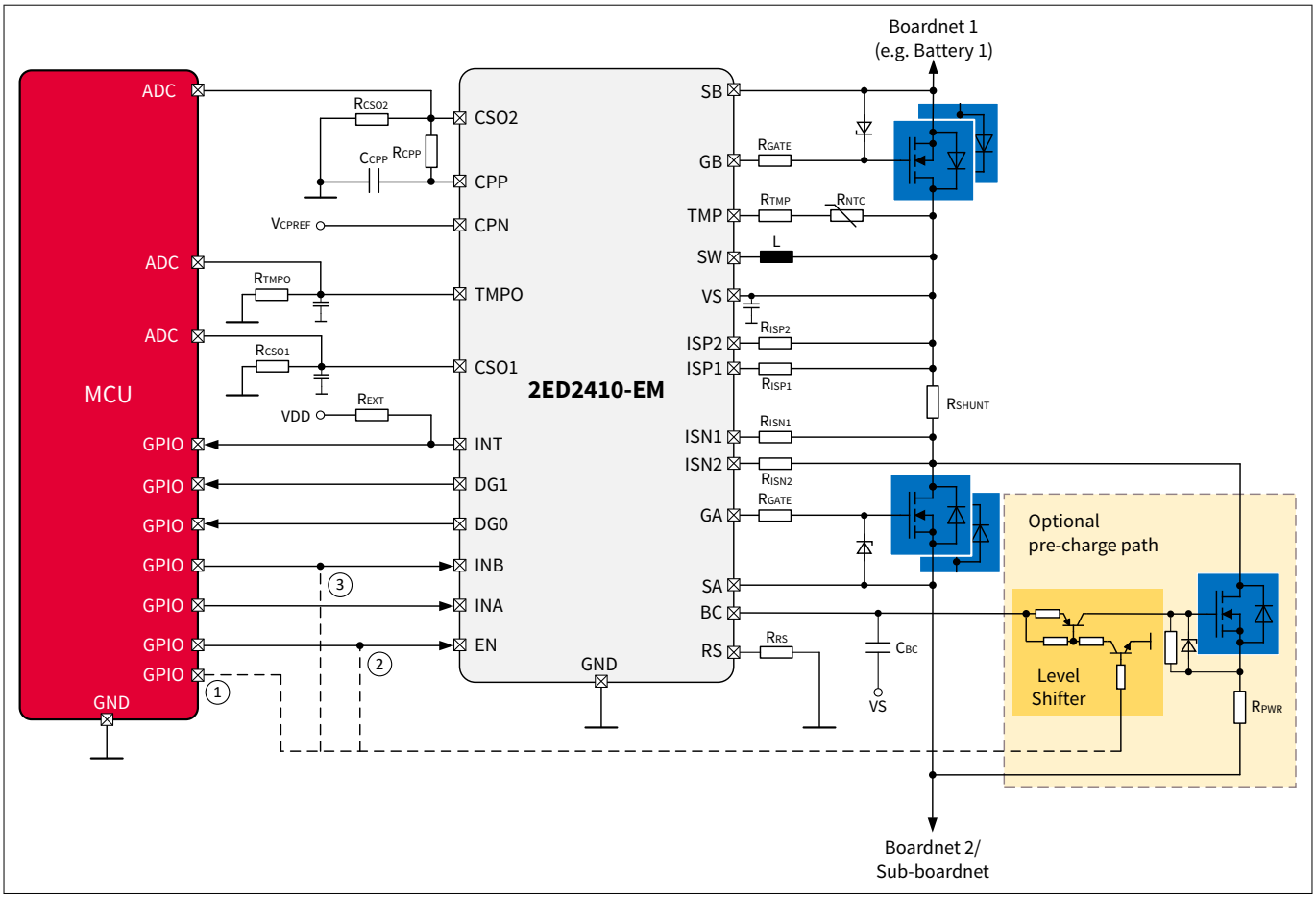


Figure 12 **Power supply protection (PSP) switch example, with a pre-charge circuit and its different control options**

***Note**: Infineon enhanced BSS83P PMOS and 2N7002 NMOS can replace PNP and NPN in the level shifter.*

***Note**: A gate-source resistor is needed for the pre-charge MOSFET to be kept OFF when the PNP (or PMOS) is open. Gate-source resistors are not needed for the power MOSFET in the main current path because the driver has an integrated gate-source pull-down by default, as long as a VS voltage is present.*

The figure below is another example that features a single high-side switch and makes use of the second gate driver output to drive the pre-charge.

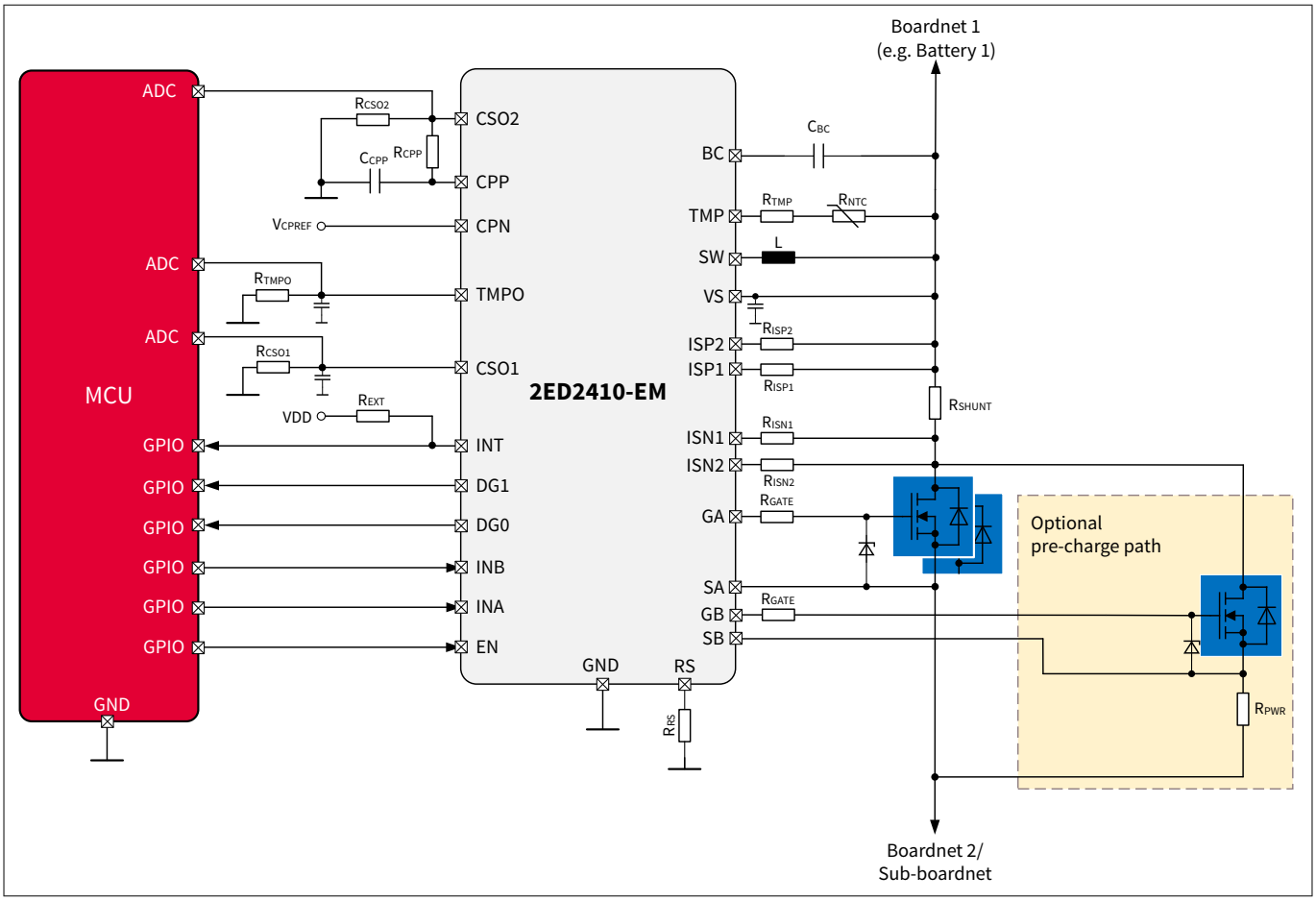


Figure 13 **Power supply protection (PSP) switch example where inverse current blocking is not needed, with a pre-charge circuit**

3.1.3 Pre-charge using Linear FET

Using the new OptiMOS™ Linear FET MOSFETs (example reference IAUAN04S7N004L), it is possible to pre-charge high values of capacitance within a short time frame with the following circuitry:

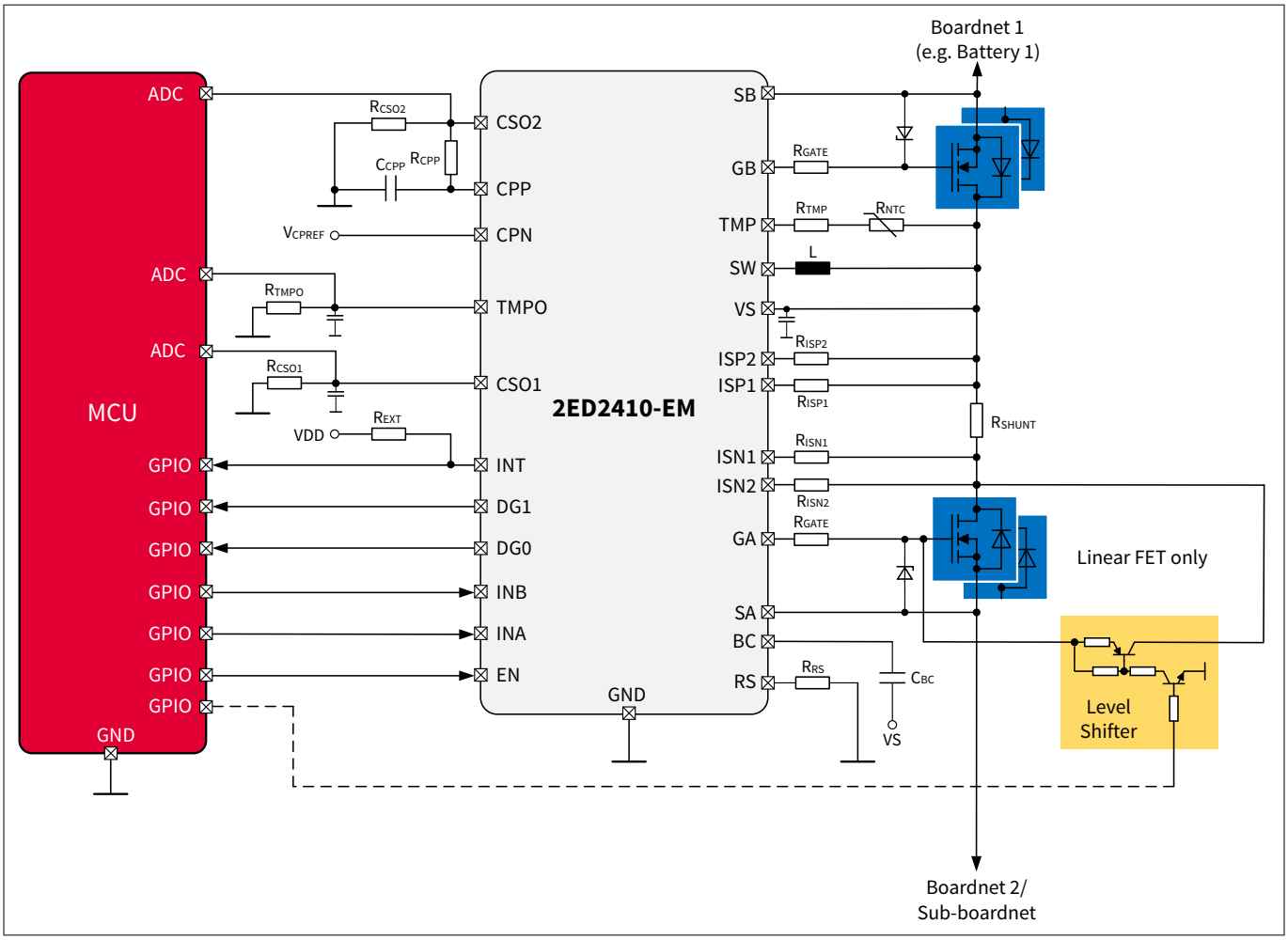


Figure 14 Power supply protection (PSP) pre-charge with OptiMOS™ Linear FET

Implementing the linear mode control circuitry shorting MOSFET drain to gate, allows for example, to pre-charge a 4 mF capacitor within 0.5 ms.

Besides the pre-charge capability, the Linear FETs also allow effectively clamping inductive energy after short circuit events, with a limited number of additional external components and our EiceDRIVER™ devices.

3.2 Supply voltage decoupling (diode between battery and VS pin)

In some applications, it is necessary to add a diode between the battery and the VS pin to ensure reverse blocking covering undervoltage events.

In either case adding a capacitor $C_{VS\text{-}BAT}$ in parallel with the diode (see Figure 15) is required, to maintain the current sense amplifier input voltage range V_S-V_{ISxx} (PRQ-344) during transient events on the supply node. Exceeding the input voltage range of the amplifier results in an undefined current sense output state, which in some cases leads to an unwanted latch (for example, due to the short circuit comparator connected to CSO1 pin).

Choose a value for C_{VS} based on system *electromagnetic compatibility (EMC)* requirements and compute $C_{VS\text{-}BAT}$ creating the capacitive voltage divider with C_{VS} on the VS pin:

$$C_{VS-BAT} \geq \left(\frac{V_{BAT1}}{V_{BAT2} + (V_S - V_{ISxx})} - 1 \right) \times C_{VS} \quad (12)$$

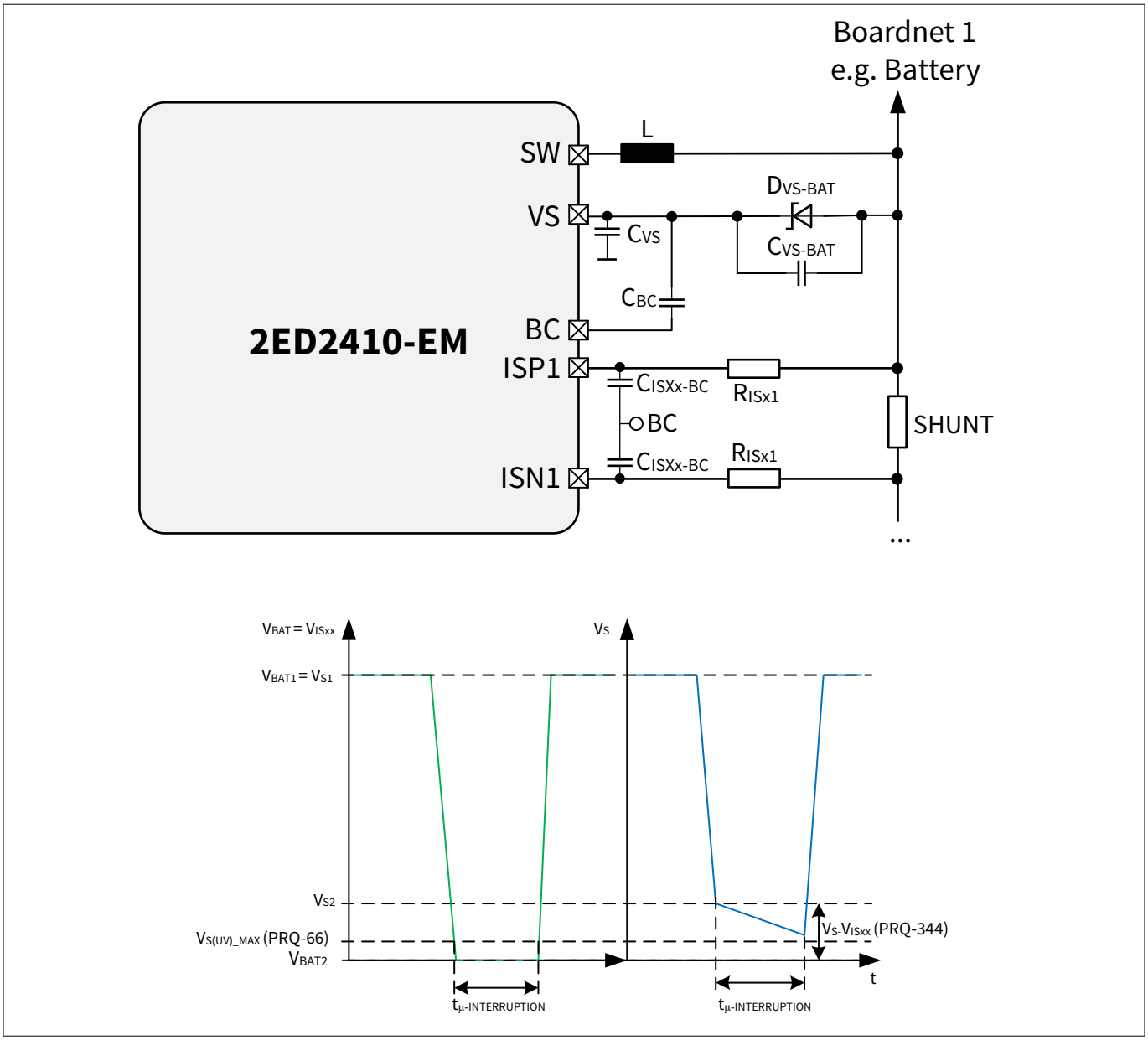


Figure 15 Principle schematic and waveforms for increased micro-interruption robustness

3.2.1 Maintaining the switch active during undervoltage events

For battery undervoltage events going lower than the maximum of $V_{S(UV)}$ (PRQ-66) specification, the diode between the battery and VS pin is required to prevent depletion of the decoupling capacitor, consequently latching the device during micro-interruptions on the supply.

The capacitance value for C_{VS-BAT} and C_{VS} withstanding supply interruption durations up to $t_{\mu\text{-INTERRUPTION}}$, considering the average bypass current $I_{SOURCE(AVE)}$ and the number of source pins connected N_{SX}:

$$C_{VS-BAT} + C_{VS} \geq \frac{t_{\mu-INTERRUPTION} \times I_{SOURCE(AVE)}}{V_{S2} - V_{S(UV)}} \quad (13)$$

The worst-case average source bypass current $I_{SOURCE(AVE)}$ during this event can be approximated to:

$$I_{SOURCE(AVE)} \cong N_{SX} \times I_{SOURCE(TYP)} \quad (14)$$

With N_{Sx} = 1 or 2

See the automated calculations in the excel workbook [2], tab “Micro-interruptions”.

It is assumed that the diode’s ($D_{VS\text{-}BAT}$) reverse leakage current is negligible compared to $I_{SOURCE(AVE)}$.

Considering VS pin is a reference voltage, the diode’s forward voltage is negligible as leakage currents will charge C_{VS} to V_{BAT} starting from SLEEP-mode.

Note that to maximize the delay before latching, due to VS undervoltage, the SW pin must be connected to the battery (see Figure 15).

For pulses longer than 1 ms, it is assumed that the microcontroller can perform the reset to meet the expected functional status C. Nevertheless, the above solution can be implemented for undervoltage durations longer than 1 ms. In this case, the boost converter output capacitance C_{BC} may need to be increased as V_{BC}-V_S decreases due to the driver’s self-consumption, leading to a boost converter undervoltage lockout (UVLO, PRQ-140).

The following tables show the resulting functional status, for example, configurations under ISO16750-2-4.6.2 typical test conditions.

Table 2 ISO16750-2 results for 100 µs interruptions – V_{BAT} = 11 V, $C_{VS\text{-}BAT}$ = 10 µF/10 V, C_{VS} = 2.2 µF/50 V

t1	Functional status expected	Functional status observed
>10 µs to 100 µs - int = 10 µs	A	A
100 µs to 1 ms - int = 100 µs	C	D
1 ms to 10 ms - int = 1 ms	C	D
10 ms to 100 ms - int = 10 ms	C	D
100 ms to 2 s - int = 100 ms	C	D

Table 3 ISO16750-2 results for 1 ms interruptions – V_{BAT} = 11 V, $C_{VS\text{-}BAT}$ = 45 µF/10 V, C_{VS} = 10 µF/50 V

t1	Functional status expected	Functional status observed
>10 µs to 100 µs - int = 10 µs	A	A
100 µs to 1 ms - int = 100 µs	C	A
1 ms to 10 ms - int = 1 ms	C	D
10 ms to 100 ms - int = 10 ms	C	D
100 ms to 2 s - int = 100 ms	C	D

4 Current sense amplifier

4.1 Operating area

Current sense amplifiers inside 2ED2410-EM operate within a specific input voltage range relative respectively to the *BC* output (BC pin) and *ground (GND)*. Parameter specification from the datasheet and consequent operating area are visualized below:

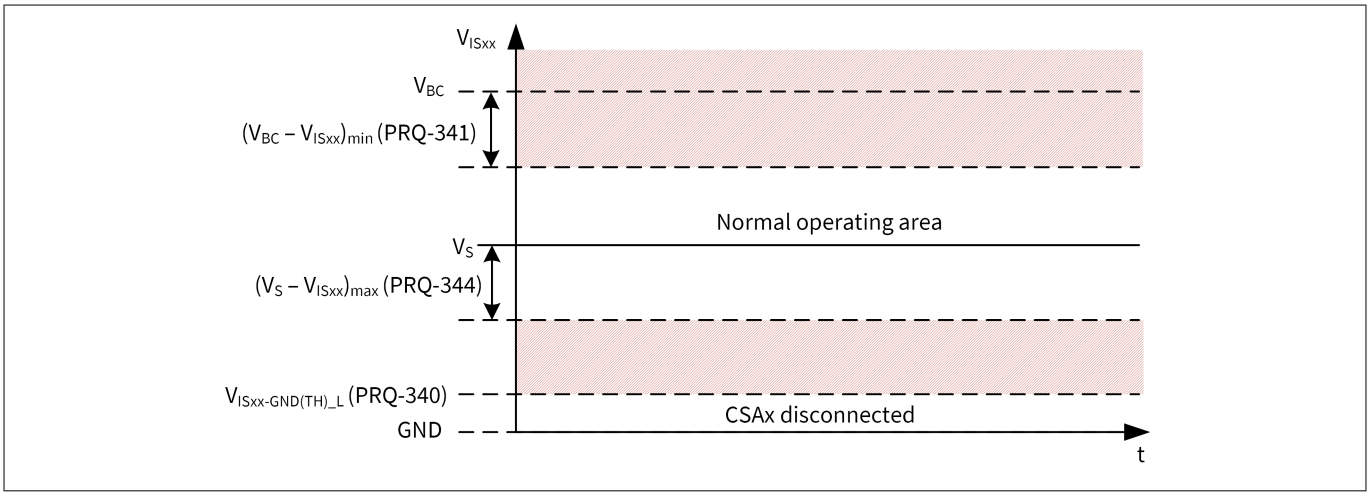


Figure 16 Current sense amplifier operating area

4.1.1 Input voltage range

In case one of the current sense amplifier inputs' voltage V_{ISxx} is outside of the input common mode voltage range (in the red striped area in Figure 16), the current sense amplifier output behavior is not guaranteed. Therefore, any operation within this area is not recommended.

4.1.2 Connection/disconnection

In some applications, one or both of the current sense amplifiers may not be needed. Disconnecting current sense amplifiers leads to a reduction of quiescent current (see Quiescent current example for quiescent current calculations). The disconnection is performed either by pulling one of the current sense input pins (ISxx pins) to VS and the other one to GND, or connecting both to GND (see figure below). In either case, the CSOx pin must be connected to GND.

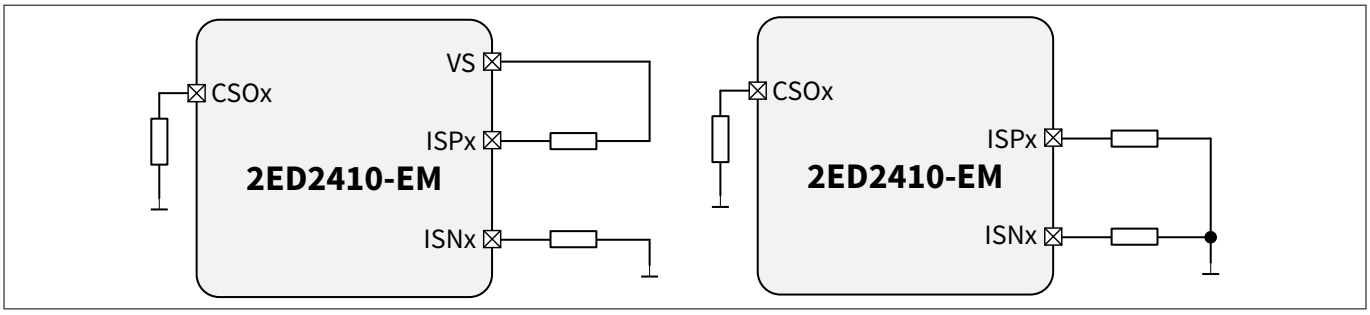


Figure 17 Current sense amplifier disconnection schemes

Resistors of up to 10 kΩ maximum can be added between the current sense amplifier pins and the respective potentials they are connected to.

In case activation and deactivation are performed during the device's operation, VISxx-GND(TH)_L (PRQ-340) specifies the lower boundary ensuring disconnection, and VISxx-GND(TH)_H (PRQ-487) specifies the higher boundary ensuring reconnection of the current sense amplifiers.

4.2 Steady state current sense error

The 2ED2410-EM driver's *current-sense amplifier (CSA)* have a very low offset [PRQ-323]. Therefore, to get the lowest error possible, resistors with a tolerance lower than 1% are recommended for R_{SENSE}, R_{ISxx}, R_{CSOx}.

The typical error between V_{SENSE} and V_{CSO1} is shown in the next figure based on V_{SENSE} values. This figure is an average based on a limited number of productive samples based on lab test conditions.

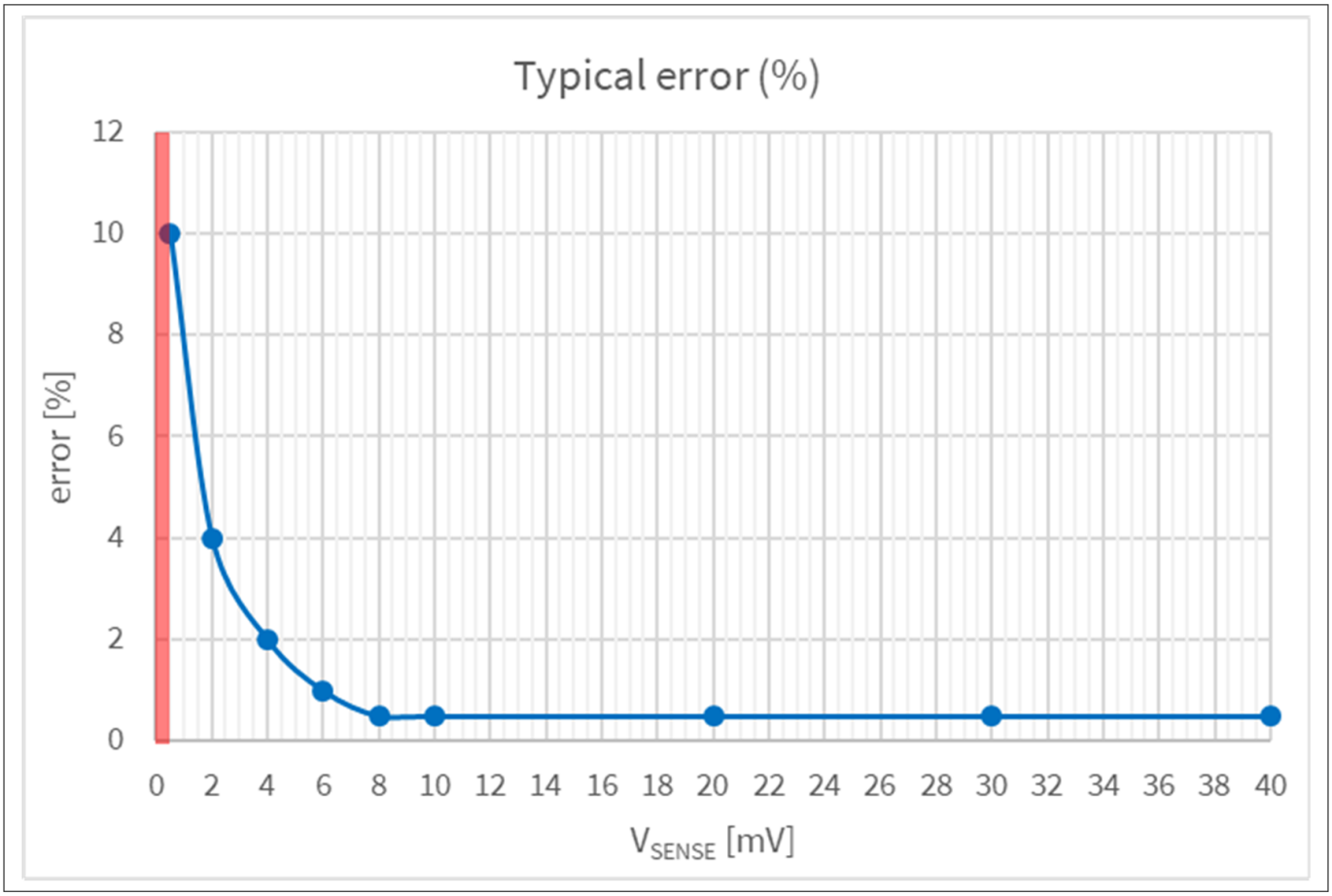


Figure 18 Typical CSA error at 25°C, VS = 12 V (in red: blind zone)

***Note**: The CSA input is not limited to 40 mV. 400 mV is also possible. The limitation is the combination of the chosen R_{SENSE}, the gain range of 2ED2410-EM [PRQ-317] and the amplifier output saturation, [PRQ-310].*

4.3 Minimum readable current

The table below shows the minimum readable current by the *CSA*, based on typical shunt/sense resistor values and the driver's blind-range (in red in Figure 18). The minimum readable current can be read with 10% accuracy typically, according to Figure 18, above.

The CSAs are meant to be operated from outside of the blind-range, therefore, sense resistance values should be chosen according to the expected minimum continuous current. It needs to be ensured that a minimum current higher than the blind-range is always present so that $V_{SENSE} \geq V_{ISx(BLIND)}$. If this is not possible, refer to

the following chapters to detect the “open-load” condition or workarounds to operate the current sense amplifiers continuously from outside of the blind-range.

The table below shows examples of sense resistance values with corresponding minimum readable current from outside of CSA blind-range and maximum nominal current while observing a thermal power dissipation of around 2 W.

Table 4 Minimum readable current and maximum nominal current based on sense resistance value

Total R_{SENSE} resistor value [Ω]	Minimum readable current [A]	Maximum nominal current [A]	Power dissipated [W]	2ED2410 Blind zone max. [µV]	FSR nominal current [mV]
0.001	0.5	45	2	500	45
0.0005	1	65	2	500	32.5
0.0002	2.5	100	2	500	20
0.0001	5	140	2	500	14
0.00005	10	200	2	500	10

***Note**: The minimum readable current corresponds to the ratio between the device’s blind-zone specification and the sense resistance, not to the current sense output when in blind-range.*

***Note**: The FSR corresponds to the nominal current measurement range for continuous current. It is possible to read higher dynamic currents.*

4.4 Current sense blind zone

The current sense “blind-range” or “blind zone” is specified in the datasheet [1] as a differential input voltage $V_{ISx(BLIND)}$ [PRQ-324].

Within the mentioned differential input voltage range, the current sense output does not display accurate current sense information. The combination of V_{CSOx} with current direction information on DG1 allows for maximum resolution across the reading range as the driver outputs from $G * V_{ISx(BLIND)}$ to $V_{AMP(SAT)}$ [PRQ-310].

The next figures illustrate the DG1 pin behavior in the blind zone, which can be observed during slow current ramps of 7.6 µA/µs and 0.5 mA/µs.

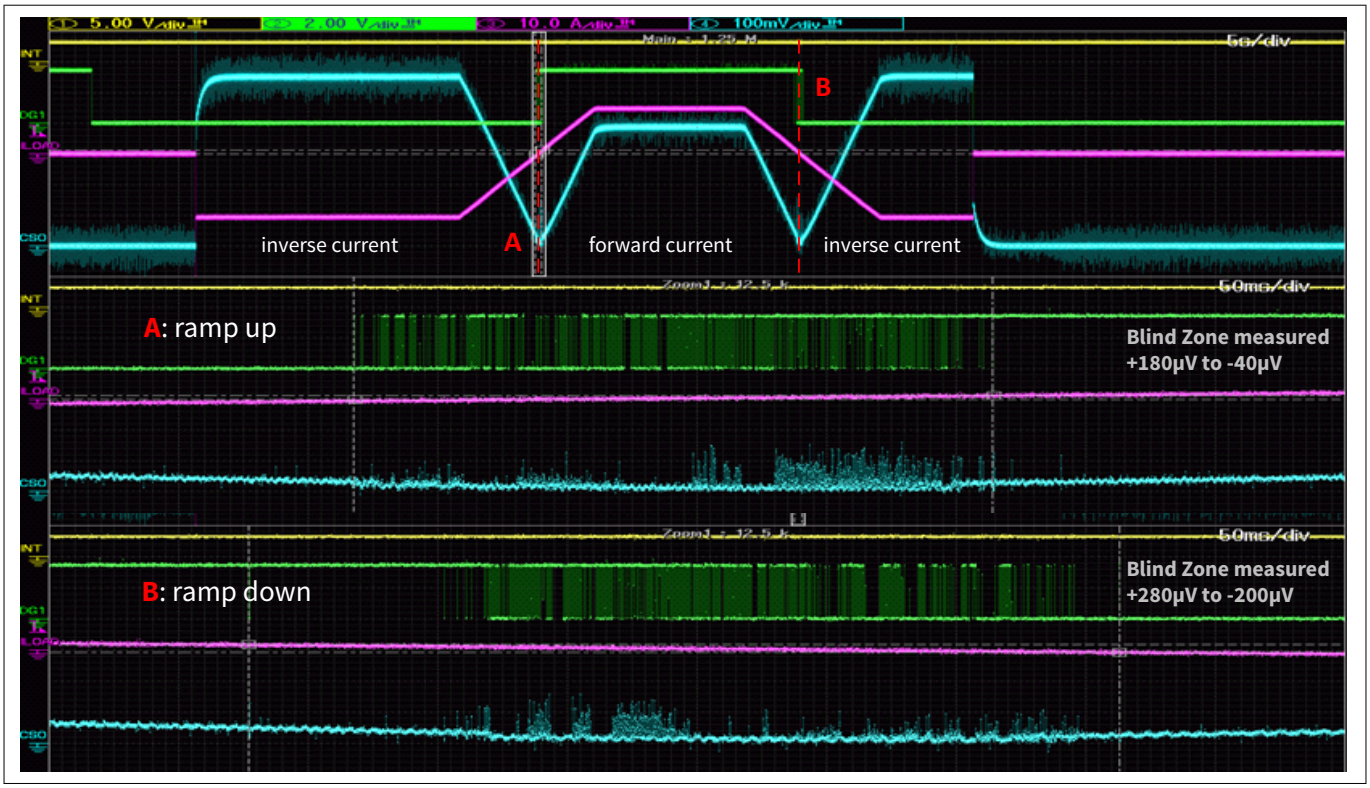


Figure 19 DG1 behavior in blind zone with slow ramp 7.6 µA/µs

V_S= 24 V, V_{EN}= 3.3 V, G = 100, R_{SENSE} = 200 µΩ [Yellow V_{INT}; Green V_{DG1}; Purple I_{LOAD}; Blue V_{CSO1}]

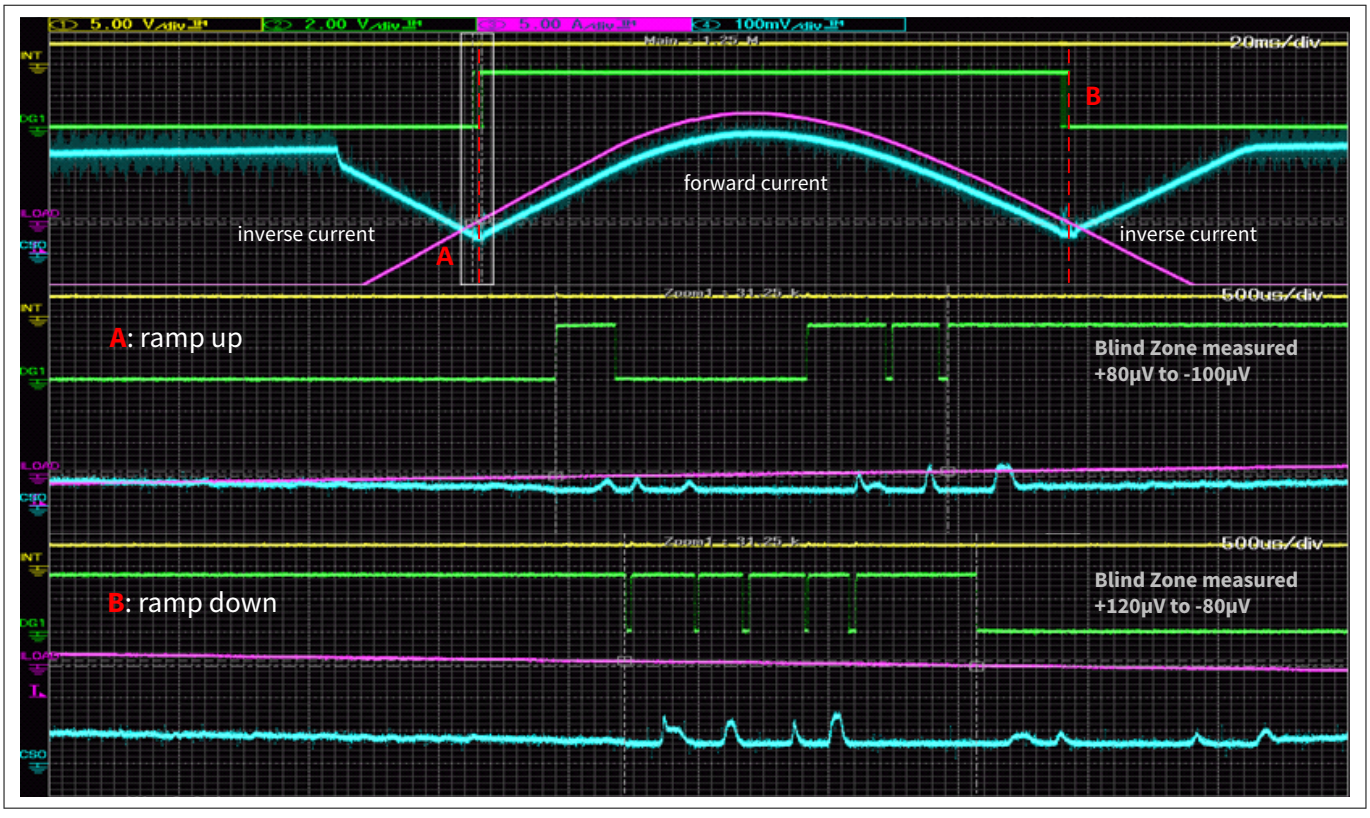


Figure 20 DG1 behavior in blind zone with slow ramp 0.5 mA/µs

V_S= 24 V, V_{EN}= 3.3 V, G = 100, R_{SENSE} = 200 µΩ [Yellow V_{INT}; Green V_{DG1}; Purple I_{LOAD}; Blue V_{CSO1}]

If the current ramp is faster, for example, 10 mA/µs, the blind zone would not be seen on DG1. Delay t_{ISD} applies when the current direction changes.

It is necessary to verify that the minimum continuous current $I_{NOM(MIN)}$ which will always flow through the switch leads to operation outside of blind range:

$$\left|V_{SENSE(MIN)}\right| = \left|I_{NOM(MIN)}\right| \times R_{SENSE} \geq \left|V_{ISx(BLIND)}\right| \tag{15}$$

If this cannot be ensured, refer to Ensure operation from outside of the blind zone using an external offset.

4.4.1 Open load detection using diagnostic in ON-mode

When in open load condition, the CSA is inside the blind-zone and therefore no information can be retrieved from the current sense output. Thanks to the DG1 pin current direction indication toggling as the current direction is unknown, the open load condition can be detected using a simple logic implemented inside the microcontroller:

- Implement an edge counter on DG1 pin
- If the number of DG1 edges is higher than 2 within a period of V_{CSOx} sampling, then the V_{CSOx} measurement can be discarded

4.4.2 Ensure operation from outside of the blind zone using an external offset

When the minimum continuous load current is too low to continuously ensure $V_{SENSE} \geq V_{ISx(BLIND)}$, and the sense resistor value cannot be further increased, an external offset circuitry can be implemented to work around the CSA blind-range.

Principle: a small constant current is drawn from the battery to bias the input resistor so that a voltage above $V_{ISx(BLIND)}$ is applied across that resistor and therefore between ISPx and ISNx pins (see Figure 21). This way, even when no current is flowing through the sense resistor, the amplifier operates from outside of the blind zone with an input voltage:

$$V_{OFFS(EXT)} = I_{OFFS(EXT)} \times R_{ISxx(OFFS)} \tag{16}$$

It may be necessary to split the current sense input resistance value into two resistors to achieve the desired offset depending on how much offset current can be drawn with the external circuitry.

The offset voltage must be considered in the back calculation of the current when acquired with a microcontroller ADC:

$$I_{LOAD} = \frac{\frac{V_{CSOx}}{G} - V_{OFFS(EXT)}}{R_{SHUNT}} \tag{17}$$

This is also applicable to the overcurrent protection threshold which will be covered in the following chapter.

Beware that applying an offset modifies the operation boundaries for the inverse current direction. To ensure operating outside of blind-range with an inverse current, the input voltage must exceed the blind zone and the offset value:

$$\left|V_{SENSE}\right| \geq \left|V_{ISx(BLIND)}\right| + \left|V_{OFFS(EXT)}\right| \tag{18}$$

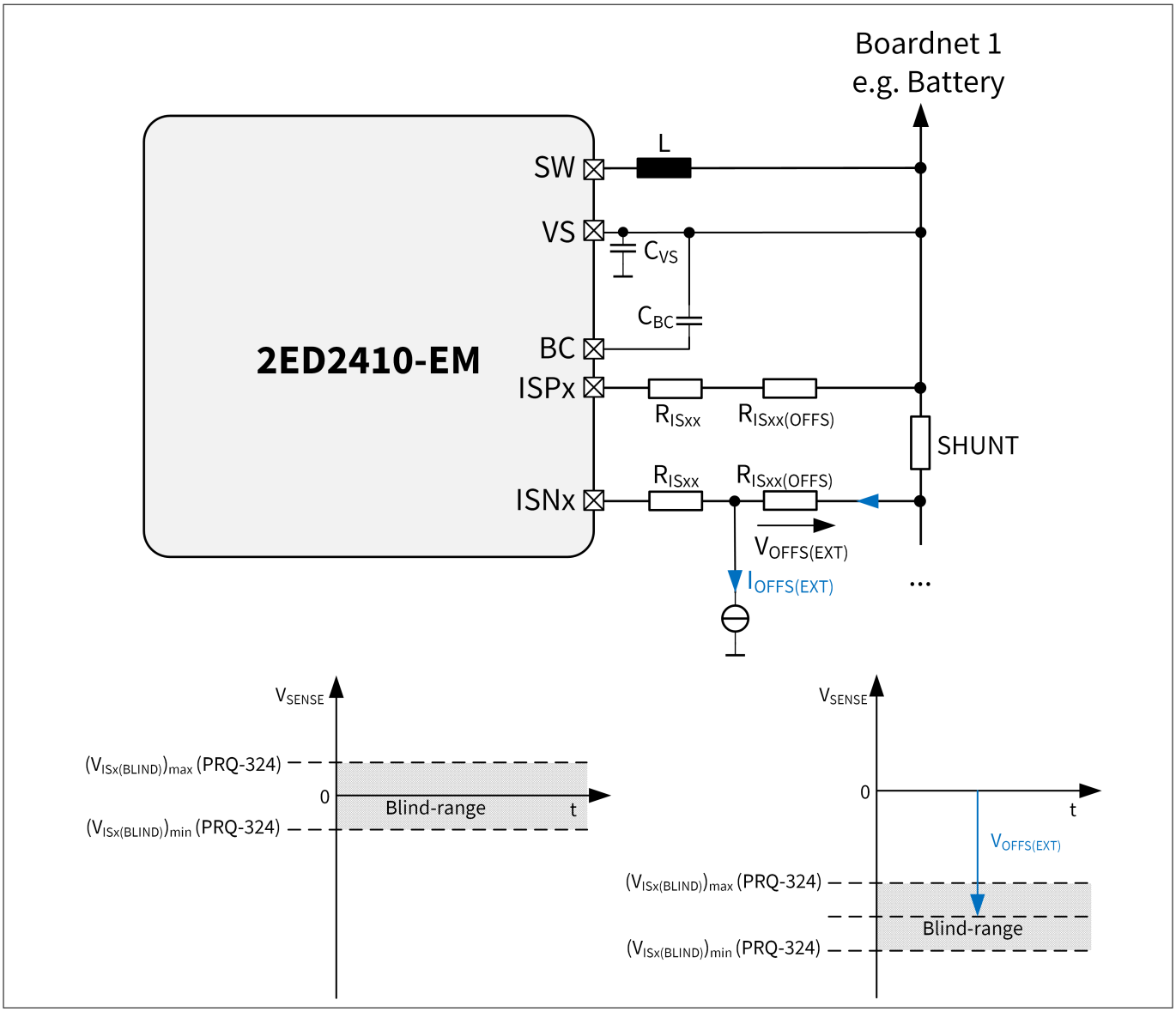


Figure 21 External offset principle and blind-range shift

4.5 Short circuit protection

This section provides a methodology on how to accurately set up a short-circuit limit using *CSA* 1 (CSA1). The sensing element, here a shunt resistor, is initially set by the customer based on the application's thermal and electrical requirements (see Minimum readable current). The EN pin voltage is either fixed by the low voltage power supply or the microcontroller. To target the desired protection threshold and obtain consistent current readings, R_{ISPx}, R_{ISNx} and R_{CSOx} need to be determined according to each application's requirements.

The 2ED2410-EM's current sense amplifiers are meant to operate outside of the blind-range ($V_{ISx(BLIND)}$, PRQ-324). The below example and calculations assume that the CSAx are outside of the blind-range. If the application assumptions lead to an operation within the CSA blind-range, and none of the previously presented ways to ensure CSA operation from outside of blind-range can be implemented in the application, contact Infineon sales representatives.

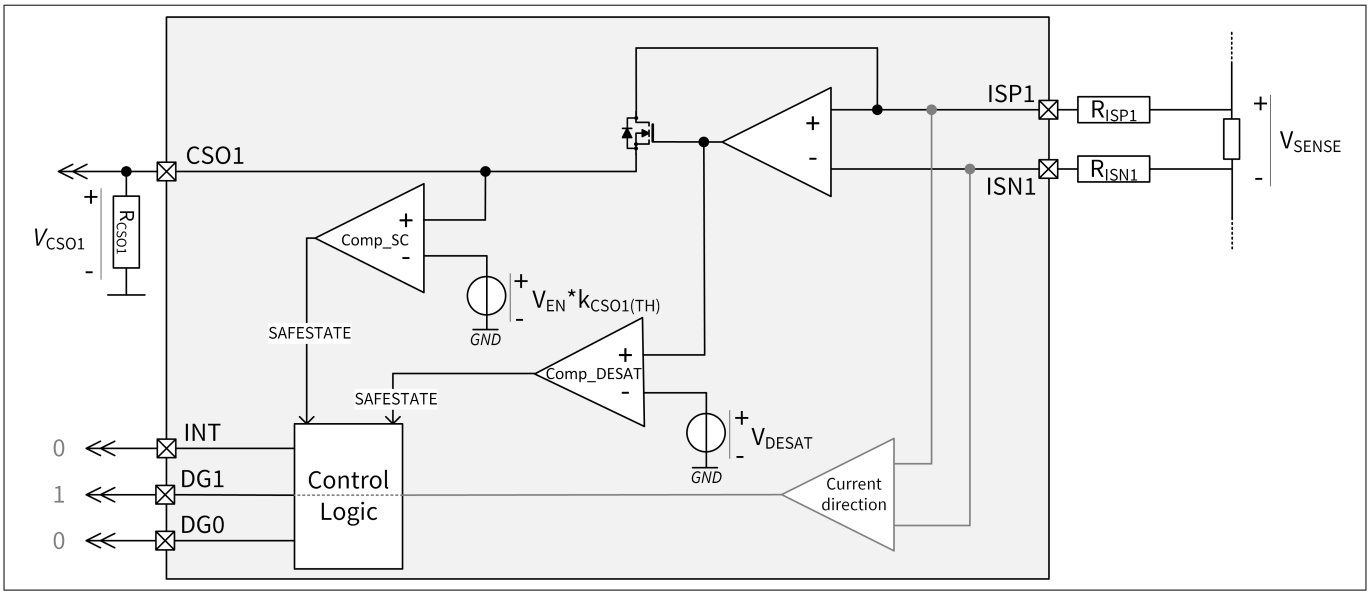


Figure 22 Overview of bi-directional current sense amplifier CSA1

***Note**: CSA2 is identical, but does not feature the COMP on the output for protection. CSA1, internal* COMP, *and diagnostics (one amplifier direction represented for simplicity).*

4.5.1 Managing short circuit requirements

While sizing the short circuit protection, two main requirements need to be ensured:

- Load availability: the device protection should be set so that no latch occurs in case of a load step (within the load current profile) close to the short circuit detection threshold. Therefore, a margin between the maximum load step current and the minimum short circuit protection current level should be implemented
- MOSFET current and energy rating: the device overcurrent protection should be set so that the maximum peak current reached during a short circuit current does not lead to the destruction of the power MOSFETs

The following paragraphs will guide through the sizing of the short circuit protection with 2ED2410-EM's current sense amplifiers with an example aiming to demonstrate setting a short circuit protection for a maximum load current of I_{LOAD_MAX} = 200 A, a maximum continuous current $I_{NOM(MAX)}$ below 65 A (see Table 4) and a minimum continuous current of $I_{NOM(MIN)}$ = 5 A (see Current sense blind zone).

4.5.2 Sizing overcurrent protection in shunt resistor based applications

Most applications in power distribution use a shunt resistor for current sensing and overcurrent protection. The following steps guide through the calculations with example values to set the required short circuit protection level using a shunt resistor:

1. Select the appropriate resistor according to previous chapters: R_{SHUNT}= *500 µΩ*
2. Determine the maximum load current slope in the application:

$$\left(\frac{dI_{LOAD}}{dt}\right)_{MAX} = 5\frac{A}{\mu s}$$

3. When using a shunt resistor, determine the shunt's parasitic inductance and consequent constant error across the current sense inputs during a load current step:

$$V_{SHUNT} = L_{SHUNT} \times \left(\frac{dI_{LOAD}}{dt}\right)_{MAX} = 1.5 \quad nH \times 5\frac{A}{\mu s} = 7.5 \quad mV \tag{19}$$

4. Determine if an external offset is required (see Ensure operation from outside of the blind zone using an external offset): $V_{OFFS(EXT)} = 0\ mV$
5. Compute the initial minimum short circuit protection threshold:

$$I_{SC(TH)MIN} \geq I_{LOAD_{MAX}} + \frac{V_{SHUNT(ERR)} + V_{OFFS(EXT)}}{R_{SHUNT}} = 200 \quad A + \frac{7.5 \quad mV + 0 \quad mV}{500 \quad \mu\Omega} = \quad 215 \quad A \tag{20}$$

6. Compute the initial gain:

$$G = \frac{k_{CSO1(TH)MIN} \times V_{EN_{MIN}}}{R_{SHUNT} \times I_{SC(TH)MIN}} = \frac{0.718 \times 5 \quad V}{500 \quad \mu\Omega \times 215 \quad A} = 33.4 \tag{21}$$

7. Determine the CSAx overshoot based on maximum load step input voltage slope, initial gain, and target output voltage:

   $OVS_{CSOx} = 8\%$

   The characterization report is available on Infineon's myICP platform to adjust on each application's specific current sense amplifier implementation and system requirements

$$\left(\frac{dV_{SENSE}}{dt}\right)_{MAX} = \left(\frac{dI_{LOAD}}{dt}\right)_{MAX} \times R_{SHUNT} = 5\frac{A}{\mu s} \times 500 \quad \mu\Omega = 2.5\frac{mV}{\mu s} \tag{22}$$

$$V_{CSOx(TARGET)} = \quad G \times \left(I_{LOAD} \times R_{SHUNT} + V_{OFFS(EXT)}\right) = \quad 33.4 \times (200 \quad A \times 500 \quad \mu\Omega + 0 \quad mV) = \quad 3.34 \quad V \tag{23}$$

Read the overshoot value from the values provided in the graph with respect to the closest $V_{CSOx(TARGET)}$ in the figure below:

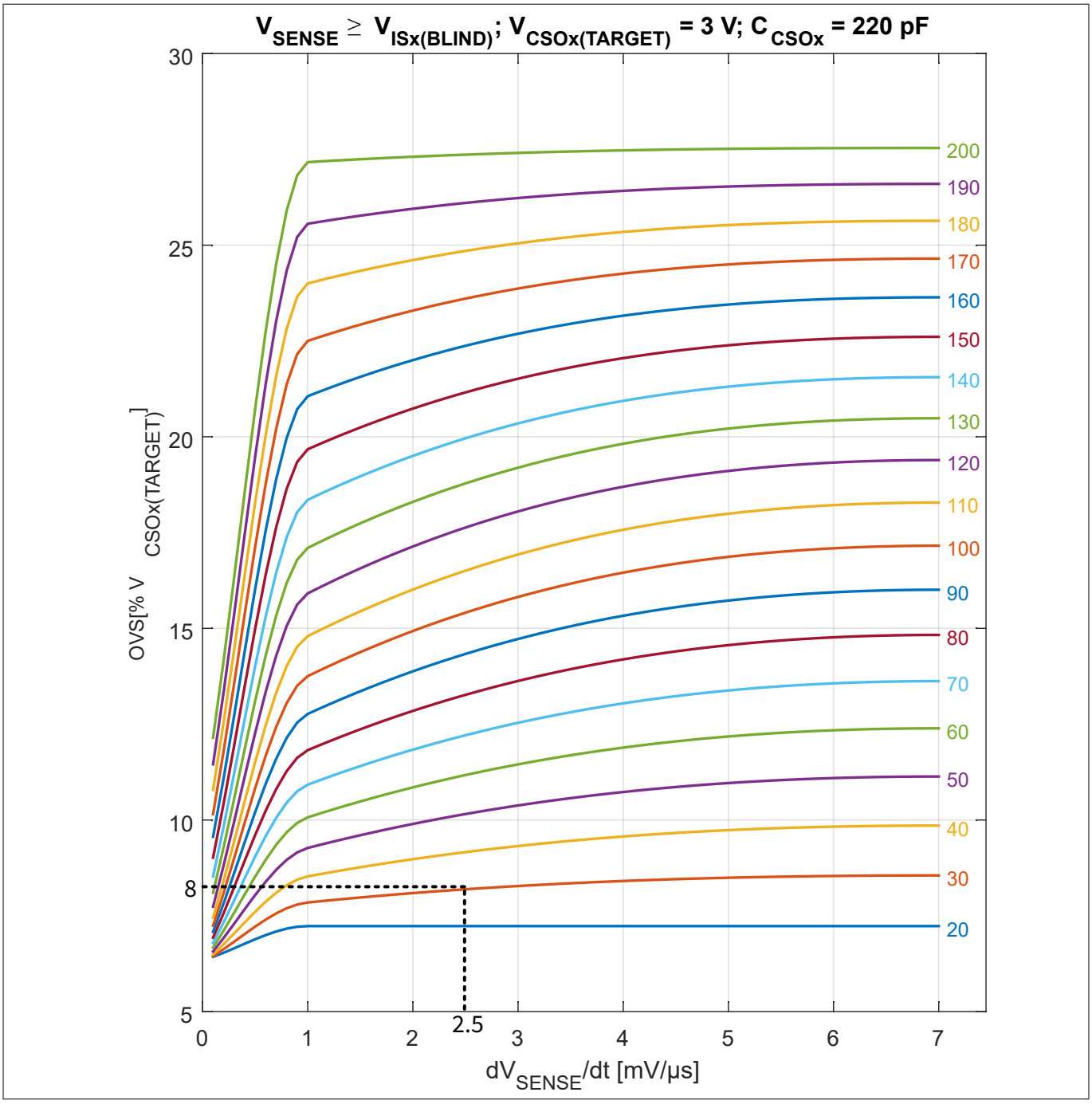


Figure 23 **CSOx overshoot graph reading for $V_{CSOx(TARGET)}$ = 3 V, dV_{SENSE}/dt = 2.5 mV/µs and G = 33.4**

8. Compute the minimum short circuit threshold required:

$$I_{SC(TH)_{MIN}} \geq I_{LOAD_{MAX}} \times (1 + OVS_{CSOx}) + \frac{V_{SHUNT(ERR)} + V_{OFFS(EXT)}}{R_{SHUNT}} = 200 \quad A \times \left(1 + 8\,\%\right) + \frac{7.5 \quad mV + 0 \quad mV}{500 \quad \mu\Omega} = 231 \quad A \tag{24}$$

A significant part of the oversizing in short circuit detection level is due to the parasitic inductance of the shunt resistor. Placing two or more in parallel will allow reducing the total parasitic inductance and consequently the associated error

9. Compute the final gain for the application:

$$G = \frac{k_{CSO1(TH)\_M} \times V_{EN\_M}}{R_{SHUNT} \times I_{SC(TH)\_M}} = \frac{0.718 \quad \times 5 \quad V}{500 \quad \mu\Omega \times 231 \quad A} = 31 \tag{25}$$

10. Choose the external current sense resistor value R_{CSO1} within R_{CSOx} [PRQ-326] specification range: R_{CSO1}= 20 kΩ

11. Compute the input resistors R_{ISx1}:

$$R_{ISx1} = \frac{R_{CS01}}{G} = \frac{20 \quad k\Omega}{31} = 645 \quad \Omega \tag{26}$$

***Note**: It is recommended to use low tolerances (0.01%) to minimize the error linked to variation of the resistance over lifetime and temperature.*

4.5.3 Current sense output impedance considerations

Beware of any circuitry in the impedance range of R_{CSOx} connected to the current sense outputs. Commonly used circuits to filter the current sense output voltage for the *analog-to-digital converter (ADC)* interface dynamically change the impedance of the CSOx node to ground which lead to a dynamical gain change consequently shifting the short circuit detection. It is recommended to use only CSO2 pin for current measurement to avoid the impact of any external circuitry on the short circuit protection using CSA1.

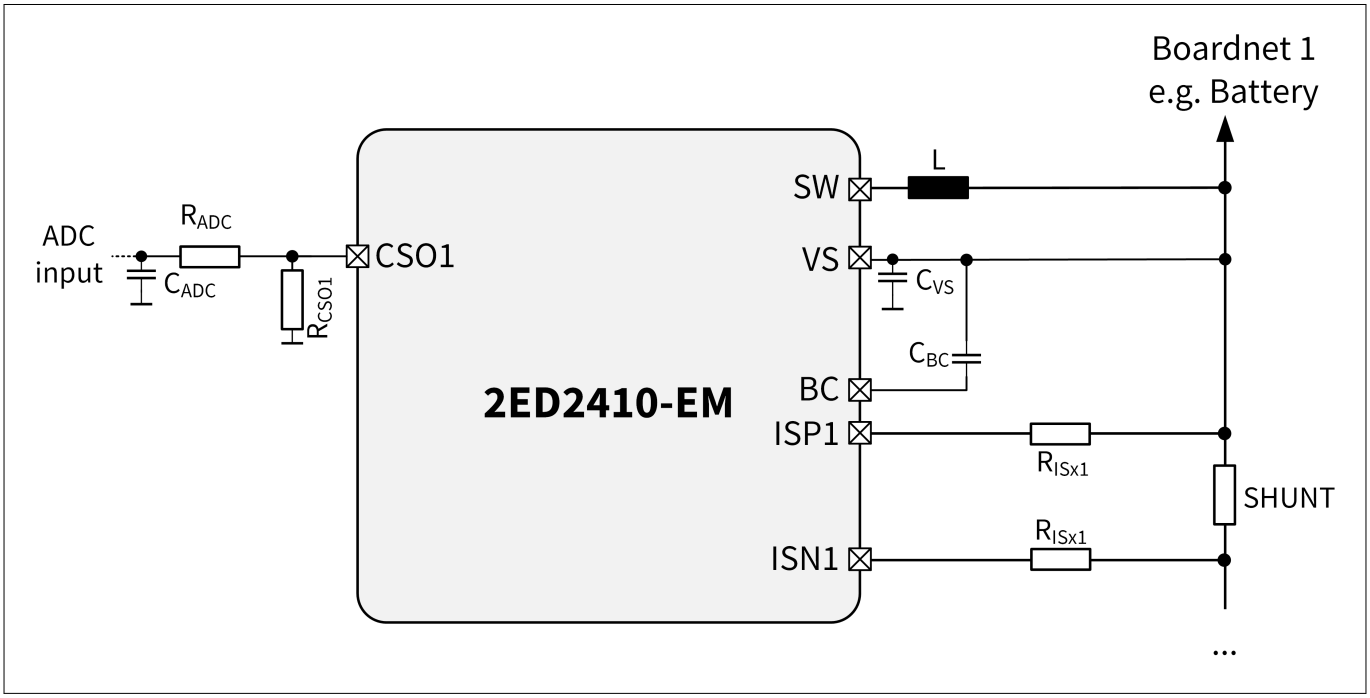


Figure 24 Current sense output equivalent resistance to GND

Taking the example of a 350 µs filter implemented according to two configurations, assuming a R_{CSOx} value of 20 kΩ:

- R_{ADC} = 10 kΩ; C_{ADC} = 35 nF
- R_{ADC} = 470 kΩ; C_{ADC} ≈ 470 pF

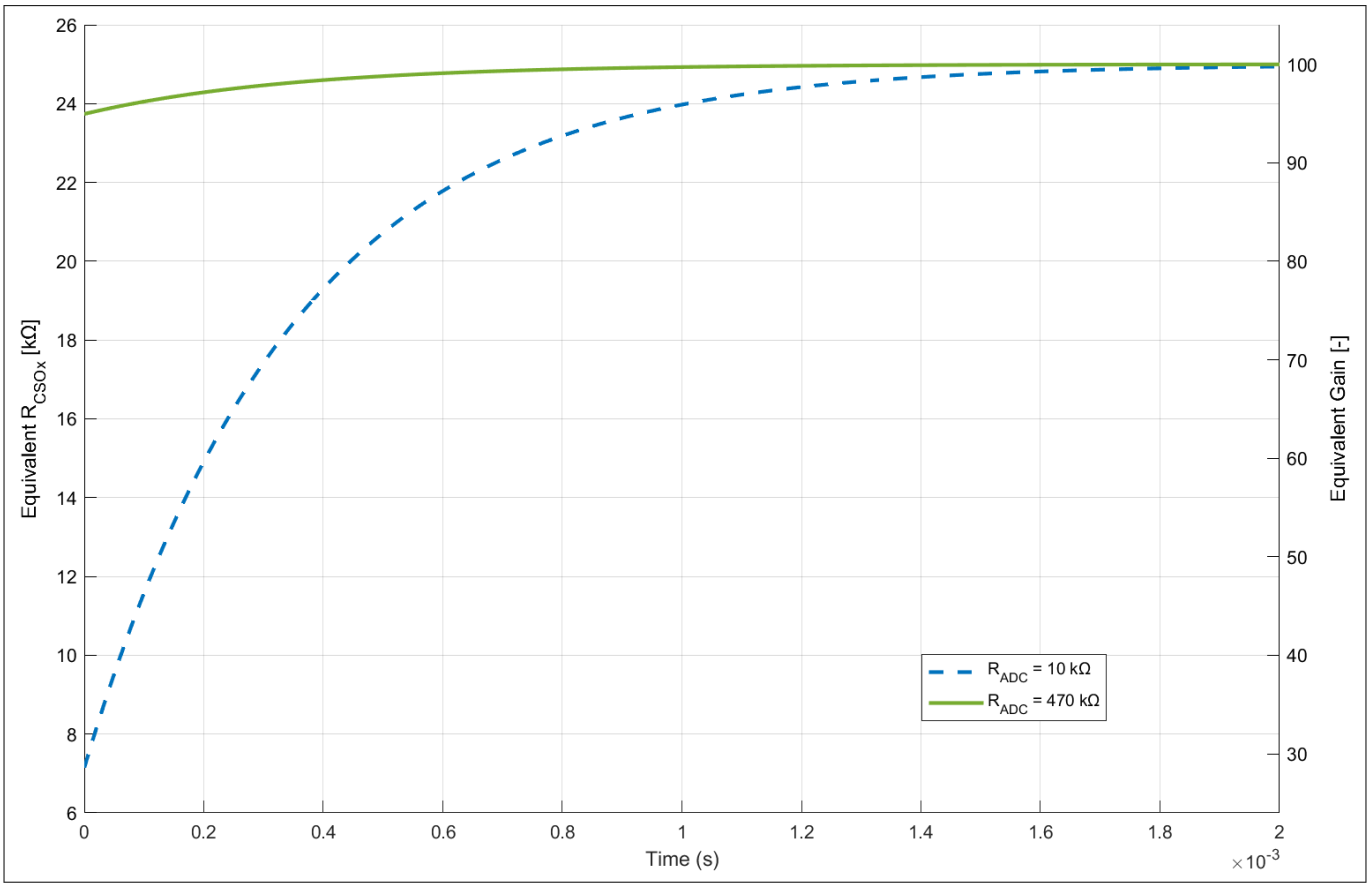


Figure 25 Evolution of equivalent current sense output resistance and gain vs time (for RADC = 10 kΩ in blue and RADC = 470 kΩ in green)

In any circumstances, it is highly recommended to maintain equivalent resistance to ground in the R_{CSOx} range (PRQ-326), as external circuitry leading to much lower resistance can affect the current sense output behavior and therefore the short circuit protection of the device, especially in the case of CSA1 (see Desat comparator).

$$R_{CSOx_{MIN}} < \frac{R_{CSOx} \times R_{ADC}}{R_{CSOx} + R_{ADC}} \quad (27)$$

In case the upper condition cannot be fulfilled, it is recommended to implement a follower circuit decoupling the CSOx from the ADC pre-conditioning circuitry.

4.5.4 Minimum short circuit comparator reference voltage

Beware that a minimum reference voltage of $V_{CSOx(TH)\_MIN}$(PRQ-485, PRQ-486) must be respected. To avoid triggering *COMP*s connected to either current sense output used for short circuit protection due to noise coming from CSA outputs or from the system.

- Short circuit protection using CSO1 pin:

  The reference voltage of the SC-COMP being determined by the V_{EN} voltage which lowest acceptable voltage is determined by $V_{CSO1(TH)\_MIN}$ as follows:

$$V_{CSO1(TH)\_MIN} = k_{CSO1(TH)\_MIN} \times V_{EN\_MIN} = \frac{2.3V}{0.718} \Leftrightarrow V_{EN\_MIN} = 3.2V \quad (28)$$

This can be achieved with a typical V_{EN} of 3.3 V supplied by a source with a total system tolerance of maximum ± 3% (microcontroller or LDO output supply voltage variation tolerance and additional external components such as resistive voltage dividers)

- Short circuit protection using CSO2 pin:

  Any reference voltage source can be used, provided that the lowest value is not below $V_{CSO2(TH)\_MIN}$ = 2.3 V

Note that when filtering the V_{CSO2} with a filter time constant (R_{ADC}*C_{ADC}) higher than 150 µs the noise can be expected to be limited to a level where voltages across the $V_{CP(REF)}$ range can be used as reference voltages.

Typically, I-t wire protection applications can be implemented with a reference voltage as low as $V_{CP(REF)\_MIN}$ on CP-COMP.

4.5.5 Desat comparator

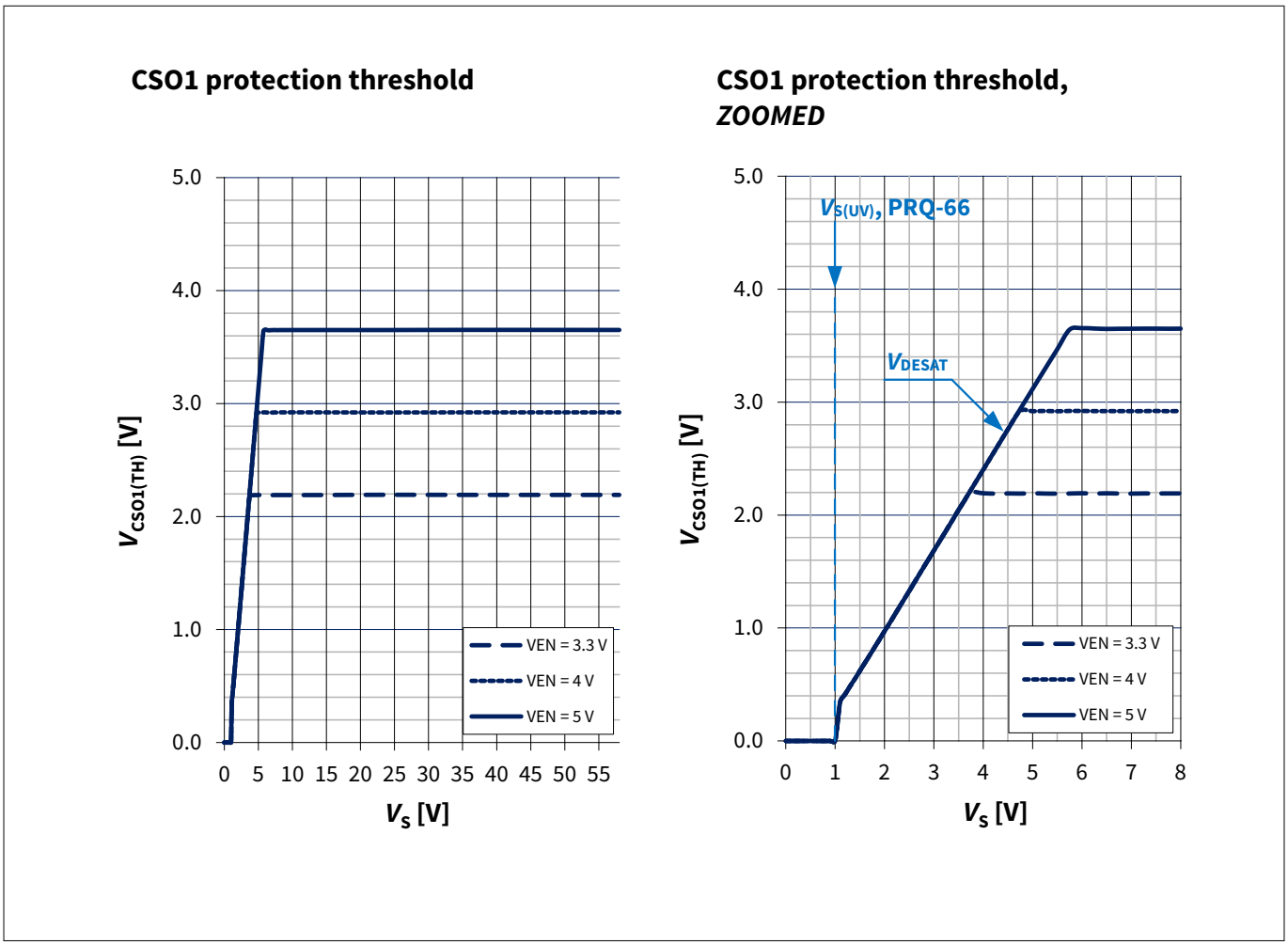


Figure 26 Typical VCSO1(TH) versus VS (independent of TJ)

In addition to the short circuit *COMP*, the CSA1 also embeds a so called “comp_DESAT” COMP (see Figure 22) which covers the following scenarios:

- Short circuit protection in the lower extended supply voltage range ($V_S = V_{S(SC)LOW}$, PRQ-40): In these conditions, the current sense amplifier cannot output a current sense output voltage up to $V_{AMP(SAT)}$,

hindering the device from transitioning to SAFESTATE-mode with the internal short circuit COMP. To achieve this, the desat COMP voltage reference V_{DESAT} lowers according to Figure 26, allowing the current sense output to trigger the COMP. This way short circuit protection is ensured even when battery voltage collapses below $V_{S(NOR)}$

- CSO1 pin short to ground protection: To ensure short circuit protection even when the current sense output might be shorted to ground and failing to output the desired current sense voltage, the device goes into SAFESTATE. Therefore, when the current sense output resistor R_{CSO1} is below R_{CSOx} (PRQ-318), the equivalent impedance from CSO1 pin to ground is too low or a short to ground occurs on this pin, the desat COMP is triggered. Consequently, it is recommended to follow the recommendations related to the minimum equivalent current sense output impedance to ground in Current sense output impedance considerations

The ”desat” COMP allows for a short circuit protection in the upper described scenarios with a reaction delay of $t_{DSCG(L)\_LOW}$ (PRQ-343).

5 Temperature sense amplifier

The main drawback of the "standard solution" is that it needs to use the V_{DD} of a microcontroller.

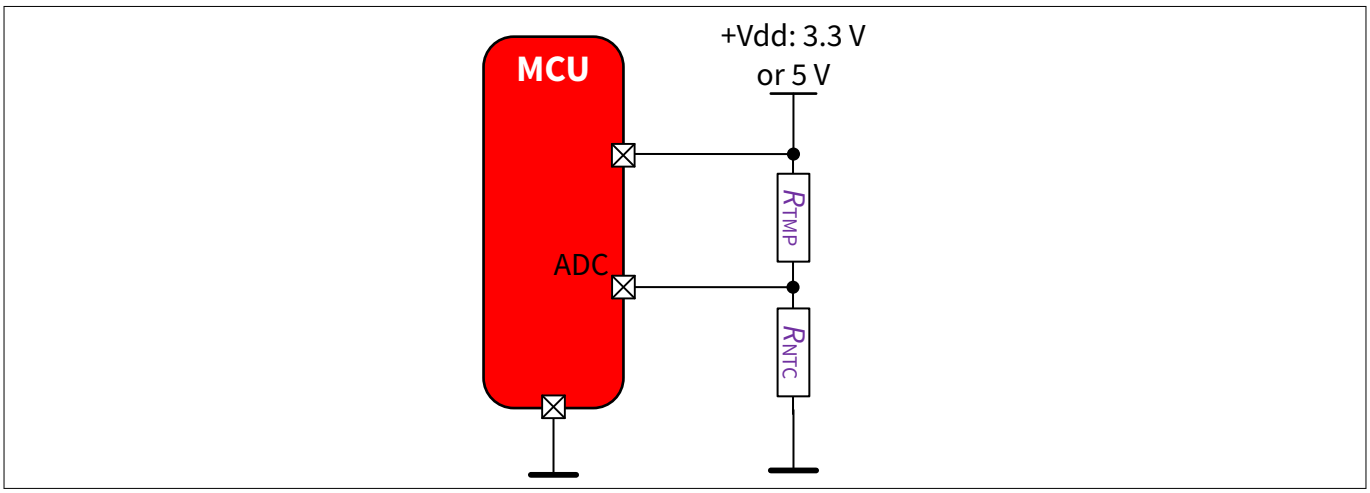


Figure 27 Basic temperature sense circuit

Therefore, it is complicated to route on layout the *negative temperature coefficient (NTC)* (or another thermistor used) to the MOSFET TAB and back to the microcontroller. This basic circuit also draws additional consumption permanently; as long as V_{DD} is still on, meaning, it would need additional components to control it with a small NPN or NMOS to activate or deactivate it and therefore an additional µC GPIO used.

The purpose of 2ED2410-EM's temperature amplifier is to sense switch temperature which is the equivalent of MOSFET TAB temperature. The advantage of 2ED2410-EM solution is that the V_{DD} is replaced by the battery line voltage and therefore the thermistor being either *positive temperature coefficient (PTC)* or NTC is in the upper position. Therefore, it is very easy to route the layout of the thermistor close to MOSFET TAB. See VS node routing for routing example.

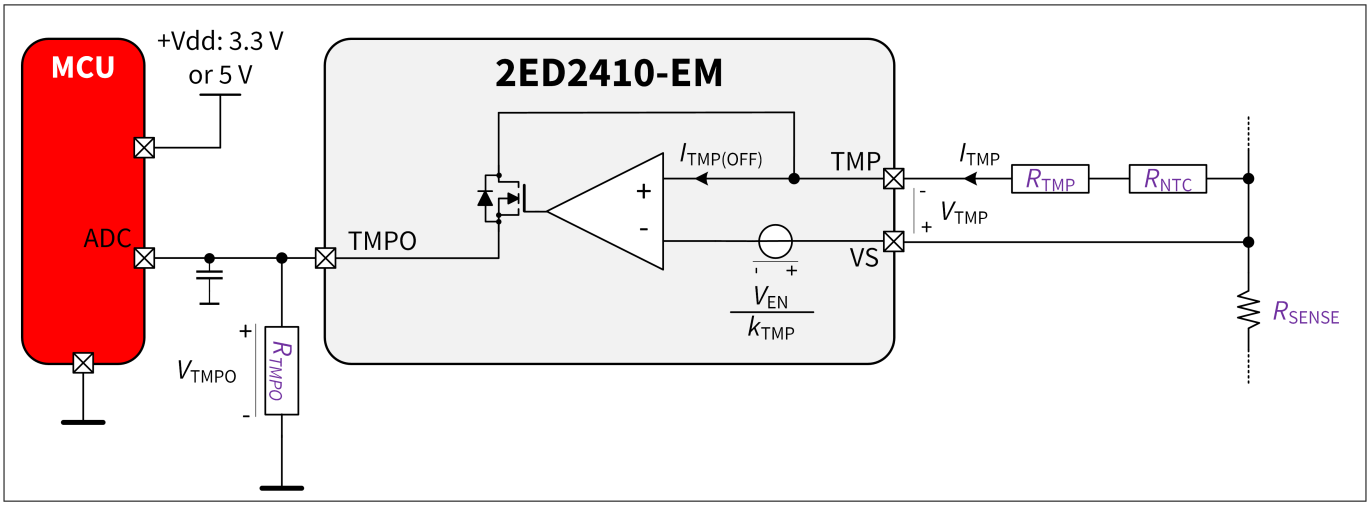


Figure 28 Overview of temperature sense amplifier TMPA

Other advantages are the following:

- The output of the TMPA amplifier is independent of battery voltage, and varies according to the resistors' settings. Not the case with the basic temperature sensing circuit shown in Figure 27
- The consumption of the TMPA amplifier itself is low. In addition, this additional self-consumption current is not present in IDLE or SLEEP mode, because the amplifier is not activated in these modes

- The output can be linearized easily using R_{TMP} resistor. Therefore, temperature can be sensed accurately over a wide range, for example, from 0°C to 150°C. It can be verified with a demo board and a temperature sensor
- It is advised to use 10 nF on TMPO, see Table 6

5.1 TMPA target curve calculation example

TMPA is an amplifier of current. The current I_{TMP} is conserved through the temperature amplifier, which, by neglecting $I_{TMP(OFF)}$, can be written:

$$I_{TMP} = \frac{V_{TMP}}{(R_{NTC} + R_{TMP})} = \frac{V_{TMPO}}{R_{TMPO}} \tag{29}$$

In Equation (30), R_{NTC} is the thermistor (in this case an NTC thermistor) resistance which varies with the temperature, and R_{TMP} is a normal resistor used to linearize the thermistor behavior with respect to temperature, positioned as per Figure 28. Therefore, V_{TMPO} can be written as:

$$V_{TMPO} = \frac{V_{TMP} \times R_{TMPO}}{(R_{NTC} + R_{TMP})} \tag{30}$$

By substituting V_{TMP} with k_{TMP} (PRQ-187) and V_{EN} in Equation (30), and considering the input offset of TMPA (PRQ-186):

$$V_{TMPO} = \left(\frac{V_{EN}}{k_{TMP}} + V_{TMP(OFFSET)}\right) \times \frac{R_{TMPO}}{(R_{NTC} + R_{TMP})} \tag{31}$$

Computed for different temperature values, it allows to trace V_{TMPO} [V] = $f(T$ [°C]), depending on the law used to describe the temperature variation of the thermistor.

The example in the figure below, is given for V_{EN} = 3.3 V, an automotive qualified 47 kΩ NTC and R_{TMP} = 1.2 kΩ. Equation (32) was used to compute $R_{NTC} = f(T$ [°C]) (where T and T (25°C) are expressed in Kelvin):

$$R_{NTC} = R_{(T\,=\,25°C)} \times e^{\beta \times \left(\frac{1}{T} - \frac{1}{T(25°C)}\right)} \tag{32}$$

5 Temperature sense amplifier

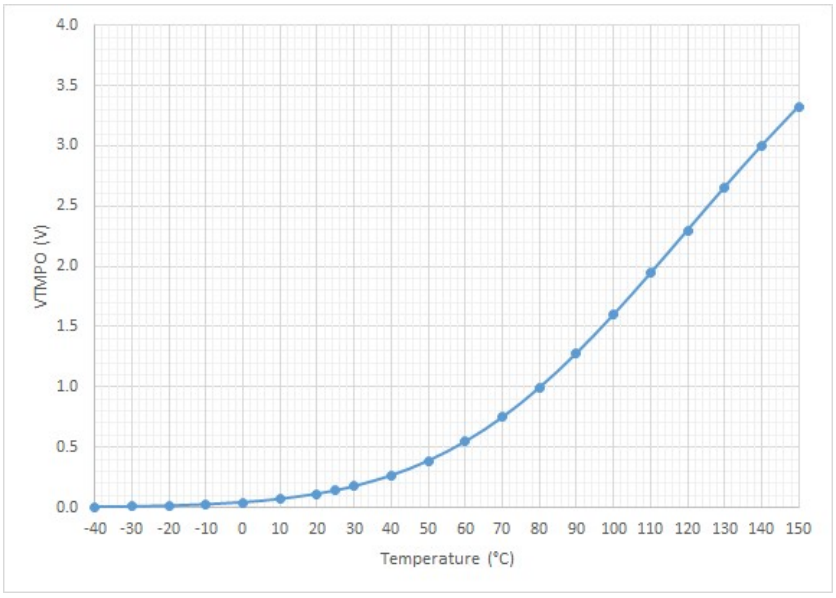


Figure 29 Example of curve V_{TMPO} [V] = $f(T$ [°C]) for V_{EN} = 3.3 V

The automated calculations can be found in the workbook [2], tab “Temperature sense set-up”.

6 External parts for driver protection

6.1 Protecting the VS node

The 2ED2410-EM's diode diagram shows us that the Zener diode between BC and GND is the critical path that should be protected against overvoltage in order to preserve the driver's integrity.

- Due to the boost converter between BC and VS, the VS node must be protected against spikes greater than $V_{BC\text{-}GND}$-$V_{BC(TH)MAX}$, giving 75 V-14 V = 61 V

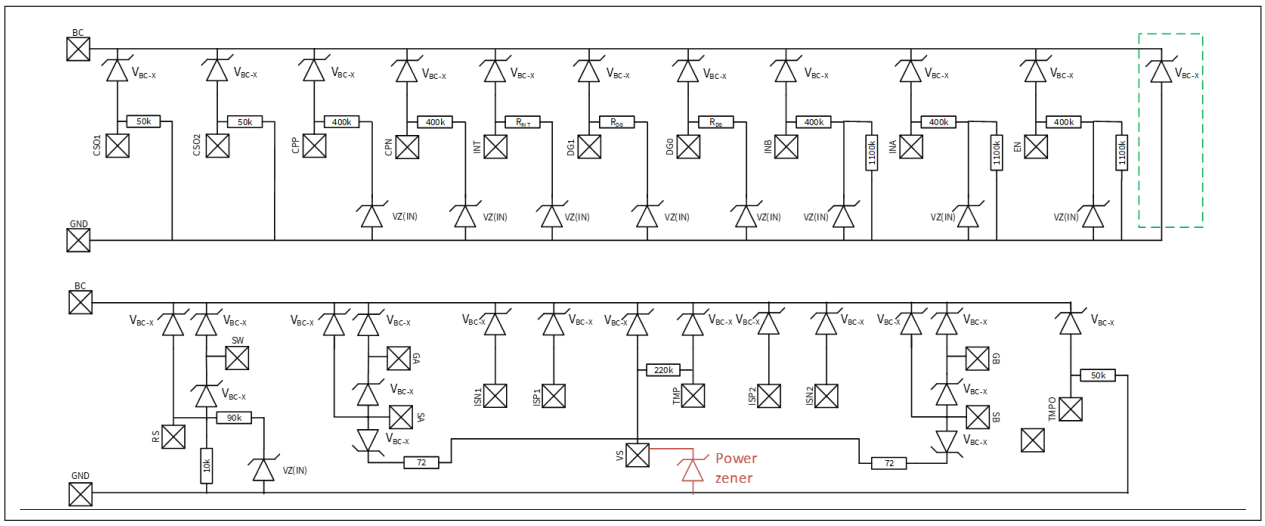


Figure 30 Diode diagram with BC-GND highlighted (green) and optional power diode (red)

- 1 W to 5 W power Zener is advised, when using MOSFET with a breakdown voltage equal or greater than 60 V. For example, this protection diode is not needed when using 40 V MOSFET, because the breakdown voltage of a 40 V MOSFET is below 61 V

6.2 ISO7637 transient pulses

***Note**: This section does not give a list of mandatory components that must be used in the application. It gives a list of possible solutions that can improve 2ED2410-EM behavior during EMC tests.*

Table 5 ISO7637 transient pulses counter-measures

Pin connection	Purpose	Counter-measure	PCB layout recommendation	Criticality
VS-GND	ISO7637 pulse 3b	C_{VS} = 3.3 µF/100 V min.	According to this chapter, Zener in Protecting the VS node can replace C_{VS}	Recommended

6.3 DPI protections

***Note**: This section does not give a list of mandatory components that must be used in the application. It gives a list of possible solutions that can improve 2ED2410-EM behavior during EMC tests.*

Table 6 DPI counter-measures

Pin connection	Purpose	Counter-measure	PCB layout recommendation	Criticality
SA-GND and SB-GND	DPI robustness	C_{SX} = 10 nF/50 V min. (12 V systems) or 100 V min. (24 V systems)	Between MOSFET source and GND plane (power)	Optional
TMPO-GND	DPI robustness	$C_{TMPO-GND}$ = 10 nF/10 V min.	Between TMPO pin and GND	Optional
ISPx-BC and ISNx-BC	DPI robustness	$C_{ISXX-BC}$ = 1 nF/25 V min.	As close as possible from driver for shortest path to BC	Recommended
ISPx-BC and ISNx-BC	DPI robustness	$C_{ISXX-BC}$ = 1 nF/25 V min.	Located in between the split R_{ISXX} resistance	Recommended
CSOx-GND	dV/dt robustness	$C_{CSOX-GND}$ = 220 pF/15 V min.	As close as possible to the driver pin. A greater value would delay short-circuit reaction time	Recommended

***Note**: Details of 2ED2410-EM EMC tests can be delivered on-demand.*

In the figure below, two variations for implementation of the $C_{ISXX-BC}$ resistor are shown. At minima, configuration (a) should be observed for CSA1 and configuration (b) is recommended for noisy environments.

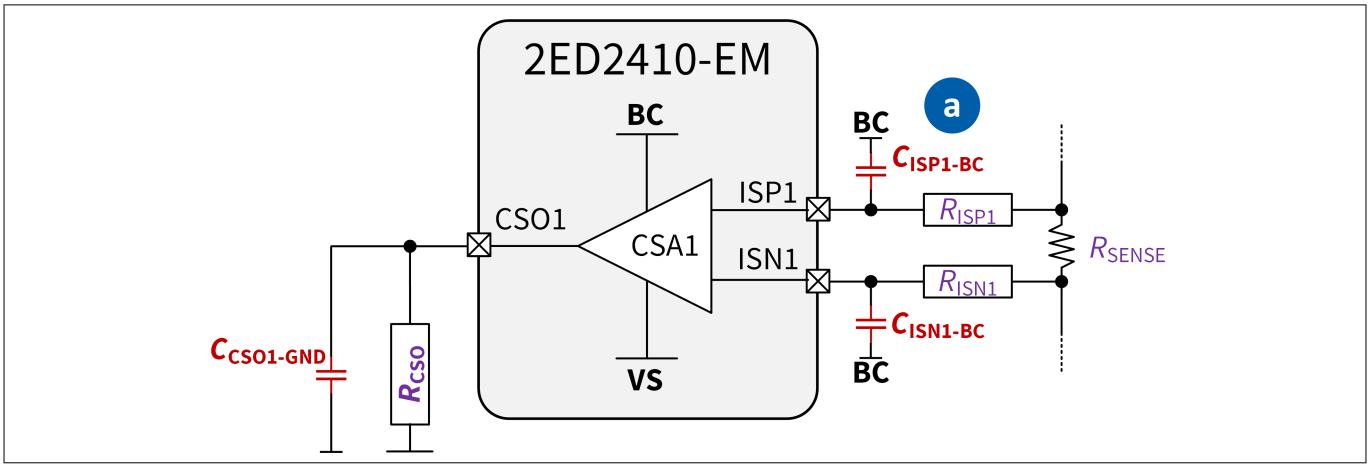


Figure 31 DPI recommendation minimal (a)

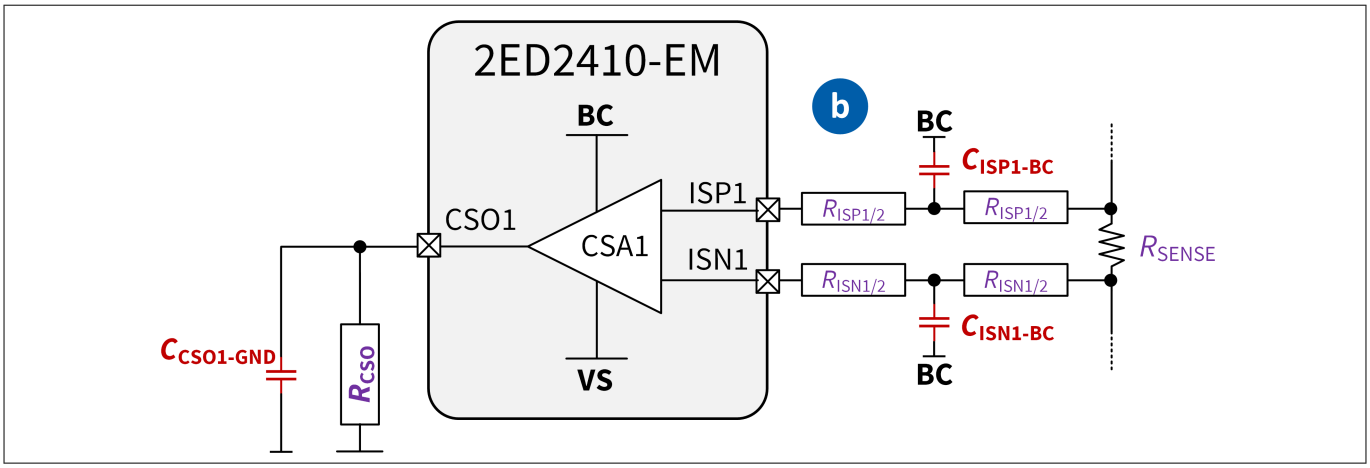


Figure 32 **Optimal (b) applied in this example to CSA1**

6.4 ESD components and layout recommendation

***Note**: This section does not give a list of mandatory components that must be used in the application. It gives a list of possible solutions that can fix a behavior, based on experiments and experience of the Infineon application and design team with gate drivers.*

For ESD automotive qualification, at device level, there are no additional components used. The bare driver passed the qualification HBM AEC-Q100 as specified in the datasheet [1] in PRQ-130.

For ESD module level ESD tests, options as depicted in the table below are available if the driver in a typical application does not comply with customer end test at module level.

Table 7 **ESD counter measures**

Pin connection	Purpose	Counter-measure	PCB layout recommendation	Criticality
GND	Improve BC-GND Zener diode robustness	R_{GND} = 10 -100 Ω	PCB trace as short as possible (to limit stray inductance) to GND PCB plane (analog). See ESD components and layout recommendation. This component is optional.	Optional
VS-GND	Improve module ESD robustness, dV/dt filtering	C_{VS} = 1-470 nF/50 V min. (12 V systems) or 100 V min. (24 V systems)	PCB trace as short as possible (to limit stray inductance) to GND PCB plane (power). See capacitor C2 in Figure 34.	Mandatory (100 nF typical value from datasheet [1] front page)

7 PCB layout recommendations

Attention**: **The PCB traces examples in this chapter are proposed layout solutions and are not mandatory. Those propositions are standard and final implementation depends on the customer layer stack and must be verified by the customer in the real application. Other layouts may achieve the same goals.

7.1 SW, BC and RS pin routing

In this sub-chapter a non-exhaustive list of advice in order to route the 2ED2410-EM amplifiers on the PCB in the correct manner, is given.

- SW is the main supply of the driver. The maximum current peak is 200 mA (I_{SW}, [PRQ-16]), therefore standard trace length on standard thickness is sufficient (35 µm, 0.254 mm/10 mil) for power dissipation considerations. However, in order to optimize boost converter efficiency, parasitic resistance of the trace must be kept to a minimum

***Note**: The SW pin must be routed separately from current senses and temperature senses strips, because the pulses in the range of hundreds of mA would highly disturb current sense reading and may cause an unintended SAFESTATE trigger in some situations. Only VS could be routed together from the main power line.*

Table 8 SW pin routing

Optimization	Power/Thermal reasons	Parasitic resistance	Parasitic capacitance
Width	According to PRQ-16 datasheet [1]. Standard width trace is generally sufficient	Augment width based on PCB thickness. Ideally, (R_L + R_{TRACE}) < 3Ω	Reduce width based on distance between top layer strip and embedded plane
Inductance choice	No specific adjustment	Choose an inductor with a parasitic resistor as small as possible. Ideally, (R_L + R_{TRACE}) < 3Ω	As close as possible to SW pin (<10 mm) to limit parasitic capacitance (<10 pF)

- If a diode is used in series with SW in order to block inverse current because of reverse battery situation, the diode voltage rating must be chosen greater than the driver maximum rating (75 V, see Absolute maximum ratings in datasheet [1]). A breakdown value of minimum 100 V is advised
- For BC tab, C_{BC} capacitor should be placed as close as possible from driver tab, ideally < 10 mm, to minimize stray inductance. Connection to VS must be direct with no capacitor to GND in between

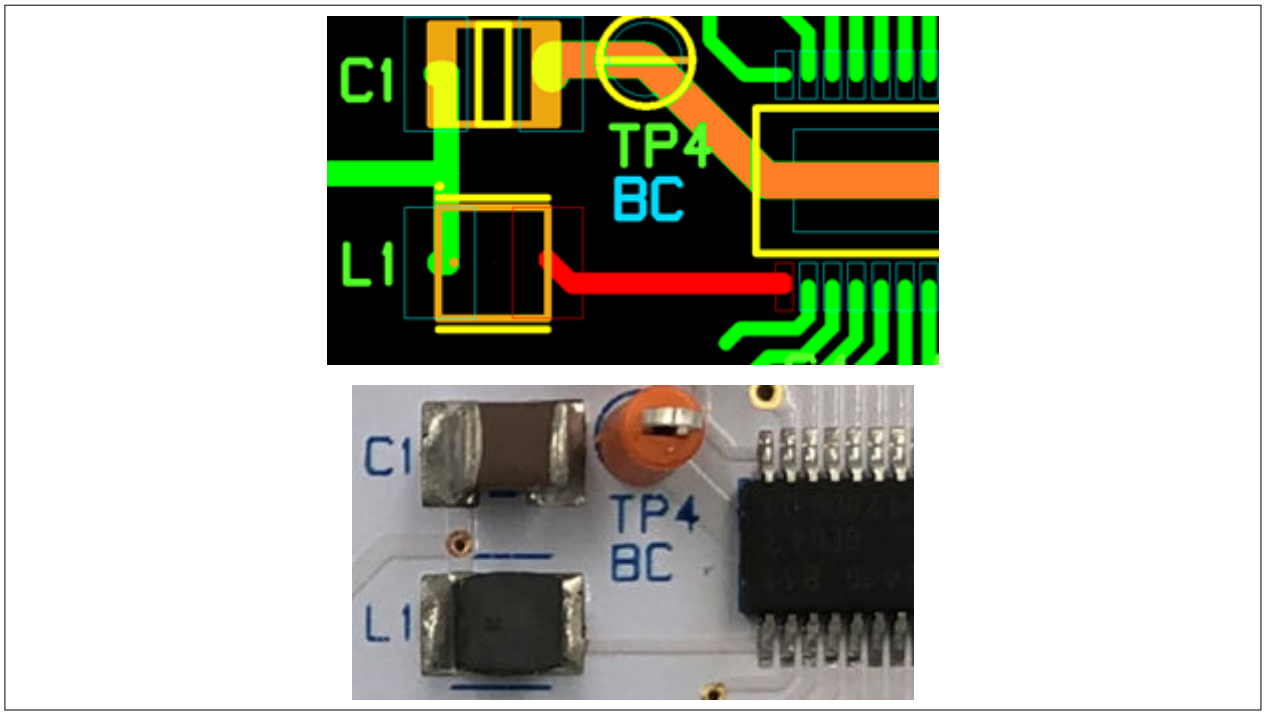


Figure 33 SW pin correct routing example (red) with VLS3015CX-101M-H and C_{BC} routing (orange)

- RS pin is the output of the boost converter. Therefore, connection to GND through the RS resistor should also be as short as possible. See ESD components and layout recommendation, same recommendation as the GND pin after the RS resistor

7.2 VS node routing

For protection purposes (ESD, ISO7637 transient disturbances), it may be needed to use capacitors and/or a Zener diode on the VS pin depending on the conditions. See Protecting the VS node.

However, it has to be noted that in order to supply the amplifiers correctly, the V_{BC}-V_S voltage must be kept stable [PRQ-339]. Therefore, any filtering on the VS pin should also apply to BC capacitor and *L* connection to VS node.

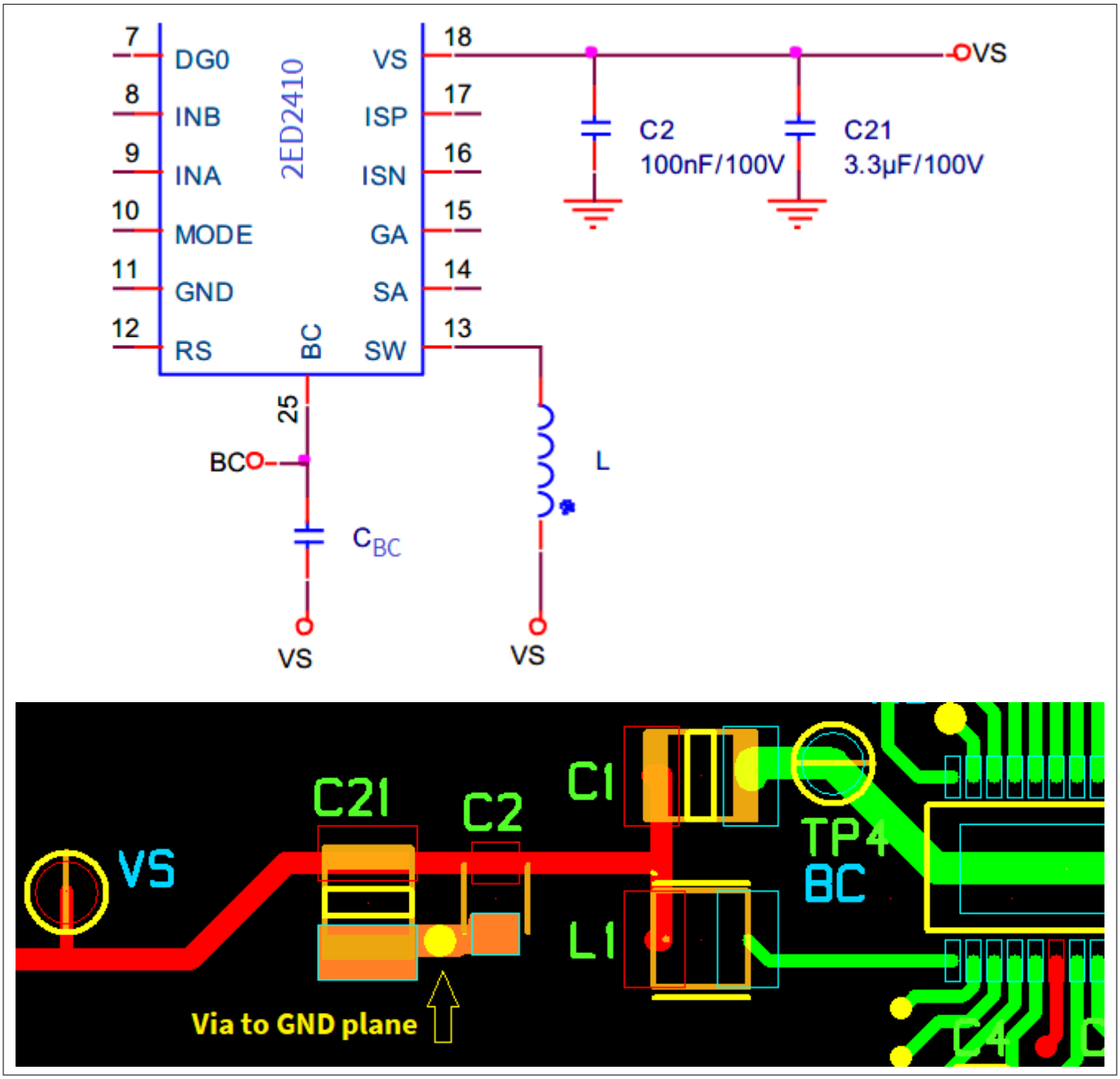


Figure 34 **VS pin schematic and correct routing example (red) with filtering caps and GND (orange)**

Because amplifiers are supplied between BC and VS, one of the two inputs of the amplifier must ideally be placed on the VS node for better amplifier performance.

7.3 Amplifiers routing

In this sub-chapter, a non-exhaustive list of advice in order to route the 2ED2410-EM amplifiers on the PCB in the correct manner is given.

- Amplifiers are supplied between BC and VS. See Chapter 7.2 in the datasheet [1] for details. Therefore, it is not advised to use capacitors between the amplifiers input pins and GND
- Output amplifier resistor R_{CSOx} [PRQ-326] and amplifier gain *G* [PRQ-317] parameters must be respected in the application

- Input and output amplifiers resistors are advised at 1% accuracy or better and ideally close to the device
- Ideally the two input traces should be routed together. The parasitic resistance of the traces must not influence the desired gain in the application. Straight lines are advised to avoid any antenna/loop effects
- To optimize the noise on current reading, the input amplifiers resistors $R_{ISPx/Nx}$ have to be minimal, as parasitic noise increases with resistance
- Even if R_{ISPx} or R_{ISNx} is electrically on the same node as VS and L1 connection, they must be routed separately to avoid interference from VS and SW pin current, that could create a parasitic voltage drop across R_{ISPx} or R_{ISNx} (R6 or R7 in the diagram below) and therefore perturbate amplifier operation

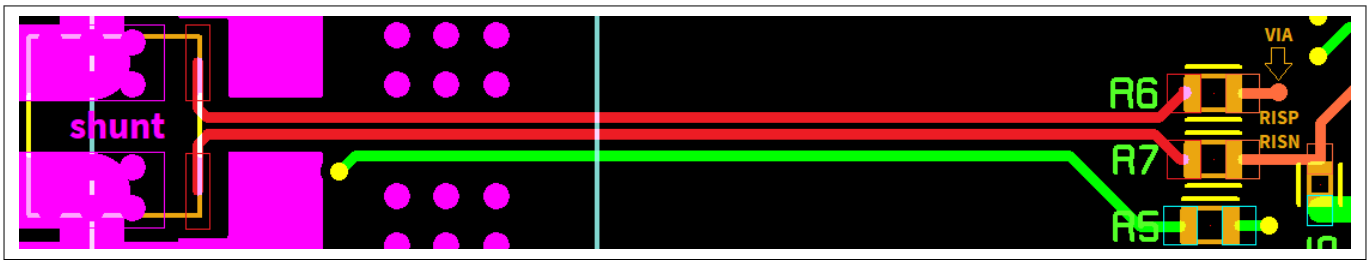


Figure 35 **Example of amplifier correct routing from shunt resistor (red) and from input resistance to pins (orange)**

***Note**: Vias can be copper-filled. In most cases, it can be assumed that their internal resistance does not impact the current sense accuracy, as it would be negligible in comparison to R_{ISXX} resistances.*

7.4 GND pin

The GND pin trace should be as short as possible to a GND plane or to the GND connector. If a GND plane is used, located below the driver, it is good practice to separate signal GND from power GND (for example if a freewheeling diode is used on PCB where the 2ED2410-EM is located).

A small, optional, resistor (see DPI protections) could be used on the GND pin to increase *electrostatic discharge (ESD)* module robustness or BCI robustness in case of failures, or for safety reasons (see 2ED2410-EM Safety Application Note). In this case, again, the path should be as shorter as possible.

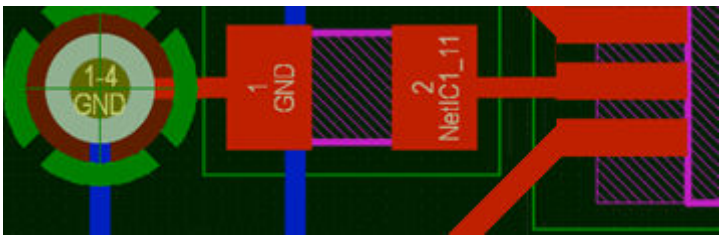


Figure 36 **Example of GND correct routing with the optional additional resistor and connection to GND plane with standard via (green)**

8 Quiescent current example

This chapter shows the formulas for computing quiescent current and shows real-life examples of consumption in 4 operating modes of the 2ED2410-EM driver.

- Power supply of the driver is a boost DC-DC converter with integrated diode and switch (K1 MOSFET, see Figure 1)
- The quiescent current of 2ED2410-EM is then related to the efficiency of the boost converter and to the battery voltage
- The efficiency depends on the boost converter external components

For this reason, quiescent current is measured from the battery line rather than the ground connection of the device.

- Due to the variety of choices of external components, Infineon cannot commit on a specific quiescent current value from the battery
- Infineon can only commit to the driver consumption itself, measured on pins BC and VS in production test and characterization. See datasheet [1] Chapter 4.6 for the current consumption parameters

8.1 SLEEP mode

In SLEEP mode, the boost converter is not active. The quiescent current can be measured on the GND+RS pin plus the source SA or SB pin depending on connection in application.

$$I_{q(SLEEP)} = I_{GND+RS(SLEEP)} + I^{1)}{}_{SA(SLEEP)} + I^{1)}{}_{SB(SLEEP)}$$

[1] To be considered only if SA or SB is below VS voltage.

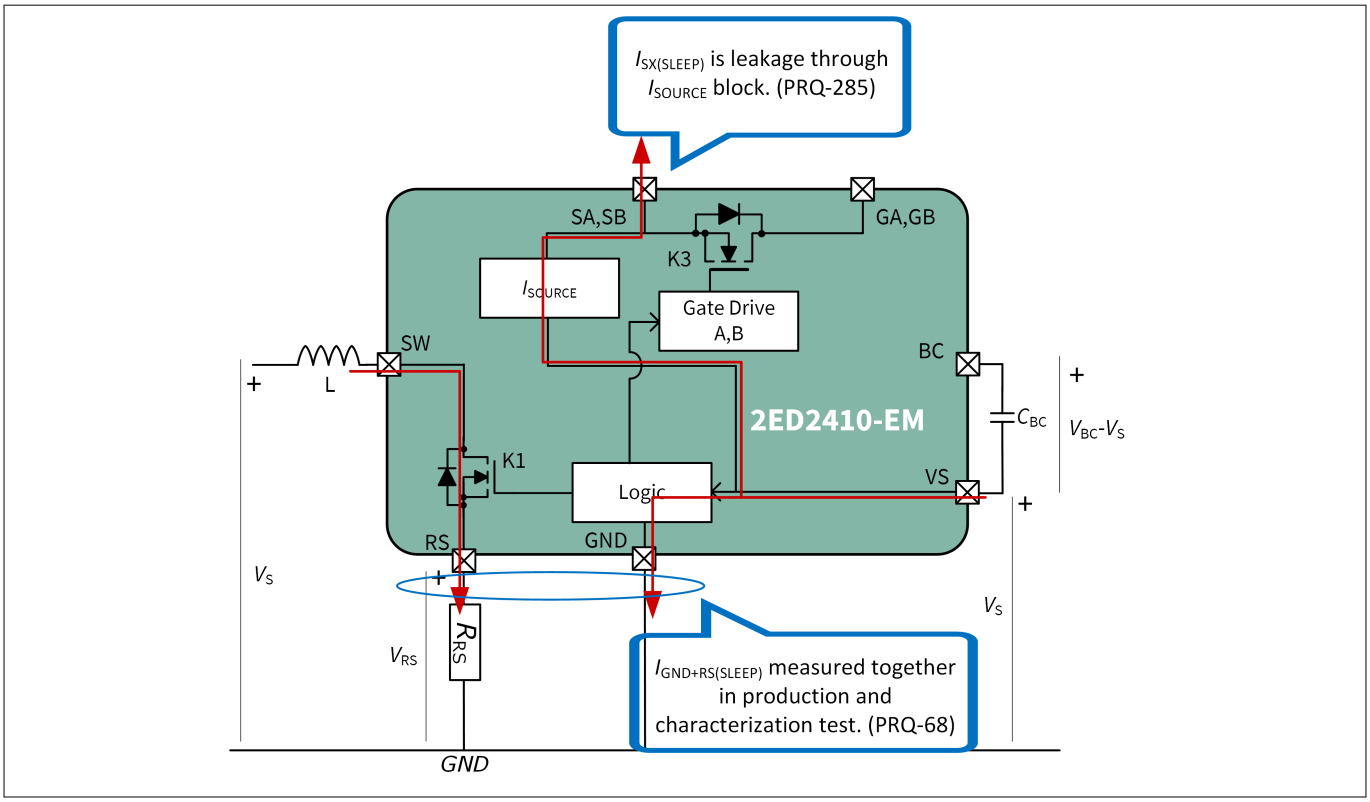


Figure 37 Current paths in SLEEP mode

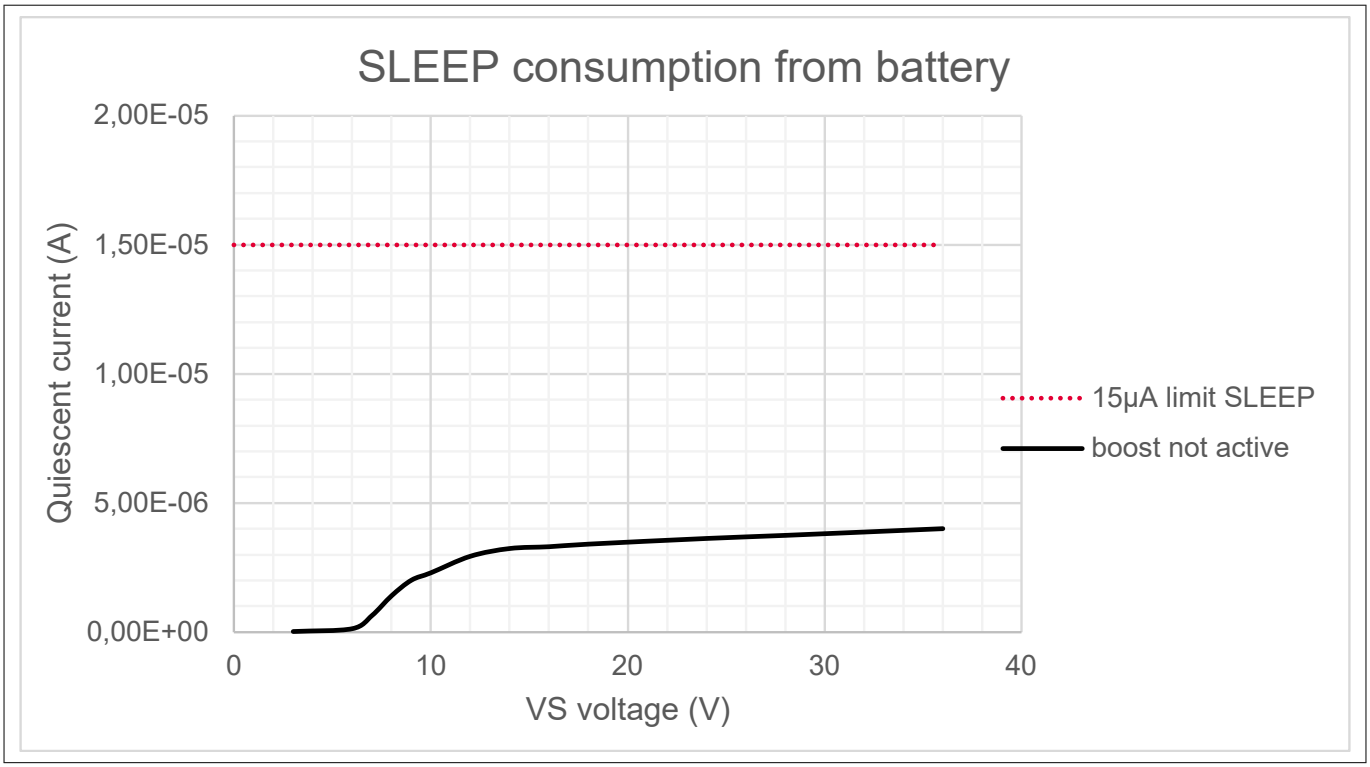


Figure 38 Quiescent current measurement of 2ED2140-EM in SLEEP mode @25°C (boost converter not active)

8.2 IDLE mode

In IDLE mode, the boost converter is active. However, amplifiers and comparators, the main contributors to current consumption, are not active. External MOSFETs are OFF.

Equation (34) is the general efficiency equation applied to our boost converter:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_{BC} \times V_{BC}}{\overline{I_{SW}} \times V_S} \tag{33}$$

The current drawn from the battery in IDLE is the sum of the current pulled by the boost input (SW) and VS pin.

$$I_{q(IDLE)} = I_{BAT} = \overline{I_{SW}} + I_{VS(IDLE)} \tag{34}$$

Combining Equation (34) and Equation (35) gives:

$$I_{q(IDLE)} = \frac{I_{BC(IDLE)} \times V_{BC}}{\eta \times V_S} + I_{VS(IDLE)} \tag{35}$$

There is no easy way to compute efficiency; therefore, the online tool [4] or excel calculation workbook [2] can be used for estimation.

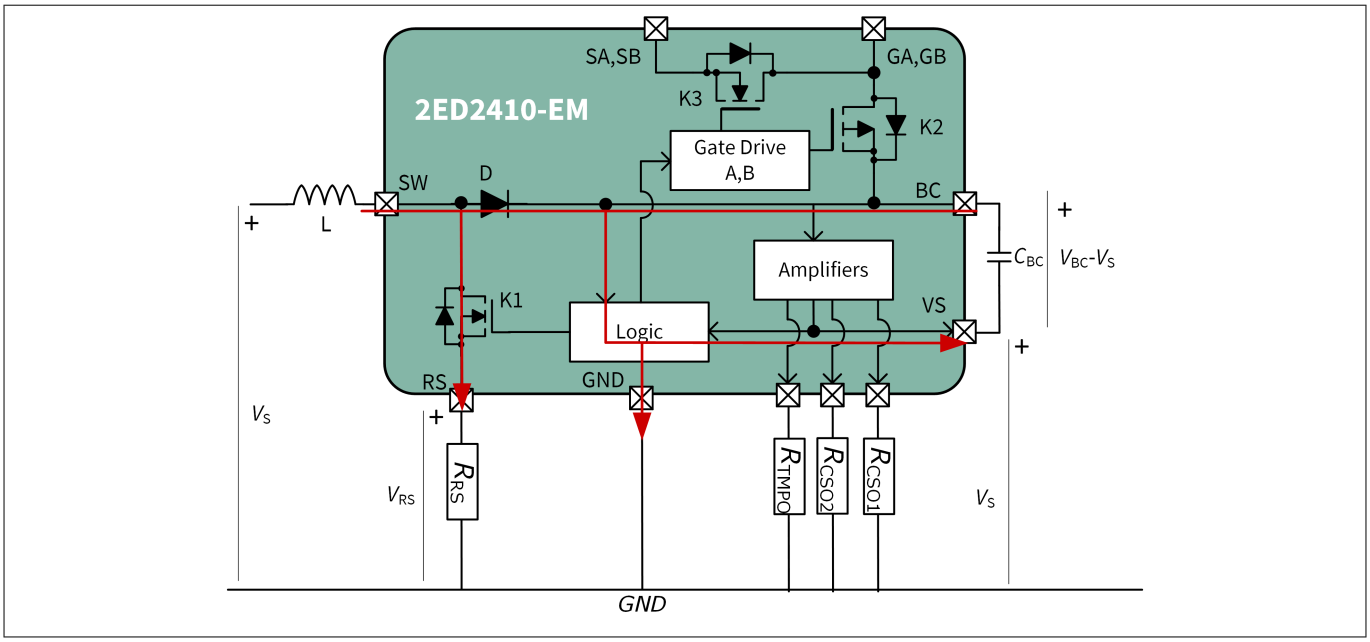


Figure 39 Current paths in IDLE mode

The graph below shows the correlation between theoretical calculation and measurement from the evaluation board. It is measured in open load to avoid interference of the I_{SOURCE} function (see Chapter 6 from the datasheet [1]).

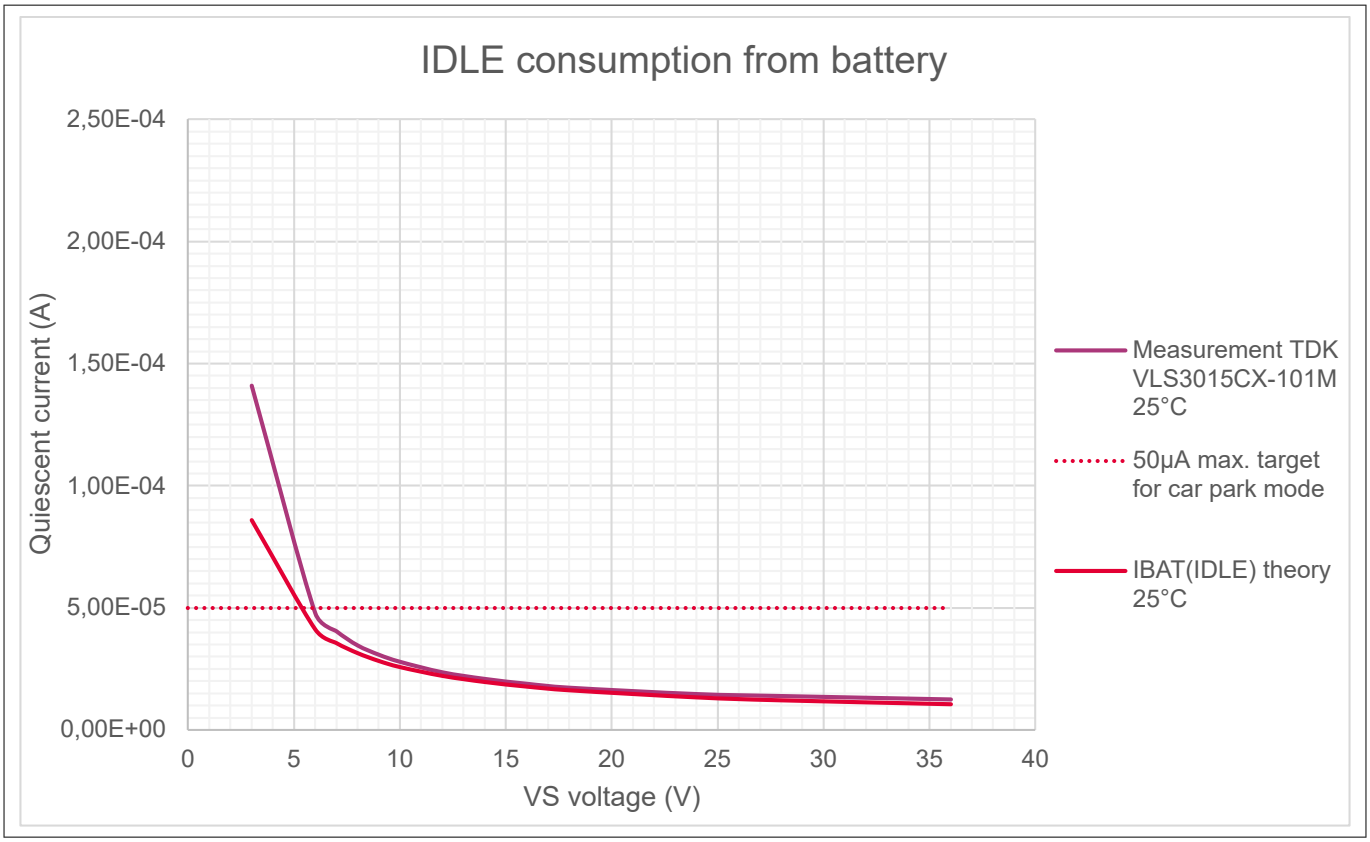


Figure 40 Quiescent current of 2ED2410-EM in IDLE mode @25°C, *open load*, using TDK VLS3015CX-101M-H and R_{RS}=10 Ω

8.3 ON/SAFESTATE mode

In ON and SAFESTATE mode, the boost converter is active. External MOSFET are turned-on. Amplifiers, the main contributors to current consumption, are also active. Additionally, current going through the amplifiers has to be added, including current sense amplifiers 1 and 2, and temperature amplifier (unless the amplifier is disabled, see Chapter 7.2 and 7.3 in the datasheet).

Therefore, the current needed by the driver from the battery is:

$$I_{q(ON)} = I_{BAT} = \overline{I_{SW}} + I^{1)}{}_{CSA1} + I^{1)}{}_{CSA2} + I^{2)}{}_{TMPA} + I_{VS(ON)}$$

[1] to be considered only if the amplifier is active and the current flowing through the sense

[2] to be considered only if temperature amplifier is active

Where:

$$I_{CSAx} = \frac{V_{CSOx}}{R_{CSOx}} \tag{36}$$

$$I_{TMPA} = \frac{V_{ENABLE}}{k_{TMP} \times (R_{NTC} + R_{TMP})} \tag{37}$$

Combining Equation (34), Equation (37), and Equation (38) in Equation (36) gives:

$$I_{q(ON)} = \frac{I_{BC(ON)} \times V_{BC}}{\eta \times V_S} + I_{VS(ON)} + \frac{V_{SENSE1}}{R_{IS1}} + \frac{V_{SENSE2}}{R_{IS2}} + \frac{V_{ENABLE}}{k_{TMP} \times (R_{NTC} + R_{TMP})} \tag{38}$$

There is no easy way to compute efficiency; therefore, a tool will be provided at product release; in the meantime, excel calculation workbook can be used for estimation.

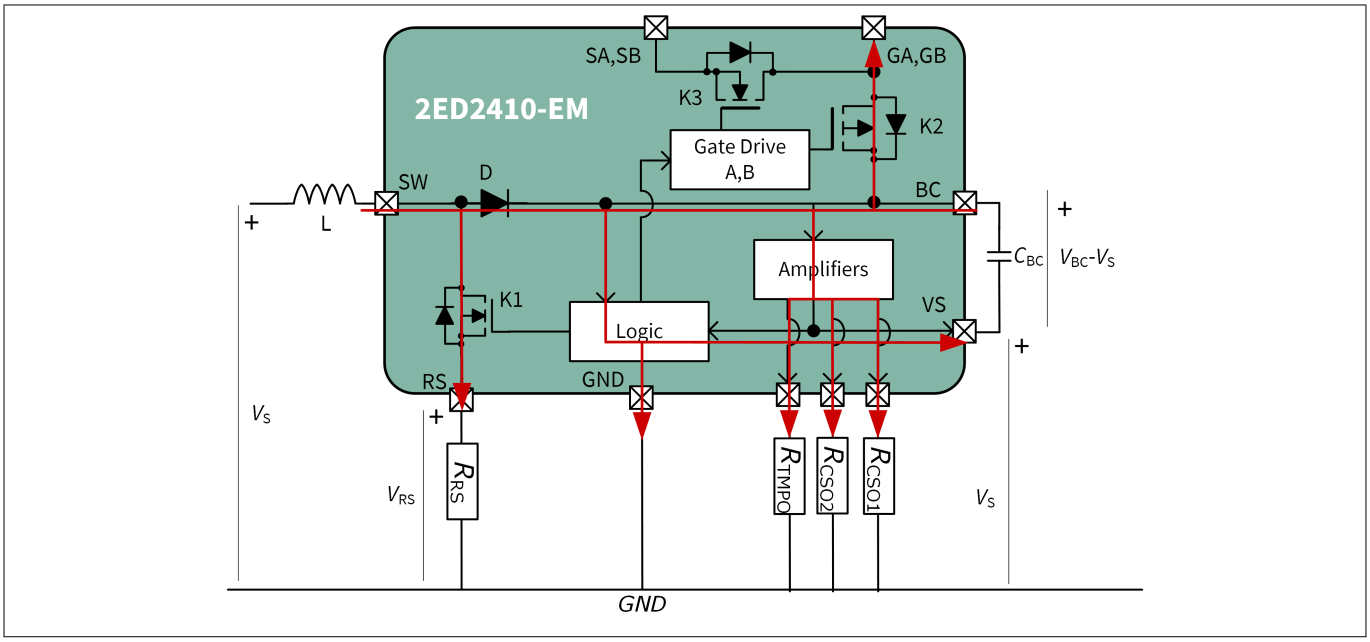


Figure 41 Current paths in ON/SAFESTATE mode

The graph below shows the correlation between theoretical calculation and measurement from evaluation board, in open load so no current is flowing through the sense element.

8 Quiescent current example

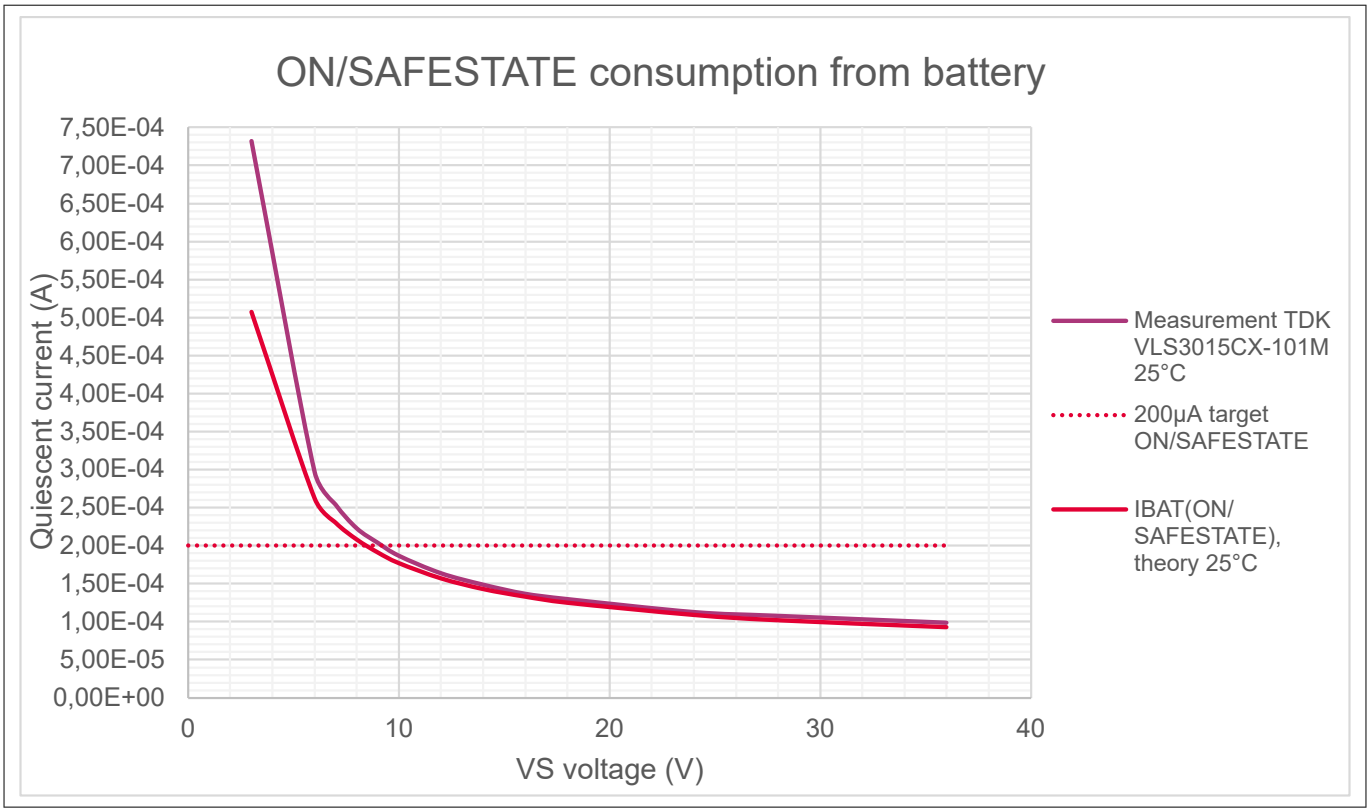


Figure 42 **Quiescent current of 2ED2410-EM in ON and SAFESTATE modes @25°C, *open load*, using TDK VLS3015CX-101M-H and R_{RS}=10 Ω**

9 References

[1] Infineon: 2ED2410-EM Datasheet Rev.3.00; Link from infineon website

[2] Infineon Getting started workbook Rev.3.30; Excel workbook from BP_myICP

[3] Infineon 2ED2410-EM Safety application note Rev.02.20

[4] Infineon Smart Power Switches EiceDRIVER™ 2ED2410-EM Tool; https://softwaretools.infineon.com/tools/com.ifx.tb.tool.eicedrivertool

Glossary

ADC

analog-to-digital converter (ADC)

BC

boost converter (BC)
A boost converter is a DC-to-DC power converter that steps up voltage from its input (supply) to its output (load). It is a class of switched-mode power supply (SMPS) containing at least two semiconductors (a diode and a transistor) and at least 1 energy storage element: a capacitor, inductor, or the two in combination.

COMP

comparator (COMP)
Compares an input voltage against a second input voltage.

CP

charge pump (CP)
A kind of DC-to-DC converter that uses capacitors for energetic charge storage to raise or lower voltage.

CSA

current-sense amplifier (CSA)
Special-purpose amplifiers that output a voltage proportional to the current flowing in a power rail. They utilize a "current-sense resistor" to convert the load current in the power rail to a small voltage, which is then amplified by the current-sense amplifiers.

EMC

electromagnetic compatibility (EMC)
The ability of electrical equipment and systems to function acceptably in their electromagnetic environment, by limiting the unintentional generation, propagation and reception of electromagnetic energy which may cause unwanted effects such as electromagnetic interference (EMI) or even physical damage in operational equipment.

ESD

electrostatic discharge (ESD)

A sudden and momentary flow of electric current between two electrically charged objects caused by contact, an electrical short or dielectric breakdown.

GND

ground (GND)

GPIO

general purpose input output (GPIO)

microcontroller

microcontroller
A small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals.

NTC

negative temperature coefficient (NTC)

A term used in thermistors to describe how resistance decreases as temperature increases.

PCB

printed circuit board (PCB)

A board that mechanically supports and electrically connects electronic components using conductive tracks, pads, and other features etched from copper sheets laminated onto a non-conductive substrate.

PTC

positive temperature coefficient (PTC)

A term used in thermistors to describe how resistance increases as temperature increases.

UVLO

undervoltage lockout (UVLO)

An electronic circuit used to deactivate functions of an electronic device if the voltage drops below a threshold.

Revision history

Document version	Date of release	Description of changes
Rev. 3.00	2025-12-22	• Chapter 3 “Enhanced functions and external components” updated - Added information for capacitive load pre-charge - Added recommendation for micro-interruption requirements • Chapter 4 “Current sense amplifier updated” - Added information for amplifier operating area - Updated “Minimum readable current” and “Current sense blind zone” subchapters - Added information for short circuit detection threshold sizing • Editorial changes
Rev. 2.01	2023-02-22	• Editorial changes • Chapter 1.4 renamed for clarity and Note added
Rev. 2.00	2022-12-13	• Updated Chapter 1.5.2 reverse batt protection in common source • Updated Chapter 3.1 pre-charge circuit • Updated Chapter 4.2 TMPO • Updated Chapter 5.2 DPI recommendations • Updated Chapter 6.1 SW routing • Added Chapter 4.1.1 current sense error • Updated Chapter 4.1.2 minimum readable current and Updated Chapter 4.1.3 current sense blind zone • Editorial changes
Rev. 1.00	2022-03-18	• First release

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