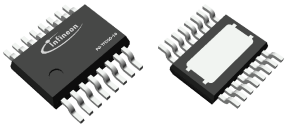
LITIX™ Interior

Features



RoHS

AEC Qualified

- 32-bit Arm® Cortex®-M23 core
  - One clock per machine cycle architecture
  - Single cycle multiplier
  - Hardware divider
- On-chip memory
  - 32 kB Flash (including 1000 TP memory)
  - 576 Bytes 1000 TP memory
  - 3 kB SRAM
  - Boot ROM for startup firmware and Flash routines
- On-chip oscillator and on-chip debug support via 2-wire SWD

Potential applications

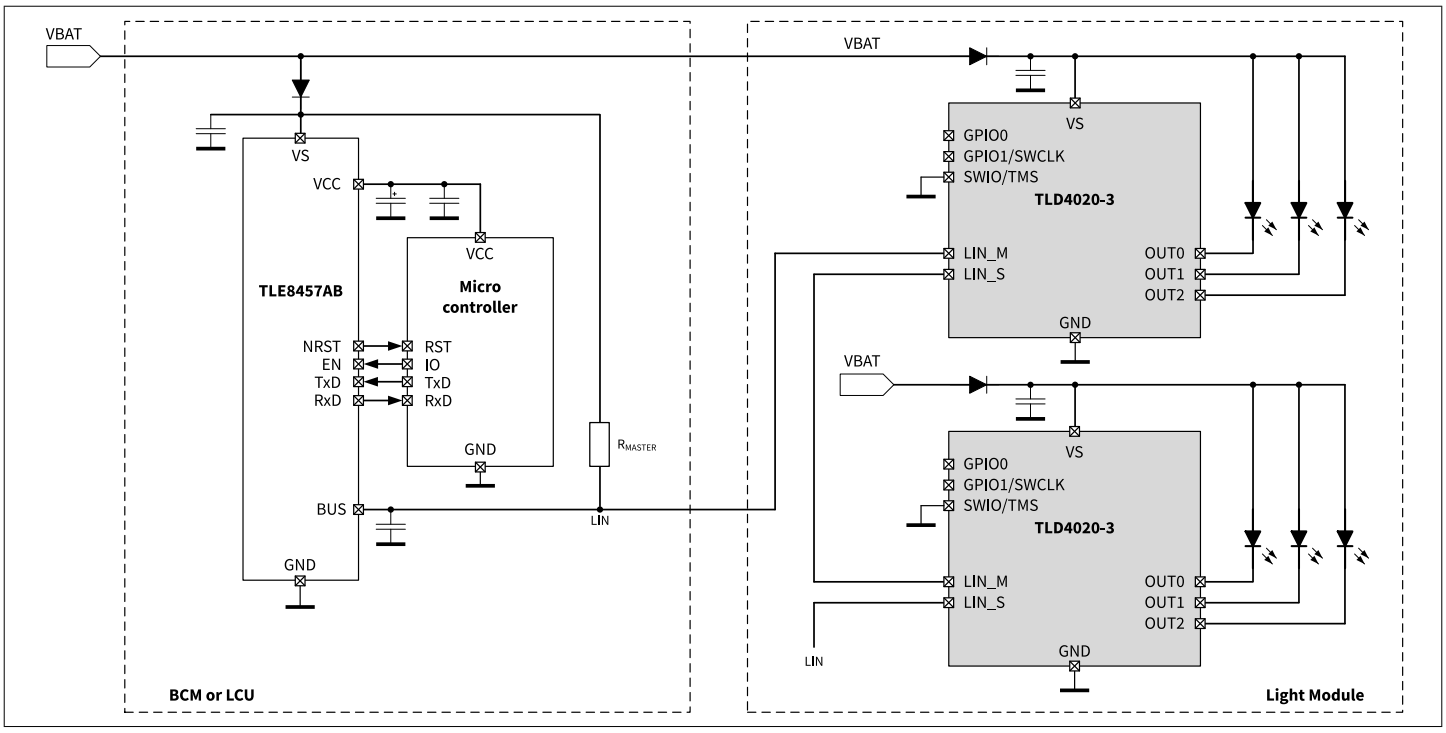
- Three channel LED driver for automotive interior lighting applications with LIN interface
- Contour lighting using a single light source with constant or slowly changing light patterns
- Functional and switch illumination
- Surface lighting requiring single LED

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100, Grade 1.

Description

The TLD4020-3ET is a three channel device with integrated and protected output stages. It is designed to control RGB LEDs with a current up to 51.5 mA as linear current sink (LCS). The power stages can be configured in parallel for higher load currents. Each individual power output stage is configurable via a 5-bit current set value. In total 3 independent and individual PWM configurations can be set. A LIN interface is used for programming (via bootloader), control and diagnostic feedback.



Product type	Package	Marking
TLD4020-3ET	PG-TFDSO-16	402

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1 Block diagram and terms

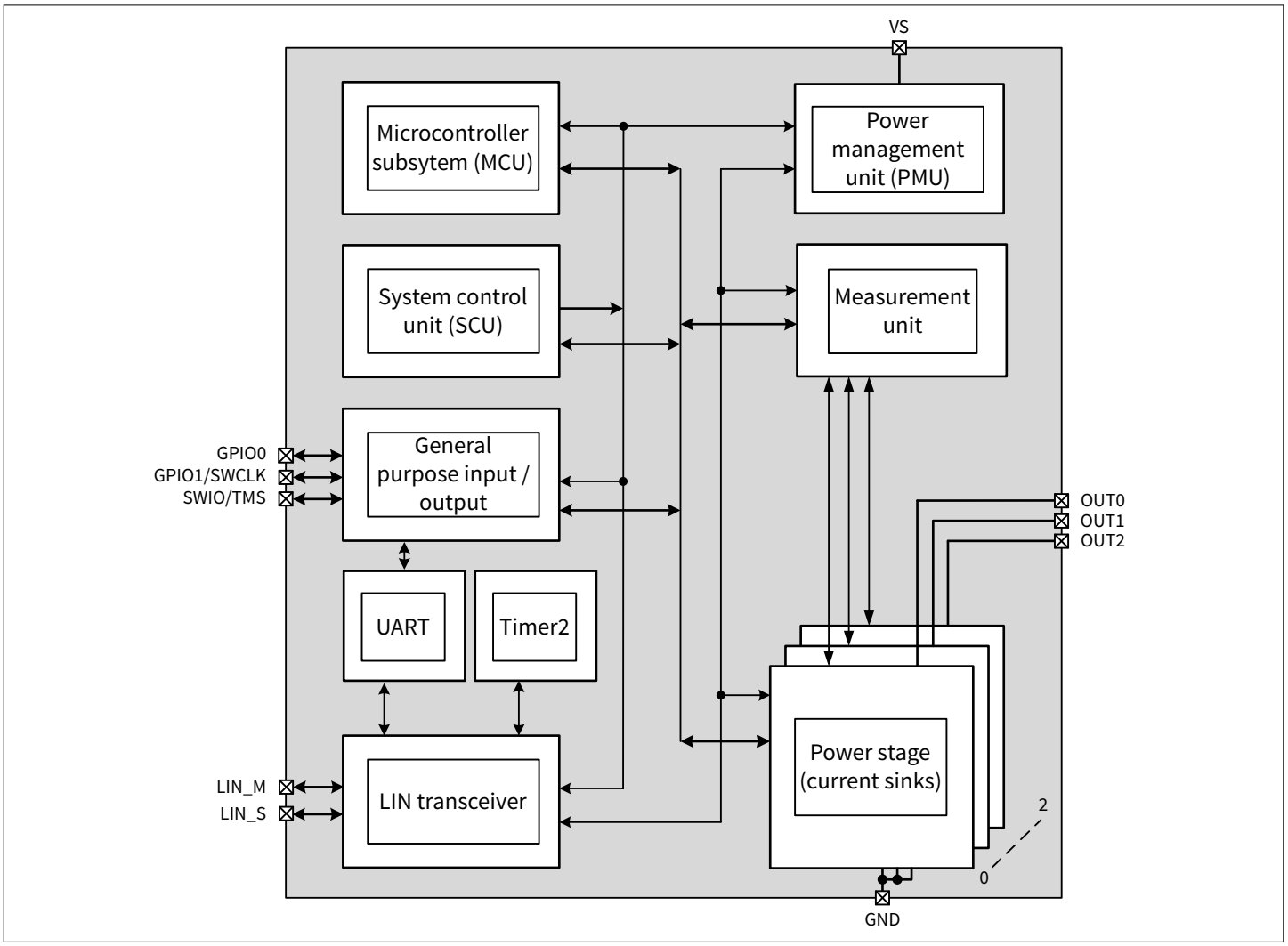


Figure 1 Block diagram of TLD4020-3ET

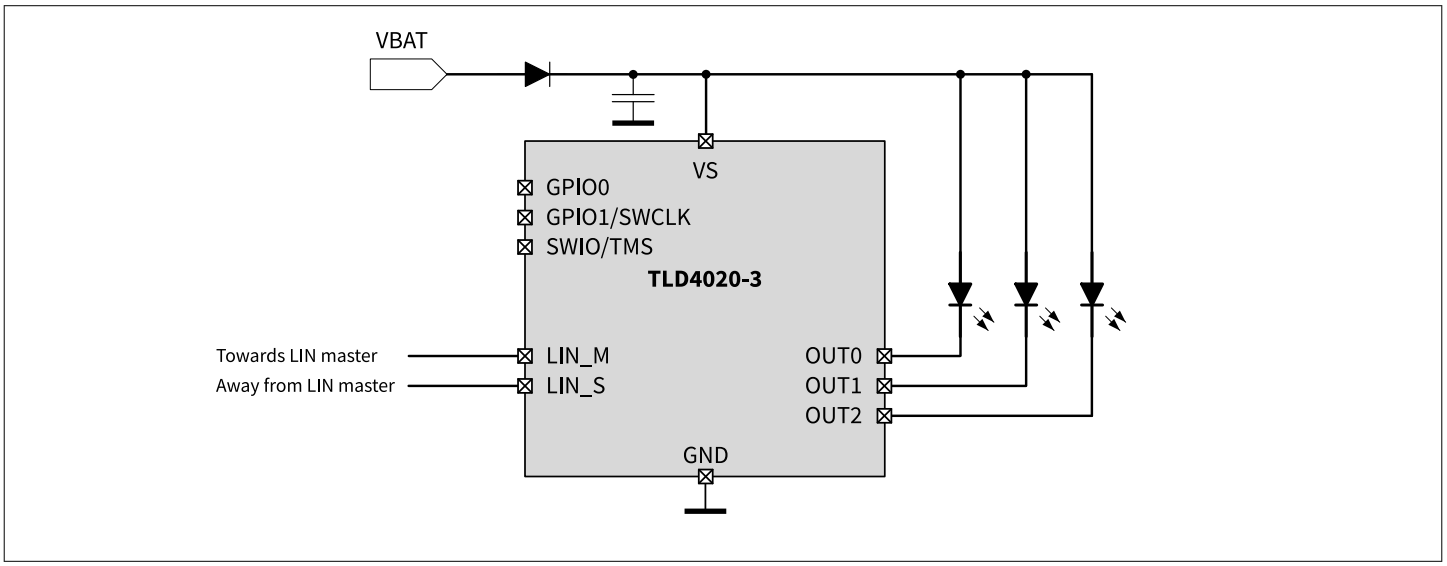


Figure 2 Application block diagram (simplified)

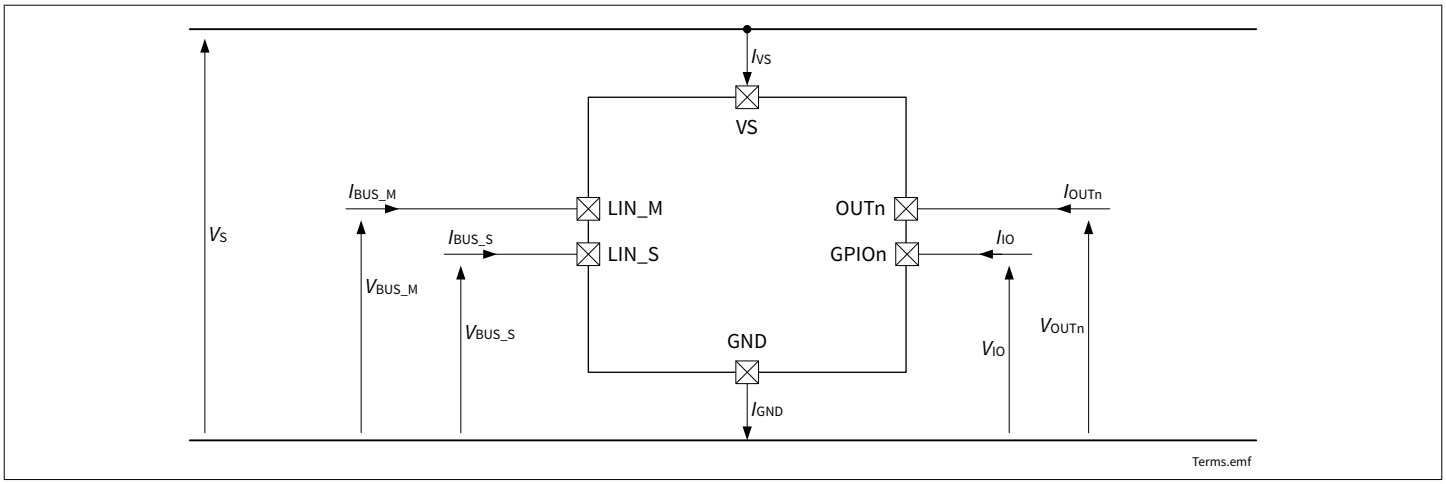


Figure 3 Terms and definitions

OUTn: n denotes the channel number from 0 to 2
GPIOn: n denotes the GPIO number from 0 to 1

2 General product characteristics

2.1 Absolute maximum ratings

Table 1 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive currents flowing as described in Chapter 1 (unless otherwise specified) [1)].

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Power supply voltage	V_S	-0.3	–	40	V	Suppressed load dump acc. to ISO16750-2	PRQ-142
Output pins							
Power output voltage	V_{OUT}	-0.3	–	40	V	–	PRQ-3150
Power output current	I_{OUT}	0	–	56.65	mA	–	PRQ-495
GPIO pins							
Voltage at pin GPIO0, GPIO1, TMS	V_{IO}	-0.3	–	5.5	V	–	PRQ-898
Current at pin GPIO0, GPIO1, TMS	I_{IO}	0	–	4	mA	–	PRQ-3162
LIN							
Voltage at pin LIN_M, LIN_S	V_{BUS}	-27	–	40	V	–	PRQ-1138
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-144
Ambient temperature	T_A	-40	–	125	°C	–	PRQ-145
ESD susceptibility							
ESD susceptibility all pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002	PRQ-150
ESD susceptibility LIN vs GND (HBM)	$V_{ESD(HBM)\_GND}$	-8	–	8	kV	ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002	PRQ-151
ESD susceptibility all pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011 Rev D	PRQ-152

(table continues...)

Table 1 (continued) Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive currents flowing as described in Chapter 1 (unless otherwise specified) [1)].

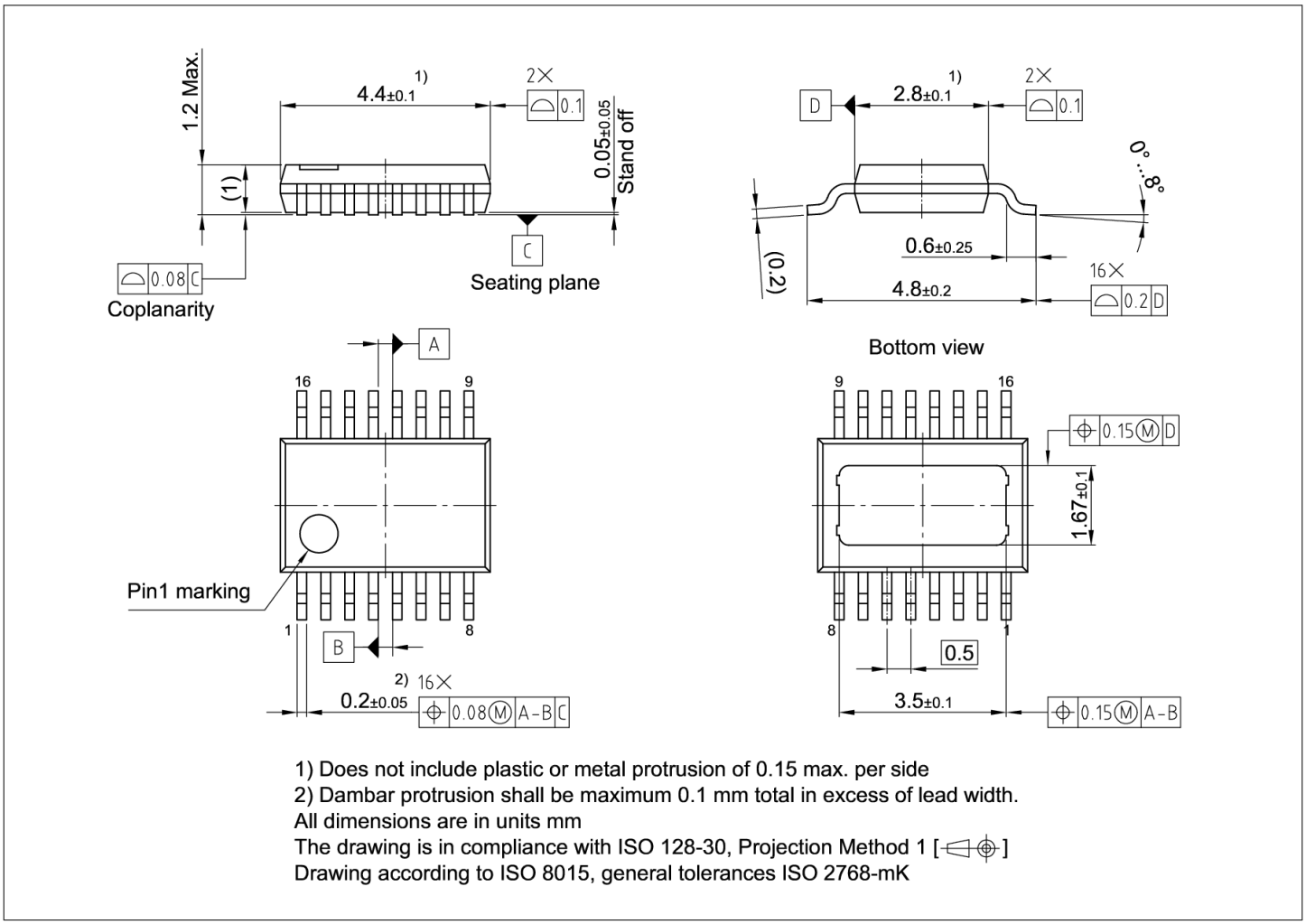
Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ESD susceptibility corner pins (CDM)	$V_{ESD(CDM)\_CR}$	-750	–	750	V	ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011 Rev D	PRQ-153

1) Not subject to production test - specified by design

***Note**:* *1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3 Package dimensions



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⇿]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 4 Package outline PG-TFDSO-16

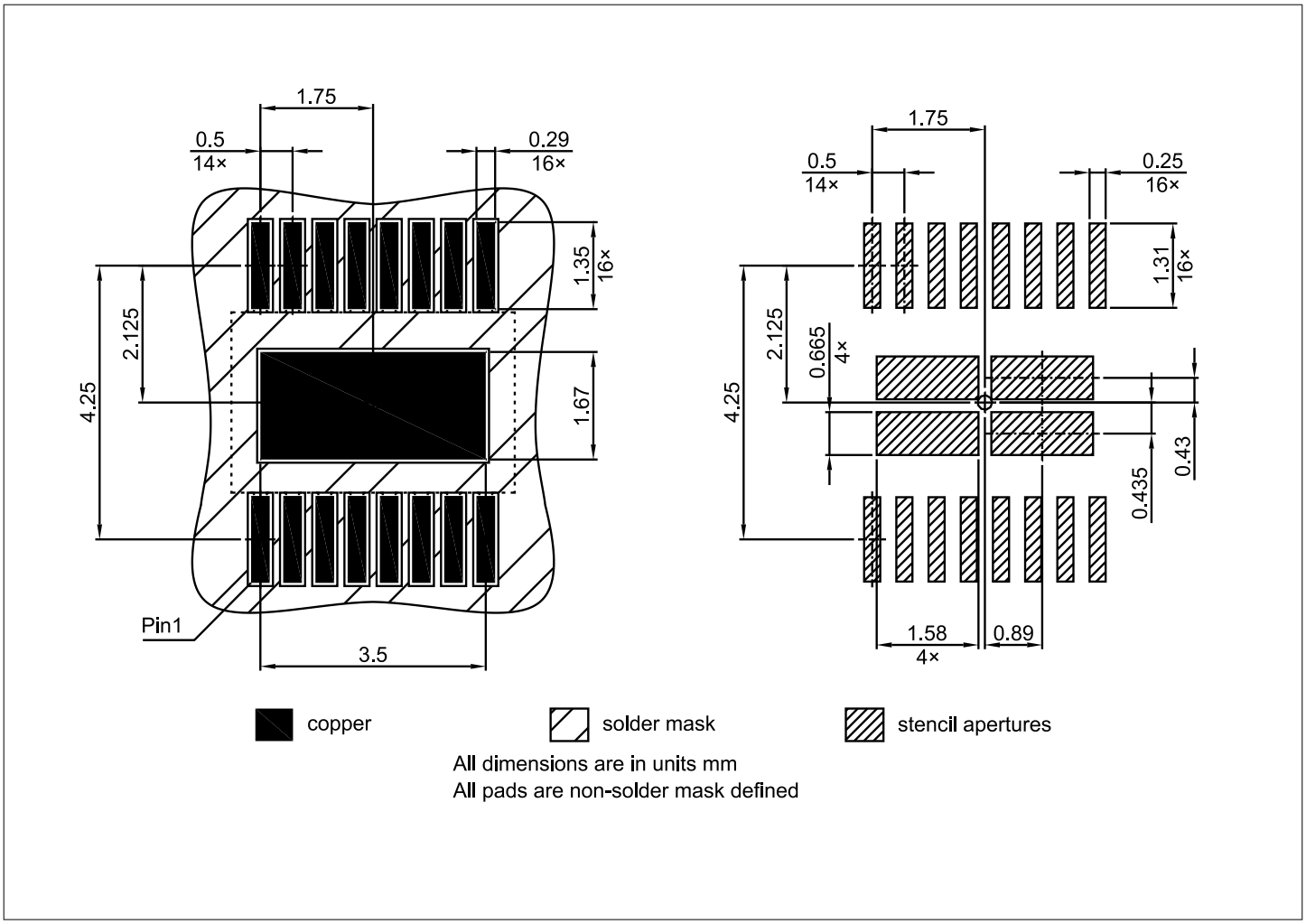


Figure 5 PG-TFDSO-16 package pads and stencil

Note: ***Green product (RoHS compliant)***

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).
For further information on packages, please visit our website: https://www.infineon.com/packages

Revision history

Document version	Date of release	Description of changes
Rev. 1.00	2025-05-09	• Initial document release

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