Product Qualification Report (PQR)

# S25FL128SAGBHB203

## Package: PG-TFBGA-24

All reliability stress tests according to AEC-Q100 Rev. J1 (Grade 2) are assessed as PASS. The data outlined in this document may reference existing qualification results of similar products.

**Table 1 Reliability stress tests.**

| # | Test description | Abbr. | Condition | Duration | Min. # of lots × sample size | Result |
|---|---|---|---|---|---|---|
| **Test group A – accelerated environment stress tests** | | | | | | |
| **A1** | **Preconditioning**<br>*JEDEC JESD22-A113, J-STD-20 (MSL)* | PC | MSL 3 | 3 × reflow 260°C | Before A2, A3, A4 | Pass |
| **A2** | **Highly accelerated temperature and humidity stress**<br>*JEDEC JESD22-A110* | HAST | 110°C 85% RH | 264 h | 3 × 77 | Pass |
| **A3** | **Unbiased highly accelerated temperature and humidity stress**<br>*JEDEC JESD22-A118* | UHAST | 130°C 85% RH | 96 h | 3 × 77 | Pass |
| **A4** | **Temperature cycling**<br>*JEDEC JESD22-A104* | TC | -65°C to 150°C | 500× | 3 × 77 | Pass |
| **A5** | **Power temperature cycling**<br>*JEDEC JESD22-A105* | PTC | Power dissipation < 1W | | | n.a |
| **A6** | **High temperature storage life**<br>*JEDEC JESD22-A103* | HTSL | 150°C | 1000 h | 1 × 45 | Pass |
| **Test group B – accelerated lifetime simulation tests** | | | | | | |
| **B1** | **High temperature operating life**<br>*JEDEC JESD22-A108* | HTOL | 125°C Vcc max | 1000 h | 3 × 77 | Pass |
| **B2** | **Early life failure rate**<br>*AEC Q100-008* | ELFR | 125°C Vcc max | 48 h ≤ t ≤ 168 h | 3 × 800 | Pass |
| **B3** | **NVM endurance, data retention, and operational life**<br>*AEC Q100-005* | EDR + HTOL | 125°C | 100000 × 1000 h | 3 × 77 | Pass |
| **B3** | **NVM endurance, data retention, and operational life**<br>*AEC Q100-005* | EDR + HTSL | 125°C | 100000 × 1000 h | 3 × 77 | Pass |

| # | Test description | Abbr. | Comment | Result |
|---|---|---|---|---|
| **Test group C – package assembly integrity tests** | | | | |
| **C1** | **Wire bond shear**<br>*AEC Q100-001, AEC Q003* | WBS | Covered by package platform qualification and production monitoring | Pass |
| **C2** | **Wire bond pull**<br>*MIL-STD883 Method 2011, AEC Q003* | WBP | Covered by package platform qualification and production monitoring | Pass |
| **C3** | **Solderability**<br>*JEDEC J-STD-002* | SD | Covered by package platform qualification and production monitoring | Pass |
| **C4** | **Physical dimensions**<br>*JEDEC JESD22-B100 and AEC Q003* | PD | Covered by package platform qualification and production monitoring | Pass |
| **C5** | **Solder ball shear**<br>*AEC Q100-010, AEC Q003* | SBS | Covered by package platform qualification and production monitoring | Pass |
| **C6** | **Lead integrity**<br>*JEDEC JESD22-B105* | LI | For through-hole devices only | n.a |
| **C7** | **Bump shear test**<br>*JEDEC JESD22-B117, AEC-Q003* | BST | For flip-chip technology only | n.a |

| # | Test description | Abbr. | Comment | Result |
|---|---|---|---|---|
| **Test group D – die fabrication reliability tests** | | | | |
| Die fabrication reliability tests like EM, TDDB, HCI, BTI, SM are covered by wafer technology qualification | | | | Pass |
| **Test group E – electrical verification tests** | | | | |
| **E1** | **Pre- and post-stress function parameter** | TEST | Performed for all qualification parts | Pass |
| **E2** | **ESD human body model**<br>*AEC Q100-002* | ESD HBM | Class 2 ( 2000 V to ＜ 4000 V) | Pass |
| **E3** | **ESD charged device model**[1)]<br>*AEC Q100-011* | ESD CDM | Class C2a ( 500 V to ＜ 750 V, corner pins ≥ 750 V ) | Pass |
| **E4** | **Latch-up**<br>*AEC Q100-004* | LU | Class II | Pass |
| **E5** | **Electrical distributions**<br>*AEC Q100-009, AEC Q003* | ED | Test at room, hot, cold temperature | Pass |
| **E6** | **Fault grading**<br>*AEC Q100-007* | FG | | n.a |
| **E7** | **Characterization**<br>*AEC Q003* | CHAR | | Pass |
| **E9** | **Electromagnetic compatibility**<br>*SAE J1752/3 – Radiated Emissions* | EMC | Data will be provided on request | Pass |
| **E10** | **Short circuit characterization**<br>*AEC Q100-012* | SC | For smart power devices only | n.a |
| **E11** | **Soft error rate**<br>*JEDEC JESD89-1 (un-accelerated)*<br>*JEDEC JESD89-2/-3 (accelerated)* | SER | Covered by wafer technology qualification | Pass |
| **E12** | **Lead (Pb) free**<br>*AEC Q005* | LF | Covered by package platform qualification | Pass |
| **Test group F – defect screening tests** | | | | |
| **F1** | **Process average testing**<br>*AEC Q001* | PAT | Implemented in production test | Pass |
| **F2** | **Statistical bin / yield analysis**<br>*AEC Q002* | SBA | Implemented in production test | Pass |
| **Test group G – cavity package integrity tests** | | | | |
| Cavity package integrity tests like MS, VFV, CA, GFL, DROP, LT, DS, IWV apply for hermetic packages only | | | | n.a. |
| **Components using copper (Cu) wire interconnections** | | | | |
| **AEC Q006** qualification | | | | Pass |

For further information and documentation please refer to the product homepage:
https://www.infineon.com/part/S25FL128SAGBHB203

[1)] voltage refers to test condition (TC) mentioned in the standard

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