Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Cypress Semiconductor
Product Qualification Report

QTP# I000005
October 2013

0.35um Technology, CSM Fab 2	
CY7B9950	2.5V / 3.3V, 200MHz High Speed Multi-Phase PLL Clock Buffer
CY2DP818*	3.3V, 1:8 Clock Fanout Buffer
CY28346	3.3V, Clock Synthesizer with Differential CPU Out- put
CY29946 CY29947 CY29948	2.5V / 3.3V, 200MHz, 1:9,1:10, 1:12 Clock Distribution Buffer
CY29972 CY29973	3.3V, 125MHz Multi-Output Zero Delay Buffer

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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Quality Engineering Director
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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
I000005	3.3V, 125MHz Multi-Output Zero Delay Buffer, CY29972AIT is a member of the G35C base wafer product, 0.35um Technology, Chartered Semiconductor Singapore, Fab 2	2000

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: Qualify G35C Die			
Marketing Part #:	Various		
Device Description:	3.45V, Commercial, available in various packages		
Cypress Division:	Cypress Semiconductor Corporation – Timing Technology Division (TTD-IMI)		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A	
Die Size (stepping):	80 mils x 93 mils		
What ID markings on DIE	G35C		

TECHNOLOGY/FAB PROCESS DESCRIPTION S4AD-5			
Number of Metal Layers:	3	Metal Composition:	Metal 1,2: 100Å IMPTi/300Å TiN/.5KAlCu/350Å Tin ARC Metal 3: 300Å IMPTi /300Å TiN/.8K AlCu/350Å TiN ARC
Passivation Type and Materials:		350Å TiN/2K PSG/7K Si_3N_4	
Free Phosphorus contents in top glass layer(%):		0%	
Number of Transistors in Device:		8,000	
Number of Gates in Device		2225	
Generic Process Technology/Design Rule (µ-drawn):		CMOS, Triple Metal /0.35 µm	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 65Å	
Name/Location of Die Fab (prime) Facility:		Chartered Semiconductor Singapore	
Die Fab Line ID/Wafer Process ID:		2L313-698-CBB/CRA	

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	N/A
Package Outline, Type, or Name:	TQFP
Mold Compound Name/Manufacturer:	N/A
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated 85% Sn, 15% Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	N/A
Die Attach Material:	N/A
Die Attach Method:	Epoxy
Bond Diagram Designation:	N/A
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0mil
Thermal Resistance Theta JA °C/W:	94.2°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	N/A
Name/Location of Assembly (prime) facility:	Signetics (Korea)

DIE QUALIFICATION TEST RESULTS

CY28346 was used to qualified G35C base die platform (0.35 um, 3 layers metal, CMOS, CSM-Singapore)

Test	Military or Industry Standard	Conditions	Test Points	Test Results	Comments
Life Test	MIL-STD-883 Method 1005	125^{o}C/3.6V	500 1000	0/116 0/116	
Life Test	MIL-STD-883 Method 1005	125^{o}C/3.6V	500 1000	0/116 0/116	
Life Test	MIL-STD-883 Method 1005	125^{o}C/3.6V	500 1000	0/116 0/116	
ESD	MIL-STD-883 Method 3015	HBM	2000V 3000V 4000V	0/3 0/3 0/3	
Latch-up	JESD78		200 mA	0/5	

PACKAGE QUALIFICATION TEST RESULTS

TQFP

Test	Military or Industry Standard	Conditions	Test Points	Test Results	Comments
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{O}C	500	0/76	
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{O}C, 2 atm	168	0/76	
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{O}C	500	0/76	
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{O}C, 2 atm	168	0/76	
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{O}C	500	0/45	
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{O}C, 2 atm	168	0/45	
Physical Dimension	JEDEC Spec.	Applicable drawing	N/A	0/12	
Resistance to Solvent	MIL-STD-883 Method 2015		N/A	0/12	
Solderability	MIL-STD-883 Method 2003	260 Deg, 5 sec 95% Min Covrg	N/A	0/5	
Coplanarity	JEDEC Spec.	Max = 4 Mil	N/A	0/20	
Physical Dimension	JEDEC Spec.	Applicable drawing	N/A	0/12	
Resistance to Solvent	MIL-STD-883 Method 2015		N/A	0/12	
Solderability	MIL-STD-883 Method 2003	260 Deg, 5 sec 95% Min Covrg	N/A	0/5	
Coplanarity	JEDEC Spec.	Max = 4 Mil	N/A	0/20	

Package: SSOP

Test	Military or Industry Standard	Conditions	Test Points	Test Results	Comments
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{O}C	500	0/76	
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{O}C	500	0/77	
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{O}C	500	0/77	
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{O}C, 2 atm	168	0/76	
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{O}C, 2 atm	168	0/77	
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{O}C, 2 atm	168	0/76	

Note: "MSL-1" indicates samples were preconditioned to MSL-1 moisture level prior to package qualification stress tests

Package: TSSOP

Test	Military or Industry Standard	Conditions	Test Points	Test Results	Comments
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{o}C	500	0/76	
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{o}C	500	0/45	
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{o}C, 2 atm	168	0/76	
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{o}C, 2 atm	168	0/45	

Note: "MSL-1" indicates samples were preconditioned to MSL-1 moisture level prior to package qualification stress tests

Document History Page

Document Title: QTP#I000005:125MHZ MULTI-OUTPUT ZERO DELAY BUFFER "CY29972AIT" 0.35UM TECHNOLOGY, CSM FAB 2
Document Number: 001-89529

Rev.	ECN No.	Orig. of Change	Description of Change
**	4145424	HSTO	Initial Spec Release Qualification report published on Cypress.com and was transferred to qualification report spec template.

Distribution: WEB

Posting: None