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The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Cypress Semiconductor
Product Qualification Report

QTP# 97132 VERSION *B
June, 2014

32K X 8 LOW POWER SRAM R32 TECHNOLOGY, FAB4	
CY62256V	32K x 8 SRAM Low Power (3V)
CY62256	32K x 8 SRAM Low Power (5V)

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
97132	CY62256/CY62256V , 32K x 8 Low Power SRAM - R32 Technology Qualification	Jun 03

PRODUCT DESCRIPTION (for qualification)			
Information provided in this document is intended for generic qualification and technically describes the Cypress part			
Marketing Part #:	CY62256, 5V Operation CY62256V, 3V Operation		
Package:	28-pin, 300-mil SOJ		
Device Description:	32K x 8 Static RAM		
Cypress Division:	Cypress Semiconductor Corporation		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. C	
What ID markings on Die:	7C1256A (CY62256) 7C1257A (CY62256V)		

TECHNOLOGY/FAB PROCESS DESCRIPTION - R32			
Number of Metal Layers:	1	Metal Composition:	Metal 1: TiW/Al, 500Å/8,000Å
Passivation Type and Materials:	Silicon Dioxide 7,000Å + Silicon Nitride 6,000Å		
Number of Transitors in device	1,600,000		
Number of Gates in devices	N/A (Not a Logic device)		
Free Phosphorus contents in top glass layer(%):	0%		
Die Coating(s), if used:	No die coat (Low Alpha Molding)		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Double Poly, Single Metal /0.5 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 145Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R32		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	28-pin, 300-mil SOJ		
Mold Compound Name/Manufacturer:	NITTO-8000CH		
Lead Frame material:	Copper Alloy 194		
Lead Finish, composition:	Solder Plated, 85%Sn, 15%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Epoxy	Die Attach Material:	Ablestick 8361
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.3 mil
JESD22-A112 Moisture Sensitivity Level:	Level 1		
Name/Location of Assembly (prime) facility:	Omedata, Indonesia		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.80V/3.90V/5.75V,150°C JESD22-A108	P
Read and Record Life Test	Dynamic Operating Condition, Vcc = 4.3V, 150°C JESD22-A108	P
Long Live Verification	Dynamic Operating Condition, Vcc = 3.90V, 150°C JESD22-A108	P
Cold Life Test	Dynamic Operating Condition, Vcc=6.5V, -30°C, f=1 MHz JESD22-A108	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 3.63V/3.90V/5.50V, 150°C JESD22-A108	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 140°C, 85%RH, 3.6V/5.5V Precondition: JESD22 Moisture Sensitivity Level 1 (168 Hrs, 85C/85%RH)	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 1 (168 Hrs, 85C/85%RH)	P
High Temp Storage	JESD22-A103:165°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	750V, JESD22-C101	P
Latchup Sensitivity	10V, In accordance with JEDEC 17	P
Aged Bond Strength	MIL-STD-883, Method 2011	P
SEM Analysis	MIL-STD-883, Method 2018	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF	Failure Rate
High Temperature Operating Life Early Failure Rate	N/A	N/A	N/A	N/A	N/A
High Temperature Operating Life[1,2] Long Term Failure Rate	1,062,000 DHRs	1	0.6	170	6 FIT

1 Assuming an ambient temperature of 55C and a junction temperature rise of 15C.
2 Chi-squared 60% estimations used to calculate the failure rate..
3 Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 97132

Device	Assy-Loc	Fablot#	Assylot#	Duration	S/S	Rej	Fail Mode
STRESS: ESD-CHARGE DEVICE MODE, 750V							
CY62256V-VC	INDNS-O	4647470	519700560/6	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODE, 2000V							
CY62256V-VC	INDNS-O	4701592	519701274/5	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT, 2200V							
CY62256V-VC	INDNS-O	4649527	519701211/2	COMP	3	0	
CY62256V-VC	INDNS-O	4701592	519701274/5	COMP	3	0	
STRESS: LATCH-UP SENSITIVITY							
CY62256V-VC	INDNS-O	4647470	519700560/6	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. 168 HRS 85C/85%RH							
CY62256V-VC	INDNS-O	4647470	519700560/604/5	128	90	0	
CY62256V-VC	INDNS-O	4647470	519700560/604/5	256	90	0	
CY62256-VC	INDNS-O	4701592	519701274/5/6	128	50	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 3.6V), PRECOND. 168 HRS 85C/85%RH							
CY62256V-VC	INDNS-O	4649527	519701211/2/3	128	50	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY62256V-VC	INDNS-O	4647470	519700560/604/5	336	48	0	
CY62256V-VC	INDNS-O	4647470	519700560/604/5	1000	48	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.9V)							
CY62256V-VC	INDNS-O	4647470	519700560/604/5	80	152	0	
CY62256V-VC	INDNS-O	4647470	519700560/604/5	168	152	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V)							
CY62256V-VC	INDNS-O	4649527	519701211/2/3	80	162	0	
CY62256V-VC	INDNS-O	4649527	519701211/2/3	168	162	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.50V)							
CY62256-VC	INDNS-O	4701592	519701274/5/6	80	162	0	
CY62256-VC	INDNS-O	4701592	519701274/5/6	168	162	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.90V)							
CY62256V-VC	INDNS-O	4647470	519700560/604/5	80	522	0	
CY62256V-VC	INDNS-O	4647470	519700560/604/5	500	522	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.80V)							
CY62256V-VC	INDNS-O	4649527	519701211/2/3	80	540	0	
CY62256V-VC	INDNS-O	4649527	519701211/2/3	500	540	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY62256-VC	INDNS-O	4701592	519701274/5/6	80	540	0	
CY62256-VC	INDNS-O	4701592	519701274/5/6	500	540	1	Non-visual single bit

Reliability Test Data

QTP #: 97132

Device	Assy-Loc	Fablot#	Assylot#	Duration	S/S	Rej	Fail Mode
STRESS: EXTENDED DYNAMIC BURN-IN (150C, 3.90V)							
CY62256V-VC	INDNS-O	4647470	519700560/604/5	1000	522	0	
STRESS: COLD LIFE TEST (-30C, 6.5V)							
CY62256-VC	INDNS-O	4701592	519701274/5/6	500	52	0	
STRESS: READ & RECORD LIFE TEST (150C, 4.3V)							
CY62256V-VC	INDNS-O	4647470	519700560/604/5	500	10	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH							
CY62256V-VC	INDNS-O	4647470	519700560/604/5	300	88	0	
CY62256V-VC	INDNS-O	4647470	519700560/604/5	1000	88	0	
CY62256V-VC	INDNS-O	4649527	519701211/2/3	300	46	0	
CY62256V-VC	INDNS-O	4649527	519701211/2/3	1000	46	0	
CY62256-VC	INDNS-O	4701592	519701274/5/6	300	48	0	
CY62256-VC	INDNS-O	4701592	519701274/5/6	1000	48	0	

Document History Page

Document Title: QTP #97132: 32K X 8 LOW POWER SRAM (CY62256V / CY62256) R32 TECHNOLOGY, FAB4
Document Number: 001-88021

Rev.	ECN No.	Orig. of Change	Description of Change
**	4033729	ILZ	Initial Spec Release Qualification report published on Cypress.com is not in spec format. Initiated spec for QTP 97132 and removed all Cypress reference spec and replaced with Industry standard. Updated package availability based on current qualified assembly
*A	4323744	HSTO	Align qualification report based on the new template in the front page Corrected ESD-CDM test condition Add ESD-CDM, ESD-HBM and Latch-Up Sensitivity data in page 6 as per memo KN-636.
*B	4417735	JYF	Sunset review: Updated Reliability Tests Performed table to include industry standard of HTS, LFR, Read/Record Life Test, LLV, Cold Life Test, HTSSL, HAST and HTS.

Distribution: WEB

Posting: None