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Cypress Semiconductor
Product Qualification Report

QTP#140304
January 2014
Simtek: 05-51-030

Simtek 4K_16K_64K 5V nvSRAM Product Qualification 0.8*u*m Technology, Chartered Semiconductor Fab2	
STK10C48	**4K (512x8) 5V nvSRAM**
STK11C48	**4K (512x8) 5V nvSRAM**
STK22C48	**16K (2Kx8) 5V nvSRAM**
STK25C48	**16K (2Kx8) 5V nvSRAM**
STK10C68	**64K (8Kx8) 5V nvSRAM**
STK11C68	**64K (8Kx8) 5V nvSRAM**
STK12C68	**64K (8Kx8) 5V nvSRAM**
STK15C68	**64K (8Kx8) 5V nvSRAM**
STK16C68	**64K (8Kx8) 5V nvSRAM**

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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
05-51-030		Simtek CSM2 4K_16K_64K 5V nvSRAM Products		Mar 2005
140304		Simtek Qualification Report Integration – Paper Qualification		Dec 2008

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PRODUCT QUALIFICATION REPORT

Fab Line Change: 4K, 16K and 64K 5V nvSRAM Products

Update: 14 February 2005
New characterization data based on process improvements.
Updated qualification test data

SUMMARY

Simtek is changing the production line at its Chartered Semiconductor Manufacturing wafer supplier in Singapore from its older Fab 1 line to its newer Fab 2 line at the same location. As the fab line changes, the revision level will change from Rev. H (Fab 1) to Rev L (Fab 2). There is no change in the design of the die and the process used in Fab 2 will continue to be the same .8 micron process that has been used in Fab 1. There are no changes to any electrical or mechanical data sheet specifications. To ensure consistency of product characteristics, Simtek has done a comparison of the electrical performance between devices manufactured in Fab 1 and Fab 2. This report details the results of this comparison and confirms the consistent characteristics of product built on both Fab lines.

PRODUCT AFFECTED

Simtek 4K 512x8, 16K 2Kx8 and 64K 8Kx8 5V nvSRAM products.

PART NUMBERS AFFECTED

STK10C48	STK25C48	STK12C68
STK11C48	STK10C68	STK15C68
STK22C48	STK11C68	STK16C68

- All package types
- All speed grades.
- All temperature grades.

NEW PRODUCT DESIGN REV ID

Products out of Fab 2 will be marked "**Simtek L**" on the first line of the topside mark. The previous revision ID was "Simtek H".

CHANGE DETAIL

- ❑ This line move is from Chartered Semiconductor's Fab 1 [CSM1] to Fab 2 [CSM2].
- ❑ The Simtek nvSRAM design has been transferred to the new line without change.
- ❑ The product is being built to the same 0.8 micron design as in CSM1.
- ❑ The process used to manufacture the 64K products is identical to that used for the Simtek 256K 5V devices. The 256K product reliability/qualification data is applicable to the 64K die.
- ❑ The 64K device will be qualified by extension using the 256K data plus a 500hr readpoint for HTOL and Retention using 64K product. 1M cycle Endurance lifetest will also be completed. ESD and Latchup characterizations will be completed.
- ❑ Product characterization data comparing the CSM1 and CSM2 products will be published in the same report format as for the 256K products.
- ❑ The CSM2 product meets the current datasheet specifications as published on the Simtek website [www.Simtek.com].
- ❑ No changes are being made in assembly or final test & burn-in.

DATA SUPPORTING CHANGE

Appendix A - Process Characterization Report:
Comparison of CSM1 and CSM2 key process parameters affecting device functionality.
Appendix B - Product Characterization Report:
Comparison of key product datasheet parameters between the CSM1 and CSM2 products.
Appendix C - Qualification Lifetest Schedule:
Life test methods, conditions and readpoint schedule.

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Appendix A

Process Characterization Report

Comparison of CSM1 and CSM2 key process parameters affecting device functionality.

Parameter	Unit	% Change	Comments
NLLS Vtlin	Volt	6%	
NLLS Idsat	mA	-3%	
NLLS Bvdss	Volt	3%	
PLLS Vtlin	Volt	4%	
PLLS Idsat	mA	-5%	
PLLS Bvdss	Volt	2%	
NHLS Vtlin	Volt	10%	
NHLS Idsat	mA	-5%	
NHLS Bvdss	Volt	8%	
PHLS Idsat	mA	-3%	
PHLS Bvdss	Volt	4%	
SNOS Icell Ik	uA	0%	
VMG Positive Vstop	Volt	1%	
VMG Negative Vstop	Volt	1%	
NLV Bkn	Volt	1%	
PLV Bkn	Volt	0%	
NHV Bkn	Volt	3%	
PHV Bkn	Volt	2%	
NLP1 Vtsat	Volt	-7%	
NHP 2 Vtsat	Volt	-6%	
Ndiff	Ohm/Sq	-4%	
Pdiff	Ohm/Sq	-5%	
Npoly1	Ohm/Sq	-3%	
NPoly2	Ohm/Sq	8%	
N Contact	Ohm	4%	
P Contact Ohm/con	Ohm	27%	* Due to use of different/better barrier metal material
M1/M2 Via	Ohm	-8%	
Buried Contact 1 Rcon	Ohm	4%	
Buried Contact 2 Rcon ohm/con	Ohm	2%	

Summary

Absolute wafer level e-parameter values are proprietary to Simtek and the Wafer Foundry.

All values for the CSM2 process correlate well with the original CSM1 process and remain well within the original CSM1 process specification limits.

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Appendix B

Product Characterization Report

Comparison of key product datasheet parameters between CSM1 [Fab 1, Rev H] and CSM2 [Fab 2, Rev L] products.

Product Characterization Report [preliminary]
Comparison of key product datasheet parameters between the CSM1 [Fab 1, Rev H] and CSM2 [Fab 2, Rev L] products

Product Tested

- STK12C68
- Package: "P", type Plastic 28 300 mil PDIP
- Date Code 0440

Applicable Devices
The characterization data applies to all devices listed on page 1 of this report. All devices are built from the same die with different bond-outs.

Test Conditions

- Standard set of all characterization parameters
- 5 temperatures (-40C, 0C, 25C, 70C, 85C).
- 5 voltages (4.0V, 4.5V, 5.0V, 5.5V, 6.0V).

Data Analysis
The following table shows the datasheet parameters, specification limits, the CSM2 [Product Revision L margin to specification and the change in margin to spec from CSM1 to CSM2. Where the change in margin to spec column shows a positive number that indicates FAB2 material has more margin than FAB1. Negative numbers in the margin to spec column indicate less margin to spec for FAB2 compared to FAB1. The parameter values are derived from the worst case averages of commercial temperature (0C to 70C) and voltage (4.5V to 5.5V) conditions for samples from each fab. All testing was performed at the same time on the same tester, hardware, and program.

Summary
The current production product is now running well within datasheet specifications with adequate margin on all parameters. Value changes between product revision parameters are nominal and should not affect in-system performance.

Corrective Actions Completed
1. VSWITCH adjustment has been made moving the Vswitch value from 4.01V to 4.18V.
2. ICC3 adjustment has been made increasing Cpk to >1.3
3. ICC4 adjustment has been made increasing Cpk to >1.3
4. ISB2 adjustment has been made increasing Cpk to >1.3

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Symbol	#	Parameter	45ns Spec		Margin to spec Fab2	Difference Fab2 to Fab1	Fab2 Cpk	Comment
			MIN	MAX				
READ CYCLE								
ELQV	1	Chip Enable Access Time		45ns	24.0	1.2	20.0	
AVAV	2	Read Cycle Time	45ns		25.1	1.5	20.9	
AVQV	3	Address Access Time		45ns	22.8	1.4	10.9	
GLQV	4	Output Enable to Data Valid		20ns	15.6	0.3	17.3	
AXQX	5	Output Hold after Address Change	5ns		9.9	1.0	11.0	
ELQX	6	Chip Enable to Output Active	5ns		10.7	0.9	8.92	
EHQZ	7	Chip Disable to Output Inactive		12ns	7.1	0.9	11.8	
GLQX	8	Output Enable to Output Active	0ns		4.3	0.4	4.8	
GHQZ	9	Output Disable to Output Inactive		12ns	7.4	0.6	6.2	
ELICCH	10	Chip Enable to Power Active	0ns		See Note	N/A	N/A	Guaranteed not tested
EHICCL	11	Chip Disable to Power Standby		45ns	See Note	N/A	N/A	Guaranteed not tested
WRITE CYCLE #1								
AVAV	12	Write Cycle Time	45ns		25.1	1.5	20.9	
WLWH	13	Write Pulse Width	30ns		18.5	0.1	20.6	
ELWH	14	Chip Enable to End of Write	30ns		19.9	0.2	33.2	
DVWH	15	Data Set-up to End of Write	15ns		8.1	-0.5	13.5	
WHDX	16	Data Hold after End of Write	0ns		3.0	0.2	5.0	
AVWH	17	Address Set-up to End of Write	30ns		22.9	-0.8	38.2	
AVWL	18	Address Set-up to Start of Write	0ns		4.4	-0.6	4.9	
WHAX	19	Address Hold after End of Write	0ns		2.2	0.4	3.7	
WLQZ	20	Write Enable to Output Disable		14ns	7.2	0.8	12.0	
WLQV	21	Output valid after end of Write		45ns	21.2	1.9	14.1	
WHQX	21	Output Active after End of Write	5ns		12.2	-6.1	10.2	
WRITE CYCLE #2								
AVAV	12	Write Cycle Time	45ns		25.1	1.5	20.9	
WLEH	13	Write Pulse Width	30ns		19.5	-0.3	16.2	
ELEH	14	Chip Enable to End of Write	30ns		19.6	0.1	32.7	
DVEH	15	Data Set-up to End of Write	15ns		8.3	-0.4	9.2	
EHDX	16	Data Hold after End of Write	0ns		3.3	0.1	3.7	
AVEH	17	Address Set-up to End of Write	30ns		22.9	-0.5	38.2	
AVEL	18	Address Set-up to Start of Write	0ns		3.7	-0.9	4.1	
EHAX	19	Address Hold after End of Write	0ns		2.4	0.3	4.0	
HARDWARE STORE CYCLE								
HLHZ	22	Store Cycle Duration		10ms	2.7	0.2	1.8	
HLQZ	23	Time allowed to compl SRAM cycle	1us		0.52	0.1	1.7	
HHQX	24	Hardware Store High to Inhibit Off		700ns	310	32.0	2.1	
HLHX	25	Hardware Store Pulse Width	15ns		10.8	0.0	9.0	
HLBL	26	Hardware Store Low to Store Busy		300ns	184	4.0	4.4	

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Symbol	#	Parameter	45ns Spec		Margin to spec Fab2	Difference Fab2 to Fab1	Fab2 Cpk	Comment
AUTOSTORE / POWER-UP RECALL								
RESTORE	27	Power-Up Recall Duration		550us	N/A	N/A	N/A	Not tested
HLHZ	28	Store Cycle Duration		10ms	2.7	0.2	1.8	
VSBL	29	Vswitch to HSB\ Low		300ns	196	0.0	5.4	
BLQZ	30	Time to complete SRAM cycle	1us		0.4	0.09	3.3	
VSWITCH	31	Low Voltage Trigger Level	4.0V		0.18	-0.02	1.5	
VRESET	32	Low Voltage Reset Level		3.9V	1.0	0.2	1.7	
SOFTWARE-CONTROLLED STORE / RECALL								
AVAV	12	Write Cycle Time	45ns		25.1	1.5	20.9	
AVEL	34	Address Setup Time	0ns		3.7	-0.9	4.1	
ELEH	35	Clock Pluse Width0.	30ns		19.6	0.1	32.7	
ELAX	36	Address Hold Time	20ns		8.5	0.6	7.1	
RECALL	37	Recall Duration		20us	4.7	1.0	2.0	
DC CHARACTERISTICS								
ICC1		Ave Vcc Current @ AVAV=45ns		65mA	26.0	-2.0	8.7	
ICC2		Ave Vcc Current During Store		3mA	1.1	0.1	3.7	
ICC3		Ave Vcc Current @200ns, 3.3V, 25C		10mA	0.8	0.9	1.3	Ave value measured
ICC4		Ave Vcap Current during Autostore		2mA	1.15	-0.05	1.9	
ISB1		Ave Vcc SB current @AVAV = 45ns		21mA	7.0	-0.7	5.8	
ISB2		Vcc Standby Current		1.5mA	0.64	-0.14	2.1	
ILKG		Input Leakage Current	-1uA	1uA	N/A	N/A	N/A	Not tested
IOLKG		Off-State Output Leakage Current	-5uA	5uA	N/A	N/A	N/A	Not tested
VIH		Input Logic "1" Level	2.2V		0.6	-0.17	2.0	
VIL		Input Logic "0" Level		0.8V	0.35	0.08	2.3	
VOH		Output Logic "1" Voltage	2.4V		1.3	0.8	10.8	
VOL		Output Logic "0" Voltage		0.4V	0.19	0.0	2.1	
VOLBU		Logic "0" Voltage on HSB\ Output		0.4V	0.31	0.01	5.3	

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Appendix C

Qualification Lifetest Report

CSM2 0.8µ CMOS/SNOS Process, Simtek 64K 5V nvSRAM

Test	Method	Conditions	Readpoint	Start Qty	# of Failures	Failure Detail
High Temperature Operating Life [HTOL]	Mil-Std-883, M1005	Dynamic, Condition D Full SRAM Array, 125C, Vcc nom	0 hrs	77	0	
			168 hrs	77	0	
			500 hrs	77	0	
			1000 hrs	77	0	Zero fails @ 1Khr
Retention	Mil-Std-883 M1008	Unbiased 150C Store nv array at 0 hr Read stored data.	0 hrs	77	0	
			48 hrs	77	0	
			168 hrs	77	0	
			500 hrs	77	0	
			1000 hrs	77	0	Zero fails @ 1Khr
Endurance	Simtek	Store/Recall cycles of full nv array Functional check at read points	0 cycles	77	0	
			100K cycles	77	0	
			500K cycles	77	0	
			1M cycles	77	0	Zero fails @ 1M cycles
ESD	JEDEC 22-B A114	Human Body Model		6	0	Pass 1.8KV
Latch-Up Integrity	JEDEC 78	± 100mA, 70C		6	0	Pass ±100mA, 70C

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Additional Qualification Lifetest Data

CSM2 0.8µ CMOS/SNOS Process, Simtek 256K 5V nvSRAM

Same cell design, peripheral circuitry, process, foundry line [see page 1]

Test	Method	Conditions	Readpoint	Start Qty	# of Failures	Failure Detail
High Temperature Operating Life [HTOL]	JESD-22 A108	Dynamic Full SRAM Array 125C Vcc nom 4 Fab Lots	0 hrs	467	0	
			168 hrs	467	0	
			500 hrs	467	0	
			1000 hrs	467	0	4 lots. zero fails @ 1K hrs.
Retention	Simtek	Unbiased Bake 150C Store nv array at 0 hr Read stored data at read points 4 Fab Lots	0 hrs	400	0	
			48 hrs	400	0	
			168 hrs	400	1	1 fail at 10yr/70C equivalent. Corrective action: Adjust retention screen limit.
			500 hrs	399	1	1 fail at 10yr/85C equivalent. Corrective action: Adjust retention screen limit.
			1000 hrs	398	0	4 lots. 2 fails through 1K hrs. Corrective actions complete & verified[1]
Endurance	Simtek	Store/Recall cycles of nv array Recall and Functional check at read points	0 cycles	269	0	
			100K cycles	269	0	
			500K cycles	269	0	
			1M cycles	269	0	4 lots. Zero fails @ 1M cycles.
ESD	JEDSD22 A114	Human Body Model		5	0	Pass 1.8KV
Latch-Up Integrity	JEDEC 78	± 100mA, 70C		6	0	Pass ±100mA, 70C

Note 1: 2 failures recorded in retention testing [store NV array followed by unbiased bake with interim readpoints to verify stored data pattern is no corrupted and all cells read correct data state]. Wafer level retention screening limits adjusted to provide greater margin against Data Sheet Retention specification.

Document History Page

Document Title: QTP 140304: SIMTEK 4K_16K_64K NVSRAM PRODUCT QUALIFICATION
Document Number: 001-90726

Rev.	ECN No.	Orig. of Change	Description of Change
**	4251890	ZIJ	Initial spec release.
*A	4258067	ZIJ	Fix a document number typo in the first and last page of the report.

Distribution: WEB

Posting: None