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Cypress Semiconductor
Product Qualification Report

QTP#124908
December 2014
Ramtron#: 02-60-5142

3V Integrated Processor Companion with F-RAM Serial Memory Product Qualification 130nm Technology, TI Fab	
FM33256B-G	256Kb 3V Serial F-RAM Memory
FM33256B-GTR	256Kb 3V Serial F-RAM Memory

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose	Date Comp
02-60-5112 / 124901		TI Process Qualification 130nm F-RAM Process	Aug 2008 / Dec 2012
02-60-5142		3V Integrated Processor Companion with F-RAM® Serial Memory Product Qualification	July 2012
124908		Ramtron quality integration - paper qual	Jan 2013
124908		Standardize from MSL1 to MSL3	Dec 2014

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate (ELFR)	2400 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate (HTOL)	547,000 DHRs* 231,000 DHRs	0	0.7	55	21 FITs

*Leverage HTOL data from TI 130nm F-RAM Process QTP#124901 (SPEC#001-85093)

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation
[4] Thermal Total device hours is based on HTOL test and post endurance cycles HTOL test

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Qualification Report

(Document #02-60-5142)

FM33256B-G

3V Integrated Processor Companion with F-RAM
Revision: AB

Foundry Supplier: Texas Instruments, Dallas, TX, USA; IBM, Burlington, VT

Package Suppliers: UTAC, Bangkok, Thailand

Issue Date: 7/20/2012

Originated by: Quality and Reliability Assurance

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1. SCOPE

1.1 Qualification die-related testing was completed on two corner lot splits and one nominal lot split of FM33256B-G product, 3V Integrated Processor Companion with F-RAM from Ramtron's 130 nm F-RAM and 180 nm CMOS interface process fab families, offered in a 14-lead Green SOIC package.

1.2 Product testing is designed to assess overall compliance to the JESD47H.01 Standard.

1.3 These devices were fabricated at Texas Instruments in Dallas, Texas and at IBM in Burlington Vermont. Product qualified was assembled at UTAC in Bangkok, Thailand. Qualification stress/testing was performed at Ramtron International Corporation in Colorado Springs, CO, Integra Technologies in Santa Clara, CA, UTAC in Bangkok, Thailand, and at Innovative Circuits Engineering in San Jose, California.

1.4 The following report details the environmental stress tests performed, test sample sizes, accept/reject criteria, test results and conclusions of this qualification. Test and inspection results performed on the selected qualification lots are also summarized in a table at the end of this report.

2. APPLICABLE DOCUMENTS

2.1 Ramtron FM33256B Datasheet dated January 2012, Rev. 1.0

2.2 JESD47H.01 Stress-Test-Driven Qualification of Integrated Circuits

3. RELIABILITY STRESS TESTS

3.1 Pre-conditioning of Samples

3.1.1 Inspection method: JEDEC JESD22 A113-C

3.1.2 Stress Conditions: Moisture Sensitivity Level 3 soak conditions (30°C, 60%

Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

3.1.3 Purpose: The purpose of the pre-conditioning of samples prior to HAST, Autoclave and Temperature Cycle is to simulate typical solder reflow operation.

3.1.4 Sample size: 77 units per lot per test

3.1.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure from sample. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an

operating temperature of 25°C and 85°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.1.6 Pre-conditioning Test Results:

FM33256B-G	Lot # 15HYB_SH	Lot# 15HYB_SL	Lot# 15HYB_Nominal
Post Pre-Condition Electrical Test @ 25 °C	0 fails/231 parts	0 fails/231 parts	0 fails/231 parts
Post Pre-Condition Electrical Test @ 85 °C	0 fails/231 parts	0 fails/231 parts	0 fails/231 parts

3.2 Preconditioned Autoclave (AC)

3.2.1 Inspection Method: Preconditioning: JEDEC JESD22 Method A113-C

Autoclave: JEDEC JESD22 Method A102 Rev. C

3.2.2 Stress Conditions:

Preconditioning Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

Autoclave: 121ºC, 29.7 psia 100% Relative Humidity, 96 hrs

3.2.3 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Unbiased autoclave is performed to evaluate the moisture resistance of non hermetic packages. This is a highly accelerated test which employs conditions of pressure, humidity and temperature to accelerate moisture penetration through external protective materials or along the interface between external protective materials and the metallic conductors passing through it.

3.2.4 Sample Size 77 parts per lot

3.2.5 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at 25°C after stress. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.2.6 Pre-Conditioned Autoclave (AC) Test Results:

FM33256B-G	Lot # 15HYB_SH	Lot# 15HYB_SL	Lot# 15HYB_Nominal

Post Pre-condition Autoclave Electrical Test 25 °C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts

3.3 Preconditioned Highly Accelerated Test (HAST)

3.3.1 Inspection Method: Preconditioning: JEDEC JESD22 Method A113-C

HAST- JEDEC Method A110-C

3.3.2 Stress Conditions:

Preconditioning: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

HAST: 130°C, 85% Relative Humidity, P=33.3psia, biased at 3.6 Vdc, 96 hours

3.3.3 Test Description: The purpose of the Preconditioned HAST test is to detect defective packaging materials and processes used for the assembly of these parts. Preconditioning simulates a standard multiple solder reflow operation. HAST conditions accelerate the penetration of moisture through the package molding material and die passivation to the active die surface. Die surface moisture, in turn, can initiate corrosion, ionic migration and other processes resulting in functional or parametric part failure.

3.3.4 Sample Size 77 parts per lot

3.3.5 Accept/Reject Criteria: Accept on 0 failures, reject on 1. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.3.6 Pre-Conditioned Highly Accelerated Stress Test (HAST) Test Results:

FM33256B-G	Lot # 15HYB_SH	Lot# 15HYB_SL	Lot# 15HYB_Nominal
Post Pre-condition Autoclave Electrical Test 25°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post Pre-condition Autoclave Electrical Test 85°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts

3.4 Preconditioned Temperature Cycling (TC)

3.4.1 Inspection method: Preconditioning: JEDEC Method A113-C;

Temperature Cycling: JESD22, Method A104, Rev. B

Stress Conditions:

Preconditioning: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

Temperature Cycling: -50°C to +125°C, 500 cycles

3.4.2 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Temperature cycling stress testing is used to subject devices to severe temperature gradients by cycling the parts into hot and cold air. This test evaluates package strength, bond quality, and assembly process consistency. The test will reveal any thermal expansion mismatches in the die or die/package interfaces. At the conclusion of the temperature cycling test, an electrical functional and parametric test is performed at 25°C and 85°C.

3.4.3 Sample size: 77 parts per lot.

3.4.4 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at 25°C and 85°C after stress.

3.4.5 Pre-Conditioned TC Test Results:

FM33256B-G	Lot # 15HYB_SH	Lot# 15HYB_SL	Lot# 15HYB_Nominal
Post Pre-condition Temperature Cycle Electrical Test 25°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post Pre-condition Temperature Cycle Electrical Test 85°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts

3.5 Data Retention and High Temperature Storage Life (HTSL)

3.5.1 Inspection method: JESD22, Method A103, Rev. B

3.5.2 Stress Conditions: 125C, 1000 hours

3.5.3 Purpose: The purpose of the high temperature storage life test is determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms, including non volatile memory devices.

3.5.4 Sample size: Data Retention sample size is 3 lots of 77 pcs; High Temperature Storage samples size is 3 lots of 45 samples.

3.5.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure for a sample size of 45 parts from 1 lot. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.5.6 High Temperature Storage Life (HTSL) Test Results:

FM33256B-G	Lot # 15HYB_SH	Lot# 15HYB_SL	Lot# 15HYB_Nominal
Data Retention Test (Read 0's and Read 1's) at 25C, 500 hours	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Data Retention Test (Read 0's and Read 1's) at 25C, 1000 hours	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post HTSL Electrical Test 25°C	0 fails/45 parts	0 fails/45 parts	0 fails/45 parts
Post HTSL Electrical Test 85°C	0 fails/45 parts	0 fails/45 parts	0 fails/45 parts

3.6 High Temperature Operating Life (HTOL)

Inspection method: JESD22, Method A108, Rev. B

3.6.1 Stress Conditions: 125°C, 3.6 Vdc, operating 1000 hrs

3.6.2 Purpose: The purpose of the high temperature operating life test is to simulate device operation at elevated temperatures and higher than nominal operating voltages. The data obtained from this test is translated to a lower temperature (55°C) by using the Arhennius temperature acceleration modeling. The acceleration factor and distribution of failures accumulated is then fit to the appropriate failure distribution equation to statistically predict product end of operating life.

3.6.3 Sample size: Three lots of 77 samples each.

3.6.4 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C, 85°C and -40°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode identification and corrective action.

3.6.5 HTOL Test Results:

FM33256B-G	Lot # 15HYB_SH	Lot# 15HYB_SL	Lot# 15HYB_Nominal
Post HTOL Electrical Test 25°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post HTOL Electrical Test 85°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post HTOL Electrical Test -40°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts

3.7 Early Life Failure Rate (ELFR)

3.7.1 Inspection method: AEC-Q100-008.

3.7.2 Stress Conditions: 125°C, 3.65Vdc, 48 hours.

3.7.3 Test Description: The units are tested per the High Temp Operating Life requirements of Jedec 22-A108.

3.7.4 Sample size: 800 per lot

3.7.5 Accept/Reject Criteria: Accept on 0, reject on 1. Failed devices are removed from the test and submitted to Failure Analysis for failure mode identification and corrective action.

3.7.6 Early Life Failure Rate (ELFR) Test Results:

FM33256B-G	Lot # 15HYB_SH	Lot# 15HYB_SL	Lot# 15HYB_Nominal
Post ELFR Electrical Test 25°C	0 fails/800 parts	0 fails/800 parts	0 fails/800 parts
Post ELFR Electrical Test 85°C	0 fails/800 parts	0 fails/800 parts	0 fails/800 parts

3.8 Wire Bond Shear Test (WBS)

3.8.1 Inspection Method: JEDEC Method 22-B117

3.8.2 Stress Conditions: 5g force minimum

3.8.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices. Family data is acceptable for this test.

3.8.4 Sample size required: 30 bonds from a minimum of 5 devices. All bonds were tested on all five parts.

3.8.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33or Ppk>1.67

3.8.6 Wire Bond Shear (WBS) Test Results:

	UTAC: Minimum Avg Strength Shown, from four B-Family devices.
	0 fails/30 bonds
Average	22.46g
Ppk	4.44

3.9 Wire Bond Pull Test (WBP)

3.9.1 Inspection Method: MIL-STD883 Method 2011

3.9.2 Stress Conditions: For gold bond wires <1mil diameter, wipe bond pull is performed with the hook over the ball bond, and not mid-wire method.

3.9.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices.

3.9.4 Sample size: 30 bonds from a minimum of 5 devices

3.9.5 Accept/Reject Criteria: 3 grams force minimum. Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33or Ppk>1.67

3.9.6 Wire Bond Shear (WBS) Test Results:

	UTAC: Minimum Avg Strength Shown, from four B-Family devices.
	0 fails/30 bonds
Average	7.14g
Ppk	7.44

3.10 Solderability (SD)

3.10.1 Inspection method: JEDEC Method B102-C

3.10.2 Stress Conditions: 8 hour steam aging prior to solderability test

3.10.3 Purpose: The purpose of this test is to determine the solderability of device package terminal leads intended to be joined to another surface using solder. Family data is acceptable for this test.

3.10.4 Sample size: 15 samples from 1 lot.

3.10.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure.

3.10.6 Solderability (SD) Test Results Family Data from UTAC:

	UTAC Solderability on SOIC Leads: Lot #00001G1, FM24W256-G
Sample Size	15 parts
Pass/fail	15 passes/0 fails

3.11 Physical Dimensions (PD)

3.11.1 Inspection method: JEDEC Method B100-A

3.11.2 Stress Conditions: N/A

3.11.3 Purpose: Package outline and leads measured for concurrence with the Device Specification package drawing. Measurements are made with micrometers to determine adherence to specifications (Jedec MS-012). Family data is acceptable for this test.

3.11.4 Sample size: 30 units, UTAC 14-lead SOIC

3.11.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure.

3.11.6 Physical Dimension (PD) Results on 14-Lead SOIC (RAM05205):

SUPPLIER	PART NUMBER
NS Electronics Bangkok (1993) Ltd.	14L-SOIC-POD-002
NAME OF INSPECTION FACILITY	PART NAME
NS Electronics Bangkok (1993) Ltd.	RAM 14L SOMT GREEN PACKAGE

ITEM	DIMENSION	SPECIFICATION	Data#	SUPPLIER MEASUREMENT RESULT	OK	NOT OK
1	Package height	0.0570-0.0660 Inch.	1	0.0601 0.0604 0.0609 0.0606 0.0607	OK	
				MIN MAX AVG		
				0.0601 0.0609 0.0605		
2	Stand off height (S)	0.0040-0.0100 Inch.	1	0.0078 0.0076 0.0076 0.0077 0.0078 0.0076	OK	
				0.0076 0.0075 0.0079 0.0076 0.0077 0.0077		
				0.0077 0.0078 0.0075 0.0079 0.0079 0.0078		
				0.0078 0.0077 0.0077 0.0077 0.0076 0.0079		
				0.0077 0.0075 0.0078 0.0076 0.0078 0.0077		
				MIN MAX AVG		
				0.0075 0.0079 0.0077		
3	Lead width	0.0140-0.0190 Inch.	1	0.0164 0.0164 0.0165 0.0164 0.0164	OK	
				MIN MAX AVG		
				0.0164 0.0165 0.0164		
4	Lead thickness	0.0070-0.0100 Inch.	1	0.0088 0.0087 0.0086 0.0088 0.0087	OK	
				MIN MAX AVG		
				0.0086 0.0088 0.0087		
5	Package length	0.3370-0.3440 Inch.	1	0.3407 0.3406 0.3403 0.3405 0.3404	OK	
				MIN MAX AVG		
				0.3403 0.3407 0.3405		
6	Lead span (S)	0.2340-0.2440 Inch.	1	0.2388 0.2388 0.2387 0.2388 0.2388 0.2385	OK	
				0.2386 0.2386 0.2386 0.2390 0.2389 0.2391		
				0.2384 0.2386 0.2389 0.2387 0.2386 0.2388		
				0.2389 0.2385 0.2388 0.2386 0.2387 0.2387		
				0.2387 0.2390 0.2387 0.2387 0.2390 0.2386		
				MIN MAX AVG		
				0.2384 0.2391 0.2387		
7	Package width	0.1500-0.1570 Inch.	1	0.1518 0.1515 0.1519 0.1517 0.1516	OK	
				MIN MAX AVG		
				0.1515 0.1519 0.1517		
8	Lead pitch	0.0500 BSC.	1	0.0500 0.0500 0.0500 0.0500 0.0500	OK	
				MIN MAX AVG		
				0.0500 0.0500 0.0500		

SUPPLIER	PART NUMBER
NS Electronics Bangkok (1993) Ltd.	14L-SOIC-POD-002
NAME OF INSPECTION FACILITY	PART NAME
NS Electronics Bangkok (1993) Ltd.	RAM 14L SOMT GREEN PACKAGE

ITEM	DIMENSION	SPECIFICATION	Data#	SUPPLIER MEASUREMENT RESULT						OK	NOT OK
9	Lead length (Pin 1)	0.0220-0.0320 Inch.	1	0.0252	0.0255	0.0252	0.0246	0.0256		OK	
				MIN	MAX	AVG					
				0.0246	0.0256	0.0252					
10	Lead length (Op pin 1)	0.0220-0.0320 Inch.	1	0.0248	0.0249	0.0247	0.0241	0.0248		OK	
				MIN	MAX	AVG					
				0.0241	0.0249	0.0247					
11	Lead angle (Pin 1)	0-8 Degree	1	3	3	3	3	3		OK	
				MIN	MAX	AVG					
				3.0	3.0	3.0					
12	Lead angle (Op pin 1)	0-8 Degree	1	3	3	3	3	3		OK	
				MIN	MAX	AVG					
				3.0	3.0	3.0					
13	Lead coplanarity (S)	0.004 Inch. Max.	1	0.0000	0.0001	0.0000	0.0001	0.0001	0.0000	OK	
				0.0000	0.0000	0.0002	0.0000	0.0000	0.0001		
				0.0001	0.0000	0.0000	0.0000	0.0000	0.0000		
				0.0000	0.0000	0.0000	0.0002	0.0003	0.0000		
				0.0000	0.0003	0.0000	0.0000	0.0000	0.0002		
				MIN	MAX	AVG					
				0.0000	0.0003	0.0001					

Physical Dimension (PD) Results on 14-Lead SOIC (RAM05205):

SUPPLIER	PART NUMBER
NS Electronics Bangkok (1993) Ltd.	14L-SOIC-POD-002
NAME OF INSPECTION FACILITY	PART NAME
NS Electronics Bangkok (1993) Ltd.	RAM 14L SOMT GREEN PACKAGE (NSE 2)

ITEM	DIMENSION	SPECIFICATION	Data#	SUPPLIER MEASUREMENT RESULT					OK	NOT OK
1	Package height	0.0570-0.0660 Inch.	1	0.0609	0.0611	0.0609	0.0614	0.0612	OK	
				MIN	MAX	AVG				
				0.0609	0.0614	0.0611				
2	Stand off height (S)	0.0040-0.0100 Inch.	1	0.0078	0.0079	0.0076	0.0076	0.0077	OK	
				0.0079	0.0076	0.0078	0.0079	0.0078		
				0.0077	0.0077	0.0090	0.0078	0.0076		
			2	0.0078	0.0077	0.0079	0.0077	0.0078		
				0.0077	0.0078	0.0078	0.0079	0.0076		
				0.0076	0.0078	0.0076	0.0077	0.0077		
				MIN	MAX	AVG				
				0.0076	0.0090	0.0078				
3	Lead width	0.0140-0.0190 Inch.	1	0.0148	0.0146	0.0148	0.0150	0.0151	OK	
				MIN	MAX	AVG				
				0.0146	0.0151	0.0149				
4	Lead thickness	0.0070-0.0100 Inch.	1	0.0081	0.0079	0.0078	0.0081	0.0078	OK	
				MIN	MAX	AVG				
				0.0078	0.0081	0.0079				
5	Package length	0.3370-0.3440 Inch.	1	0.3401	0.3404	0.3402	0.3399	0.3396	OK	
				MIN	MAX	AVG				
				0.3396	0.3404	0.3400				

SUPPLIER	PART NUMBER
NS Electronics Bangkok (1993) Ltd.	14L-SOIC-POD-002
NAME OF INSPECTION FACILITY	PART NAME
NS Electronics Bangkok (1993) Ltd.	RAM 14L SOMT GREEN PACKAGE (NSE 2)

ITEM	DIMENSION	SPECIFICATION	Data#	SUPPLIER MEASUREMENT RESULT					OK	NOT OK
6	Lead span (S)	0.2340-0.2440 Inch.	1	0.2391	0.2379	0.2389	0.2387	0.2388	OK	
				0.2388	0.2386	0.2388	0.2388	0.2386		
				0.2387	0.2387	0.2389	0.2389	0.2387		
			2	0.2389	0.2389	0.2388	0.2390	0.2386		
				0.2387	0.2390	0.2389	0.2388	0.2391		
				0.2387	0.2386	0.2387	0.2389	0.2389		
				MIN	MAX	AVG				
				0.2379	0.2391	0.2388				
7	Package width	0.1500-0.1570 Inch.	1	0.1525	0.1524	0.1523	0.1521	0.1523	OK	
				MIN	MAX	AVG				
				0.1521	0.1525	0.1523				
8	Lead pitch	0.0500 BSC.	1	0.0500	0.0500	0.0500	0.0500	0.0500	OK	
				MIN	MAX	AVG				
				0.0500	0.0500	0.0500				
9	Lead length (Pin 1)	0.0220-0.0320 Inch.	1	0.0251	0.0251	0.0246	0.0254	0.0255	OK	
				MIN	MAX	AVG				
				0.0246	0.0255	0.0251				
10	Lead length (Op pin 1)	0.0220-0.0320 Inch.	1	0.0231	0.0233	0.0238	0.0239	0.0238	OK	
				MIN	MAX	AVG				
				0.0231	0.0239	0.0236				

3.12 Electrostatic Discharge - Human Body Model (ESD-HBM)

3.12.1 Test Method: Jedec JESD22-A114

3.12.2 Stress Conditions: Human Body Model, 100pF discharge through a 1.5K-ohm resistor.

3.12.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Human Body Model as detailed in JEDEC A114-B (100pF discharged through 1.5K ohms). The devices are subjected to voltage ranging from 500V through 4500V for each group of three (3) devices.

3.12.4 Sample size: 3 parts per voltage group tested.

3.12.5 Accept/Reject Criteria: A device passed a voltage level if all devices in the sample group stressed at that voltage and below pass.

NOTE: A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

3.12.6 FM33256B-G Rev. AB ESD HBM Test Results:

TEST		Voltage/Current	LOT #109XB
Electrostatic Discharge-Human Body Model	ESD-HBM		**25C & 85C**
		500V	3/3 pass
		1000V	3/3 pass
		1500V	3/3 pass
		2000V	3/3 pass
		2500V	3/3 pass
		3000V	3/3 pass
		3500V	3/3 pass
		4000V	3/3 pass
		4500V	3/3 pass

3.12.7 The FM33256B-G Rev AB passed HBM ESD to 4,500V. This is a Class 2 part (> 4,000V to </= 8,000V) by JESD22-A114.

3.13 Electrostatic Discharge – Charged Device Model (CDM)

3.13.1 Test Method: Jedec Standard JESD22-C101

3.13.2 Stress Conditions: Transferring of electrostatic charge between bodies at different electrostatic potentials, with circuitry as described in Jedec Standard 22-C101, Direct Charge or Field Induced Charge.

3.13.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Charged Device Model as detailed in Jedec Standard 22-C101. The devices are subjected to voltage ranges from 250V to 1250V.

3.13.4 Sample size: 3 parts per voltage group tested.

3.13.5 Accept/Reject Criteria: A device passes a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

3.13.6 Test Summary: ESD CDM Results

TEST	ABR	Voltage/Current	LOT #109XB
Electro Static Discharge - Charged Device Model	ESD-CDM		**25C & 85C**
		250V	3/3 pass
		500V	3/3 pass
		750V	3/3 pass
		1000V	3/3 pass
		1250V	3/3 pass

3.13.7 Conclusion: The FM33256B-G Rev AB passed CDM ESD to 1,200V. This is a Class IV for ESD-CDM sensitivity (>1000V) by JESD 22-C101.

3.14 Electrostatic Discharge – Machine Model (MM)

3.14.1 Test Method: JEDEC 22-A115

3.14.2 Stress Conditions: Machine Model, 200pF discharge through no resistance.

3.14.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Charged Device Model as detailed in Jedec Standard 22-C101. The devices are subjected to voltage ranges from 250V to 1250V.

3.14.4 Sample size: 3 parts per voltage group tested.

3.14.5 Accept/Reject Criteria: A device passes a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

3.14.6 Test Summary: ESD MM Results

TEST	ABR	Voltage/Current	LOT #109XB
Electro Static Discharge - Machine Model	ESD-MM		**25C & 85C**
		100V	3/3 pass
		200V	3/3 pass
		300V	3/3 fail
		400V	3/3 fail

3.14.7 Conclusion: The FM33256B-G Rev AB passed MM ESD to 200V. Machine Model ESD immunity is Class B (200V-399V) for these devices.

3.15 Latch-up Immunity (LU)

3.15.1 Test Method: AEC-Q100-004; Jedec Standard 22-78B

3.15.2 Stress Conditions: Latch-Up: Must pass +/- 100mA current injection, each input pin.

Vsupply Over-Voltage Test: 3.65 to 6.4V.

3.15.3 Test Description: The Latch-Up Immunity test assesses the devices susceptibility to latch-up at maximum operating temperatures (90°C). A negative current is applied to each package pin (pin to Vss then pin to Vcc). The current is incremented to +/-300mA, although AEC Q100-011 and Jedec Standard 22-78B only requires +/–100mA. The device Icc current is measured after each current increment and compared to the maximum value as detailed in the Device Specification. During the Vsupply Over-Voltage Test, the voltage is increased from 3.65 to 6.4V .measuring Icc at each increment after removing the Voltage source.

3.15.4 Sample size: 6 parts from one lot.

3.15.5 Accept/Reject Criteria: Accept on 0 failures and reject on one failure.

3.15.6 FM33256B-G Latch-Up (LU) Test Results:

TEST	ABR	Voltage/Current	LOT #109XB
Latch Up Immunity	LU	± 100 mA	**25 & 85C**
			6/6 parts pass

3.15.7 Conclusion: All devices performed to greater than +/-100mA in Latch up Immunity and passed the Vsupply Over-Voltage Test at 85°C.

4. CONCLUSIONS

JESD47 Qualification testing was completed on the FM33256B-G product. Based on the successful qualification testing and herein, the FM33256B-G is a qualified product.

5. QUALIFICATION SUMMARY TABLE

TEST	ABR	DURATION	Lot #15HYB_SH	Lot #15HYB_SL	Lot #15HYB_Nom
Pre-Conditioning	PC		0 fails/231 parts	0 fails/231 parts	0 fails/231 parts
(Preconditioned) Autoclave	AC	96-Hr AC 25°C 85°C	 0/77 0/77	 0/77 0/77	 0/77 0/77

TEST	ABR	DURATION	Lot #15HYB_SH	Lot #15HYB_SL	Lot #15HYB_Nom
(Preconditioned) Temperature Cycle	TC	500 Cycles 25°C 85°C	 0/77 0/77	 0/77 0/77	 0/77 0/77
Data Retention and High Temperature Storage Life 125°C	HTSL	Endurance Read Zeros Read Ones 25°C 85°C	0/77 0/77 0/77 0/45 0/45	0/77 0/77 0/77 0/45 0/45	0/77 0/77 0/77 0/45 0/45
High Temperature Operating Life	HTOL (500/1000 hours)	25°C 85°C -40°C	0/77 0/77 0/77	0/77 0/77 0/77	0/77 0/77 0/77
Early Life Failure Rate	ELFR	48 hours 25°C 85°C	 0/800 0/800	 0/800 0/800	 0/800 0/800
Wire Bond Shear Test	WBS	 Avg. Ppk	 22.46g 4.44		
Bond Wire Pull Test	WBP	Avg. Ppk	7.14g 7.44		
Solderability	SD	>95% Lead Coverage	0 fails/15 parts		
Physical Dimension	PD	Recorded	Physical Dimension Data is reported from two 14-Lead UTAC SOIC assembly lots.		
Pre & Post Stress			100% passing	100% passing	
TEST	**ABR**	**Voltage/Current**	**Lot# 109XB**		
Electrostatic Discharge-Human Body Model	HBM ESD	500V 1000V 1500V 2000V 2500V 3000V 3500V 4000V 4500V	0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts		
Electro Static Discharge Machine Model	MM ESD	100V 200V 300V 400V	0fails/3parts 0fails/3parts 3fails/3parts 3fails/3parts		
Electro Static Discharge Charged Device Model	CDM ESD	250V 500V 750V 1000V 1250V	0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts		
Latch Up Immunity	E4	± 100 mA	0fails/6parts		

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Rev.	ECN No.	Orig. of Change	Description of Change
**	3866654	CNOR	Initial spec release.
*A	3949973	LJN	Inserted fields that correspond with the file/properties because the revision was missing from document header in ** revision
*B	3954275	BECK	Added Reliability Failure Rate Summary
*C	4558038	BECK	Updated Page 1 to new template, and standardized from MSL1 to MSL3

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