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Cypress Semiconductor
Product Qualification Report

QTP # 102101 VERSION *A
July 2014

Synchronous/Asynchronous Dual Port SRAM (3.3V and 5V) R42HD Technology, Fab 4 Qualification	
CY7C024E **CY7C0241E** **CY7C025E** **CY7C0251E**	**4K X 16/18 AND 8K X 16/18 DUAL- PORT STATIC RAM**

FOR ANY QUESTIONS ON THIS REPORT, PLEAE CONTACT
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PRODUCT QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date
98064	R42HD Technology qualification (1Meg SRAM)	Nov 97
98368	Asynchronous/Synchronous DP SRAM, R42HD Technology, Fa4 qualification	Jun 98
98244	Synchronous/Asynchronous Dual Port SRAM (3.3V and 5V) R42HD Technology, Fab 4 Qualification	Sep 98
102101	Qualification for CMI R4 down bond option for 7C0268, 7C0264, 7C0368, 7C0364	Jul 10

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualification of CMI R4 down bond option for 7C0268, 7C0264, 7C0368	
Marketing Part #:	CY7C024E, CY7C0241E, CY7C025E, CY7C0251E
Device Description:	4K X 16/18 AND 8K X 16/18 DUAL-PORT STATIC RAM
Cypress Division:	Cypress Semiconductor Corporation – Memory and Product Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6000Å Al -5%Cu/1200Å TiW Metal 2: 500Å TiW/8000Å Al -5%Cu/300Å TiW
Passivation Type and Thickness:		7000Å SiO_2 + 6000Å Si_3N_4	
Generic Process Technology/Design Rule (µ-drawn):		CMOS, Double Metal /0.42 µm	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 110Å	
Name/Location of Die Fab (prime) Facility:		Fab 4 / CMI - Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		R42HD	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY FACILITY SITE
100L TQFP	JCET (JT)

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	AZ100
Package Outline, Type, or Name:	100-Lead Thin Quad Flat Pack
Mold Compound Name/Manufacturer:	Kyocera - KE G6000DA
Mold Compound Flammability Rating:	UL94
Oxygen Rating Index:	V0
Leadframe Material:	Copper
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation	Backgrind
Die Separation Method:	100% Saw Through
Die Attach Supplier:	Dexter
Die Attach Material:	QMI 509
Die Attach Method:	Epoxy
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au. 1.0 mil
Thermal Resistance Theta JA C/W:	24.63°C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	CML-R
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	KYEC

Note: Please contact a Cypress Representative for other package availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 6.5V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max=5.75V, 150°C	P
High Temperature Steady State life	150°C, 5.75V, Vcc Max	P
Low Temperature Operating Life	-30°C, 6.5V	P
High Accelerated Saturation Test (HAST)	130°C, 5.5V, 85%RH Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Pressure Cooker	121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow**, 260°C**+0, -5°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JESD22, Method A114-B	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, 1000V JESD22-C101	P
Static Latch-up	125C, ± 140mA JESD 78A,	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate[1]	1523	0	N/A	N/A	0 PPM
High Temperature Operating Life[2,3] Long Term Failure Rate	791,500 DHRs	0	0.7	170	7 FIT[5]

[1] A production burn-in of 96 Hrs at 125°C, 6.5V is required for the product.

[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

[3] Chi-squared 60% estimations used to calculate the failure rate.

[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

[5] Long Term Failure Rate is based on R42HD technology, 1Meg SRAM qualification, QTP #98064.

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP#: 98244

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 6.5V)							
CY7C026-AC	4827620	619809368L2	G-TAIWAN	48	968	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
7C026EC-GACB	4833177	619811293	G-TAIWAN	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL (1000V)							
7C017EC-MJCB	4833177	619812371	M-PHIL	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2200V)							
7C026EC-GACB	4833177	619811293	G-TAIWAN	COMP	3	0	
7C017EC-MJCB	4833177	619812371	M-PHIL	COMP	3	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C026-AC	4827620	619809368L2	G-TAIWAN	168	48	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH (MSL 3)							
CY7C026-AC	4827620	619809368L2	G-TAIWAN	300	48	0	

Reliability Test Data

QTP#: 98368

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
CY7C09389-AC	4818845	619806813	G-TAIWAN	48	289	0	
CY7C09389-AC	4821104	619808005	G-TAIWAN	48	1234	0	
STRESS: ESD-CHARGE DEVICE MODEL (1,000V)							
CY7C09389-AC	4818845	619806221	G-TAIWAN	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (1,100V)							
CY7C09389-AC	4818845	619806221	G-TAIWAN	COMP	3	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C09389-AC	4818845	619806221	G-TAIWAN	168	44	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH (MSL 3)							
CY7C09389-AC	4818845	619806221	G-TAIWAN	300	48	0	
CY7C09389-AC	4818845	619806221	G-TAIWAN	1000	48	0	

Reliability Test Data

QTP#: 98064

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 1000V							
CY7C109-VC	4738602	519712560	INDNS-O	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2200V							
CY7C109-VC	4738602	519712560	INDNS-O	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 5.5V), PRECOND. 192 HRS 30C/60%RH							
CY7C109-VC	4738602	519712560	INDNS-O	128	46	0	
CY7C109-VC	4738564	519712898	INDNS-O	128	46	0	
CY7C109-VC	4738564	519712898	INDNS-O	256	46	0	
CY7C109-VC	4739644	519714390	INDNS-O	128	46	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY7C109-VC	4738602	519712560	INDNS-O	336	46	0	
CY7C109-VC	4738602	519712560	INDNS-O	500	46	0	
CY7C109-VC	4738602	519712560	INDNS-O	1000	46	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C109-VC	4738602	519712560	INDNS-O	80	78	0	
CY7C109-VC	4738602	519712560	INDNS-O	168	78	0	
CY7C109-VC	4739644	519714390	INDNS-O	80	78	0	
CY7C109-VC	4739644	519714390	INDNS-O	168	78	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C109-VC	4739644	519714390	INDNS-O	80	528	0	
CY7C109-VC	4739644	519714390	INDNS-O	500	527	0	
CY7C109-VC	4745042	519800651L1	INDNS-O	80	520	0	
CY7C109-VC	4745042	519800651L1	INDNS-O	500	529	0	
STRESS: EXTENDED DYNAMIC BURN-IN (150C, 5.75V)							
CY7C109-VC	4739644	519714390	INDNS-O	1000	527	0	
STRESS: COLD LIFE TEST (-30C, 6.5V)							
CY7C109-VC	4738602	519712560	INDNS-O	500	45	0	
CY7C109-VC	4738602	519712560	INDNS-O	1000	45	0	

Reliability Test Data

QTP#: 98064

Device	Fab Lot #	Assy Lot #	Assy Lot	Duration	Samp	Rej	Failure Mechanism
STRESS: READ & RECORD LIFE TEST (150C, 5.75V)							
CY7C109-VC	4738602	519712560	INDNS-O	48	10	0	
CY7C109-VC	4738602	519712560	INDNS-O	500	10	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH							
CY7C109-VC	4738602	519712560	INDNS-O	300	46	0	
CY7C109-VC	4738602	519712560	INDNS-O	1000	46	0	
CY7C109-VC	4738564	519712898	INDNS-O	300	46	0	
CY7C109-VC	4739644	519714390	INDNS-O	300	46	0	

Reliability Test Data

QTP#: 102101

Device	Fab Lot #	Assy Lot #	Assy Lot	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, (2,200V)							
7C0364NFC	4010277	611027886	CML-R	COMP	8	0	
7C0268NFC	4010277	611027885	CML-R	COMP	8	0	
7C0264NFC	4010277	611021065	CML-R	COMP	8	0	
7C0368NFC	4010277	611027887	CML-R	COMP	8	0	
STRESS: STATIC LATCH-UP (125C, 8.25V, 140mA)							
7C0364NFC	4010277	611027886	CML-R	COMP	6	0	
7C0268NFC	4010277	611027885	CML-R	COMP	6	0	
7C0264NFC	4010277	611021065	CML-R	COMP	6	0	
7C0368NFC	4010277	611027887	CML-R	COMP	6	0	

Document History Page

Document Title: QTP#102101: SYNCHRONOUS/ASYNCHRONOUS DUAL PORT SRAM (3.3V AND 5V) R42HD TECHNOLOGY, FAB 4 QUALIFICATION
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Rev.	ECN No.	Orig. of Change	Description of Change
**	4040721	HSTO	Initial Spec Release Qualification report published on Cypress.com was transferred to qualification report spec template. Updated package availability based on current qualified test & assembly site. Deleted Cypress reference Spec and replaced with Industry Standards in Reliability Test Performed Table.
*A	4431902	HSTO	Align qualification report based on the new template in the front page Update Cypress division from Memory Image Division (MID) to Memory Product Division (MPD) at page3.

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