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Cypress Semiconductor
Product Qualification Report

QTP# 095106 VERSION*E
July 2020

36 Meg QDR/DDR Synchronous SRAM Family 65nm (LL65P-18R) Technology, UMC Fab 12A	
CY7C1243KV18	36-Mbit QDR-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1245KV18	36-Mbit QDR-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1248KV18	36-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1250KV18	36-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1263KV18	36-Mbit QDR-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1265KV18	36-Mbit QDR-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1268KV18	36-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1270KV18	36-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1411KV18	36-Mbit QDR-II SRAM 4-Word Burst Architecture
CY7C1412KV18	36-Mbit QDR-II SRAM 2-Word Burst Architecture
CY7C1413KV18	36-Mbit QDR-II SRAM 4-Word Burst Architecture
CY7C1414KV18	36-Mbit QDR-II SRAM 2-Word Burst Architecture
CY7C1415KV18	36-Mbit QDR-II SRAM 4-Word Burst Architecture
CY7C1418KV18	36-Mbit DDR-II SRAM 2-Word Burst Architecture
CY7C1420KV18	36-Mbit DDR-II SRAM 2-Word Burst Architecture
CY7C1423KV18	36-Mbit DDR-SIO SRAM 2-Word Burst Architecture
CY7C1424KV18	36-Mbit DDR-SIO SRAM 2-Word Burst Architecture
CY7C1425KV18	36-Mbit QDR-II SRAM 2-Word Burst Architecture
CY7C1426KV18	36-Mbit QDR-II SRAM 4-Word Burst Architecture
CY7C2245KV18	36-Mbit QDR-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency) with ODT
CY7C2263KV18	36-Mbit QDR-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency) with ODT
CY7C2265KV18	36-Mbit QDR-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency) with ODT
CY7C2268KV18	36-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) with ODT
CY7C2270KV18	36-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) with ODT

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date Comp
091706	Qualification of 65nm (LL65) Technology at UMC Fab 12A and New Device 72M QDR CY7C1553K Base Die Product Family	Aug 2009
093202	Qualification of UMC 65nm Process Improvement	Nov 2009
095106	LL65 36M QDR CY7C1273K Base Die Product Family Qualification	Nov 2010

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PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose:	Qualify 36M QDR CY7C1273K Base Die Product Family, LL65P-18R Technology at UMC Fab 12A 65nm
Marketing Part #:	CY7C1412KV18, etc.
Device Description:	1.8V Commercial and Industrial available in 165-Ball FBGA (13 x 15 x 1.4 mm)
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division

TECHNOLOGY/FAB PROCESS DESCRIPTION – LL65P-18R			
Number of Metal Layers:	Proprietary	Metal Composition:	Proprietary
Passivation Type and Thickness:			Proprietary
Generic Process Technology/Design Rule (μ-drawn):			Proprietary
Gate Oxide Material/Thickness (MOS):			Proprietary
Name/Location of Die Fab (prime) Facility:			UMC Fab 12
Die Fab Line ID/Wafer Process ID:			L65LL

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
165-Ball FBGA	**CML Autoline**

Note: Package Qualification details upon request

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MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165
Package Outline, Type, or Name:	165-Ball Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	CK7000 / Plascon
Mold Compound Flammability Rating:	UL94, V-0
Oxygen Rating Index:	45%
Substrate Material:	BT resin
Lead Finish, Composition / Thickness:	Sn63Pb37
Die Backside Preparation Method/Metallization:	Grinding
Die Separation Method:	Saw
Die Attach Supplier:	Hysol
Die Attach Material:	QMI 506
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-58365
Wire Bond Method:	Thermosonic
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	CML-Philippines

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Chipmos

Note: Please contact a Cypress Representative for other packages availability

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RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C JESD22-A108	P
High Temperature Operating Life Early Failure Rate Regulator On	Dynamic Operating Condition, Vcc Max=2.05V, 150°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C /150°C JESD22-A108	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at LFR 80hrs, 500hrs & 1000hrs	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 2.25V, 150°C Static Operating Condition, Vcc Max= 2.05V, 150°C JESD22-A108	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 2.25V, -30°C JESD22-A108	P
High Accelerated Saturation Test (HAST)	JESD22-A110: 130°C, 2.25V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C /60%RH+ Reflow, 260°C +0, -5°C	P
Temperature Humidity Bias Test (THB)	JESD22-A101: 85°C, 85%RH, 2.25V Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C /60%RH+ Reflow, 260°C +0, -5°C	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C /60%RH+ Reflow, 260°C +0, -5°C	P
Pressure Cooker	JESD22-A102: 121°C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C /60%RH+ Reflow, 260°C +0, -5°C	P
High Temperature Storage	JESD22-A103: 150°C ± 5°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101	P
Electrostatic Discharge Machine Model (ESD-MM)	200V JESD22-A115	P
Soft Error (Alpha Particle)	JESD89	P
Soft Error (Neutron/Proton)	JESD89	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C /60%RH+ Reflow, 260°C +0, -5°C	P
Dynamic Latchup	JESD78	P
Static Latchup	125°C, ± 200mA / ± 140mA JESD78	P

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RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	1,533 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate (150□C)	89,000 DHRs	0	0.7	170	18 FIT
High Temperature Operating Life[1,2] Long Term Failure Rate (125□C)	656,920 DHRs	0	0.7	55	

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

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Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	5	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	128	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	128	77	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1514KV18 (7C1553K)	8844020	610851583	TAIWN-G	1000	70	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	336	77	0	

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Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8908001	610920385	TAIWN-G	96	2367	0	
CY7C15631KV18 (7C1553K)	8912000	610920386	TAIWN-G	96	2217	0	
CY7C15631KV18 (7C1553K)	8910015	610920548	TAIWN-G	96	1321	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	500	178	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	178	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	178	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.25V Vcc							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	168	76	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	168	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	168	77	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	10	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-240mA							
CY7C1514KV18 (7C1553K)	8844020	610854680	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	9	0	
CY7C15631KV18 (7C1553K)	8911000	610922436	TAIWN-G	COMP	9	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	77	0	
STRESS: STRESS: TEMPRATURE HUMIDITY TEST, 85C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	

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Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SER – ALPHA PARTICLE, 3-TEPM, 3-VOLTAGE, @ 85C, Vcc Nom							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	3	0	
STRESS: X-SECTION/STEM XY AUDIT							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	1WF		

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Reliability Test Data

QTP #: 093202

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	COMP	8	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	1000	80	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	96	596	0	
CY7C15631KV18 (7C1553K)	8910015	610921676	TAIWN-G	96	711	0	
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	96	1795	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	168	190	0	
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	500	184	0	

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Reliability Test Data

QTP #: 095106

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	COMP	8	0	
CY7C1415KV18 (7C1415K)	8004016	611047805	CML-RA	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	COMP	9	0	
CY7C1415KV18 (7C1415K)	8004016	611047805	CML-RA	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1415KV18 (7C1415K)	8004016	611047805	CML-RA	COMP	5	0	
STRESS: ELECTRICAL PARAMETER ASSESSMENT, Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	COMP	12	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE REGULATOR ON (125C, 2.05V)							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	96	48	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	96	1533	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	168	177	0	
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	1000	177	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.05V							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	168	80	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	96	80	0	
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	168	80	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 2.85V, +/140mA							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	COMP	6	0	
CY7C1415KV18 (7C1415K)	8004016	611047805	CML-RA	COMP	6	0	

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Reliability Test Data

QTP #: 095106

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	500	80	0	
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	1000	80	0	
STRESS: SER – ALPHA PARTICLE, 3-TEMP @ 88C, Vcc Nom							
CY7C1412KV18 (7C1412K)	8002011	611017731	CML-RA	COMP	2	0	

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Document History Page

Document Title: 095106: LL65 36 MEG QDR/DDR SYNCHRONOUS PRODUCT QUALIFICATION REPORT
Document Number: 001-65172

Rev.	ECN No.	Orig. of Change	Description of Change
**	3081922	NSR	Initial spec release.
*A	3676358	NSR	Added device CY7C1411KV18 in the cover page in reference to memo GRW-387 and GRW-379. Removed Version 1.0 in the QTP#095106. Removed reference Cypress spec for the reliability test conditions.
*B	4020299	HSTO	Added device CY7C2245KV18 in the cover page in reference to memo GRW-405. Removed the "®" and "™" in the cover page. Sort part number in numerical order e.g. 7C12xx, 7C14xx, 7C2xxx in the cover page.
*C	4197107	JYF	Sunset review: Changed title of QA Engineering Director to Reliability Director in QTP title page; Updated division from MID to MPD; Complete re-write of Reliability Tests Performed table for template alignment.
*D	4577791	JYF	Sunset review: Updated QTP title page for template alignment.
*E	6912142	JYF	Sunset review: Deletion of obsolete spec and alignment to current template.