Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Cypress Semiconductor
Product Qualification Report

QTP# 063807 VERSION*D
Jan 2024

1 Meg Fast Asynchronous SRAM Family C9FD-3R Technology, Fab4	
CY7C106D / CY7C1006D	**1-Mbit (256K x 4) Static RAM**
CY7C107D / CY7C1007D	**1-Mbit (1M x 1) Static RAM**
CY7C109D / CY7C1009D	**1-Mbit (128K x 8 Static RAM**
CY7C1018DV33	**1-Mbit (128K x 8) Static RAM**
CY7C1019D	**1-Mbit (128K x 8) Static RAM**
CY7C1019DV33	**1-Mbit (128K x 8) Static RAM**
CY7C1020D / CY7C1020DV33	**512K (32K x 16) Static RAM**
CY7C1021D / CY7C1021DV33	**1-Mbit (64K x 16) Static RAM**
CY7C1399DV33	**256K (32K x 8) Static RAM**
CY7C194D	**256K (64K x 4) Static RAM**
CY7C197D	**256K (256K x 1) Static RAM**
CY7C199D	**256K (32K x 8) Static RAM**
CY7C185D	**64K (8K X 8) Static RAM**

Prepared By:
Su Zheng
Reliability Engineer

Reviewed By:
Yusaku Ohta
Reliability Manager

Approved By:
Yusaku Ohta
Reliability Director

PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
052207	C9FD-3R, Fab 4 New Process using CY7C104*D (4Meg Fast Synchronous SRAM) Product Family	Mar 06
063807	Qualify 1 Meg Fast Async Product Family in C9FD-3R Technology, Fab4	Sep 06
071204	Qualify 1 Meg Fast Async Rev. B Masks (MM1, LITRM and DDLICM)	Mar 07
080603	Qualify 1 Meg Fast Async Rev.B Mask DDLIM Fix	Apr 08
114503	Qualify PMM Mask Change for C9 1M Fast Async SRAM in C9FD- 3R Technology in Fab 4	Feb 12

PRODUCT DESCRIPTION (for qualification)	
Purpose: Qualify PMM Mask Change for C9 1M Fast Async SRAM in C9FD- 3R Technology in Fab 4	
Marketing Part #:	CY7C106/7/9D, CY7C1006/7/9D, CY7C1019/20/21D, CY7C1018/9/20/21DV33, CY7C1399DV33, CY7C194/7/9D
Device Description:	1 Megabit Fast Asynchronous SRAM
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION – C9FD-3R			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 100Å Ti / 3200Å Al / 300Å TiW Metal 2: 150Å Ti / 8000Å Al / 300Å TiW
Passivation Type and Materials:		1000Å Oxide TEOS / 9000Å Nitride	
Generic Process Technology/Design Rule (-drawn):		CMOS, Double Metal, 0.09 μ m	
Gate Oxide Material/Thickness (MOS):		23Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor -- Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/C9FD-3R	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
22-Lead PDIP, 24/28-Lead PDIP	MMT (X)
24-Lead SOJ	MMT (X)
28-Lead SOIC/SOJ	MMT (X), JCET-China (JT)
28/44-Lead TSOP	JCET-China (JT)
28/32-Lead SOJ	JCET-China (JT)
32-Lead TSOP	TAIWAN- T, JCET-China (JT)
44-Lead SOJ	JCET-China (JT)

Note: Package Qualification details upon request

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-R

Note: Please contact a Cypress Representative for other packages availability

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	ZW44
Package Outline, Type, or Name:	44-Lead Thin Small Outline Packages (Type II)
Mold Compound Name/Manufacturer:	Hitachi CEL9200CYRU
Mold Compound Flammability Rating:	NA
Mold Compound Alpha Emission Rate:	N/A
Oxygen Rating Index:	NA
Lead Frame Material:	Copper base
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	Back grind
Die Separation Method:	100% Saw Through
Die Attach Supplier:	Dexter
Die Attach Material:	QMI 509
Die Attach Method:	Epoxy
Bond Diagram Designation:	10-06664
Wire Bond Method:	Ultrasonic
Wire Material/Size:	Au, 0.8mil
Thermal Resistance Theta JA °C/W:	76.93°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	
Name/Location of Assembly (prime) facility:	Cypress Philippines (CML-R)
MSL Level	3
Reflow Profile	260C

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	AEC-Q100-008 and JESD22-A108 Dynamic Operating Condition, Vcc Max = 3.77V, 150°C	P
High Temperature Operating Life Latent Failure Rate	JESD22-A108 Dynamic Operating Condition, Vcc Max = 3.77V, 150°C	P
Long Life Verification	JESD22-A108 Dynamic Operating Condition, Vcc = 3.77V, 150°C	
High Temperature Steady State Life	JESD22-A108 Static Operating Condition, Vcc Max = 3.77V, 150°C	P
High Accelerated Saturation Test (HAST)	JESD22-A110, 130°C, 3.63V/3.77V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+ Reflow, 260°C+0, -5°C	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+ Reflow, 260°C+0, -5°C	P
Pressure Cooker	JESD22-A102, 121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+ Reflow, 260°C+0, -5°C	P
High Temperature Storage	JESD22-A103, 150°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	JESD22-A101, 500V	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	JEDEC JSTD-020	P
Static Latch up	JESD78, 125C, ± 200/300mA	P
Low Temperature Operating Life Cold Life Test	JESD22-A108 Dynamic Operating Condition, Vcc = 3.77 V, -30 C/-55 C, f = 4MHz	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	11, 720 Devices	2	N/A	N/A	171 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	2,481,000	6*	0.7	170	18 FIT

Note:
EFR data was from the GOOBI qualification completed in October 2010.
LFR data was from initial C9 technology/product qualification completed in March 2006 and met Cypress 31 FITs qualification requirement. Process improvements and test screens were implemented to fix and eliminate the defects.

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

* Failures are fixed with reference corrective action (CAR) # 200613035.

Reliability Test Data

QTP #: 052207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	15	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	15	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	10	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	10	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	10	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	48	1551	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	48	1518	1	LI DEFFECT
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	48	3314	1	NON-VISUAL
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	80	1544	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	500	1542	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	80	1516	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	500	1514	3	SINGLE BIT & BLOCKED CONTACT
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	80	1517	1	LOST REJECT
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	500	1511	2	SINGLE BIT
STRESS: LONG LIFE VERIFICATION, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	1000	400	0	
STRESS: HIGH TEMPERATURE STEADY STATE LIFE, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	80	80	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	168	80	0	
STRESS: HIGH TEMPERATURE STORAGE							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	500	50	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	1000	50	0	

Reliability Test Data

QTP #: 052207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	9	0	
CY7C1041D (7C1541N)	4538630	*610610603*	CML-R	COMP	9	0	
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	9	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	9	0	
CY7C1041D (7C1541N)	4530733	*610607231*	CML-R	COMP	9	0	
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	9	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	9	0	
CY7C1049DV33 (7C1349N)	4538680	*610611051*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	3	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	3	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	3	0	
CY7C1041D (7C1541N)	4530733	*610607231*	CML-R	COMP	3	0	
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	3	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	3	0	
CY7C1049DV33 (7C1349N)	4538680	*610611051*	CML-R	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-200mA							
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	3	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	3	0	
CY7C1046DV33 (7C1346N)	4538680	*610610605*	CML-R	COMP	3	0	
CY7C1049DV33 (7C1349N)	4538680	*610611051*	CML-R	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-300mA							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	3	0	

Reliability Test Data

QTP #: 052207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: STATIC LATCH-UP TESTING, 125C, 8.5V, +/-200mA							
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	3	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	3	0	
CY7C1041D (7C1541N)	4552229	*610617290*	CML-R	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	128	45	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	128	45	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	128	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	168	46	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	168	50	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	288	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	168	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	288	50	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	300	45	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	500	45	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	1000	45	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	300	50	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	500	50	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	1000	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	300	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	500	50	0	

Reliability Test Data

QTP #: 063807

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1021DV33 (7C1321N)	4533793	*610554885*	CML-R	COMP	9	0	
STRESS: AGE BOND STRENGTH							
CY7C1021DV33 (7C1321N)	4533347	*610517618*	CML-R	COMP	10	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1021DV33 (7C1321N)	4617244	*610646792*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1021DV33 (7C1321N)	4617244	*610646792*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1021DV33 (7C1321N)	4617244	*610646792*	CML-R	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-200mA							
CY7C1021DV33 (7C1321N)	4617244	*610646792*	CML-R	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.77V, Vcc Max							
CY7C1021DV33 (7C1321N)	4617244	*610646791*	CML-R	48	3392	1	SINGLE BIT
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1021DV33 (7C1321N)	4533793	*610554885*	CML-R	128	45	0	
CY7C1021DV33 (7C1321N)	4533793	*610554885*	CML-R	256	45	0	
STRESS: HIGH TEMPERATURE STORAGE							
CY7C1021DV33 (7C1321N)	4533347	*610517618*	CML-R	500	50	0	
CY7C1021DV33 (7C1321N)	4533347	*610517618*	CML-R	1000	50	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1021DV33 (7C1321N)	4533793	*610554885*	CML-R	168	50	0	
CY7C1021DV33 (7C1321N)	4533793	*610554885*	CML-R	288	50	0	
CY7C1021DV33 (7C1321N)	4533793	*610554885*	CML-R	500	45	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1021DV33 (7C1321N)	4533793	*610554885*	CML-R	300	50	0	
CY7C1021DV33 (7C1321N)	4533793	*610554885*	CML-R	500	50	0	
CY7C1021DV33 (7C1321N)	4533793	*610554885*	CML-R	1000	49	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE, -30C, 3.77V, 4MHz							
CY7C1021DV33 (7C1321N)	4533347	610517618	CML-R	500	45	0	

STRESS: LOW TEMP DYNAMIC OPERATING LIFE, -55C, 3.77V, 4MHz

CY7C1018DV33 (7CP1318NC)	4905383	612117959	CML-R	1000	32	0

Reliability Test Data

QTP #: 071204

Device		Fab Lot #	Duration	Results	Failure Mechanism
STRESS:	***E-TEST YIELD***				
7C1021P	(Rev. B)	4635387	COMP	COMPARABLE	
7C1021P	(Rev. B)	4702461	COMP	COMPARABLE	

Reliability Test Data

QTP #: 080603

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.77V, Vcc Max								
CY7C1021DV33 (7C1321N)	4752088	610807402	CML-R	48	3923	0		
CY7C1021DV33 (7C1321N)	4752088	610807403	CML-R	48	3904	2	LTIR Short	080603-1BE1
CY7C1021DV33 (7C1321N)	4752088	610807404	CML-R	48	3893	0		

Reliability Test Data

QTP #: **114503**

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: E-TEST							
7C1021PC	4140242	N/A	N/A	COMP	COMPARABLE		
STRESS: SORT YIELD							
7C1021PC	4140242	N/A	N/A	COMP	COMPARABLE		

Document History Page

Document Title: QTP 063807: 1 Meg Fast Asynchronous SRAM Family C9FD-3R Technology, Fab4
Document Number: 001-76197

Rev.	ECN No.	Orig. of Change	Description of Change
**	3528439	NSR	Initial spec release. Original latest qualification report is posted in memo HGA-601. Added QTP 114503 data.
*A	3920284	JYF	Removed Version 5.0 in QTP# 063807 title page; Deleted obsolete referenced spec 11-20047 in Major Package Information Table and replaced with 001-64160; Deleted INDNS-O and CML-R in Assembly Site Facility Table and replaced with JCET-China (JT); Updated Reliability Test Performed Table: -Deleted “3IR” in reflow step of HAST, PCT and TCT -Deleted Cypress’ referenced specs and replaced with industry standards -Deleted Current Density (internal requirement only)
*B	4305023	HSTO	Align qualification report based on the new template in the front page
*C	4678942	HSTO	Align qualification report based on the new template in the front page
*D	7995094	SUZH	Added LTOL -55C result.