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Cypress Semiconductor
Product Qualification Report

QTP# 051207 VERSION*A
June, 2014

18 MEG QDR SYNCHRONOUS SRAM FAMILY R9Q-3R TECHNOLOGY, FAB4	
CY7C1302DV25	9-Mbit Burst of Two Pipelined SRAMs with QDR™ Architecture
CY7C1304DV25	9-Mbit Burst of 4 Pipelined SRAM with QDR™ Architecture
CY7C1308DV25	9-Mbit 4-Word Burst SRAM with DDR-1 Architecture
CY7C1303BV25 CY7C1306BV25	18-Mbit Burst of 2 Pipelined SRAM with QDR™ Architecture
CY7C1305BV25 CY7C1307BV25	18-Mbit Burst of 4 Pipelined SRAM with QDR™ Architecture
CY7C1310BV18 CY7C1312BV18 CY7C1314BV18	18-Mbit QDR-II™ SRAM 2-Word Burst Architecture
CY7C1311BV18 CY7C1313BV18 CY7C1315BV18	18-Mbit QDR-II™ SRAM 4-Word Burst Architecture
CY7C1316BV18 CY7C1318BV18 CY7C1320BV18	18-Mbit DDR-II SRAM 2-Word Burst Architecture
CY7C1317BV18 CY7C1319BV18 CY7C1321BV18	18-Mbit DDR-II SRAM 4-Word Burst Architecture
CY7C1392BV18 CY7C1393BV18 CY7C1394BV18	18-Mbit DDR-II SIO SRAM 2-Word Burst Architecture
CY7C1323BV25	18-Mb 4-Word Burst SRAM with DDR-I Architecture

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
033302	New Technology R9T-3R, Fab 4 and New Device CY7C137*/138*E, 18 Meg Synchronous product family	Sep 04
051207	R9 18 Meg QDR, 7C1313D 4 Metal Layer Process	Mar 05

PRODUCT DESCRIPTION (for qualification)			
Purpose: Qualify CY7C1313D, 18Meg QDR Synchronous Product Family in qualified Technology R9Q-3R, Fab 4			
Marketing Part #:	CY7C1310/2/4BV18, CY7C1311/3/5BV18, CY7C1316/8/20BV18, CY7C1317/9/21BV18, CY7C1392/3/4BV18, CY7C1305/7BV25, CY7C1303/6BV25, CY7C1302DV25, CY7C1304DV25, CY7C1308DV25, CY7C1323BV25		
Device	2.5V, 3.3V, Commercial and Industrial		
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. D	
What ID markings on Die:	7C1313C		

TECHNOLOGY/FAB PROCESS DESCRIPTION – R9Q-3R			
Number of Metal Layers:	4	Metal Composition:	Metal 1: 150Å Ti /3200Å Al / 300Å TiW Metal 2: 150Å Ti /6000 Å Al / 300Å TiW Metal 3: 150Å Ti / 6000Å Al / 300Å TiW Metal 4: 150Å Ti / 8000Å Al / 300Å TiW
Passivation Type and Materials:			1000Å Oxide TEOS / 9000Å Nitride
Free Phosphorus contents in top glass layer (%):			0%
Number of Transistors in Device			~120M
Number of Logic Gates in Device			~40M
Generic Process Technology/Design Rule (µ-drawn):			CMOS, Triple Metal, 90 nm
Gate Oxide Material/Thickness (MOS):			Nitridized SiO_2, 22Å
Name/Location of Die Fab (prime) Facility:			Cypress Semiconductor - Bloomington, MN
Die Fab Line ID/Wafer Process ID:			Fab4/R9Q-3R

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
165-Ball FBGA	**TAIWAN-G, CML-RA**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165 (13X15)
Package Outline, Type, or Name:	165-Ball Fine Pitch Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	PLASKON / SMT-B1-LAS
Mold Compound Flammability Rating:	V-0 per UL94
Oxygen Rating Index:	>28%
Substrate Material:	BT
Lead Finish, Composition / Thickness:	Solder Ball, 63% Sn, 37% Pb
Die Backside Preparation	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	2025D
Die Attach Method:	Epoxy
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0mil
Thermal Resistance Theta JA °C/W:	20.7°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41034
Name/Location of Assembly (prime) facility:	ASE-Taiwan

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	KYEC,Taiwan, CML-RA
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 150°C Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 125°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max (Core)=2.25V, 150°C JESD22-A108	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max=2.25V, 150°C JESD22-A108	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 2.45V, -30°C JESD22-A108	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130°C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260C Reflow)	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260C Reflow)	P
Pressure Cooker	JESD22-A102, 121°C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260C Reflow)	P
High Temperature Storage	JESD22-A103:150 C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260C Reflow)	P
Dynamic Latch-Up	JESD78	P
Static Latch-Up	125C, ± 300mA JESD78	P

RELIABILITY FAILURE RATE SUMMARY

Stress/ Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	1,803 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	599,051 DHRs	0	0.7	170	9 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4323794	*610348235*	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1370DV33 (7C1370E)	4421235	*610447674*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	COMP	5	0	
STRESS: BALL SHEAR							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: BOND PULL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4421235	*610446833*	CML-R	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	9	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	500	47	0	
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	1000	47	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	48	193	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	48	951	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	48	1246	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	48	1382	1	Non-Visual
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	500	170	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	500	400	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	500	400	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 3.63V, Vcc Max							
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	80	85	0	
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	168	85	0	
STRESS: INTERNAL VISUAL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	5	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.45V, Vcc							
CY7C1470V33 (7C1470A)	4333765	*610349455*	CML-R	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	168	50	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	168	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	168	43	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	128	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	128	47	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	128	44	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/300mA							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	300	50	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	500	49	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	1000	49	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	300	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	500	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	1000	42	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	300	34	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	500	33	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	1000	33	0	
STRESS: THERMAL SHOCK							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	100	46	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	200	46	0	
STRESS: X-RAY							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	15	0	

Reliability Test Data

QTP #: 051207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1314BV18 (7C1314D)	4444085	*610507866*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1314BV18 (7C1314D)	4444085	*610507866*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1314BV18 (7C1314D)	4444085	*610507866*	TAIWN-G	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.25V, Vcc Max (Core)							
CY7C1312BV18 (7C1312D)	4440030	*610465503*	TAIWN-G	96	1803	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 2.25V, Vcc Max (Core)							
CY7C1312BV18 (7C1312D)	4440030	*610465503*	TAIWN-G	168	1395	0	
CY7C1312BV18 (7C1312D)	4440030	*610465503*	TAIWN-G	500	359	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1313BV18 (7C1313D)	4436152	*610459993*	TAIWN-G	168	50	0	
CY7C1313BV18 (7C1313D)	4436152	*610459993*	TAIWN-G	288	50	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 4.5V, +/300mA							
CY7C1314BV18 (7C1314D)	4444085	*610507866*	TAIWN-G	COMP	3	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1313BV18 (7C1313D)	4436152	*610459993*	TAIWN-G	300	50	0	
CY7C1313BV18 (7C1313D)	4436152	*610459993*	TAIWN-G	500	50	0	
CY7C1313BV18 (7C1313D)	4436152	*610459993*	TAIWN-G	1000	50	0	

Document History Page

Document Title: QTP # 051207 : 18 MEG QDR SYNCHRONOUS SRAM (CY7C1313D PRODUCT FAMILY), R9Q-3R TECHNOLOGY , FAB 4
Document Number: 001-88010

Rev.	ECN No.	Orig. of Change	Description of Change
**	4033646	ILZ	Initial Spec Release Qualification report published on Cypress.com is documented on memo HGA-457 and not in spec format. Initiated spec for QTP 051207 and all data from memo# HGA-457 was transferred to qualification report spec template. Deleted package qualification details on package qualification history table. Deleted Cypress reference Spec and replaced with Industry Standards Updated package availability based on current qualified test & assembly site.
*A	4419250	JYF	Sunset review: Updated QTP title page and Reliability Tests Performed table (EFR/LFR, HTSSL, LTOL, HAST, TCT, PCT, HTS, Acoustic Microscopy, Dynamic/Static Latch-Up) for template alignment; Updated device division from MID to MPD.

Distribution: WEB

Posting: None