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Cypress Semiconductor
Product Qualification Report

QTP# 044102
June 2013

SYNCHRONOUS DUAL PORT RAM FAMILY
CY7C085XV / CY7C083XV / CYDXXS18V / CYDXXS36V / CYDXXS72V
R7FT-3R TECHNOLOGY, FAB 4

CY7C0830AV/CY7C0831AV CY7C0832AV/CY7C0833AV CY7C0837AV	**FLEx18™ 3.3V 64K/128K x 36 and 128K/256K x 18 Synchronous Dual-Port RAM**
CYD01S18V/CYD02S18V CYD04S18V/CYD09S18V	**FLEx18™ 3.3V 64K/128K/256K/512K x 18 Synchronous Dual-Port RAM**
CY7C0850AV/CY7C0851AV CY7C0852AV/CY7C0853AV	**FLEx36™ 3.3V 32K/64K/128K/256K x 36 Synchronous Dual-Port RAM**
CYD01S36V/CYD02S36V CYD04S36V/CYD09S36V CYD18S36V	**FLEx36™ 3.3V 32K/64K/128K/256K/512 x 36 Synchronous Dual-Port RAM**
CYD047S72V/CYD09S72V CYD18S72AV	**FLEx72™ 3.3V 64K/128K/256K x 72 Synchronous Dual-Port RAM**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Zhaomin Ji
Principal Reliability Engineer
(408) 432-7021

Mira Ben-Tzur
Quality Engineering Director
(408) 943-2675

PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
014807	New Technology Derivative R7FT-3R (Hot Al) / Synchronous Dual-Port RAM CY7C0852V, product family and package option.	Feb 02
020709	Process R7FT-3R with Via 2 W Plug (4 Meg Dual Port)	Apr 02
023101	9 Meg Sync Dual Port Stacked Die, R7FT-3R, 172-ball FBGA (15mm x 15mm x 1.25mm), ASE Taiwan Assembly, MSL3	Dec 02
032406	18 Meg Dual Port 2 Stacked Die (4- 4 Meg die), R7FT-3R, 484-ball FBGA, MSL3 Assembled @ASE-Taiwan	Dec 03
033202	Increased Polyimide thickness of 10um max from 5-6um	Mar 04
044104	6 micron Polyimide thickness for 18 Meg (4-4) die fabricated @ Fab4, 484-ball FBGA	Nov 04
041505	8 micron Polyimide thickness for 18 Meg (4-4) die fabricated @ Fab4, 484-ball FBGA	Nov 04
044102	18Meg to 1/2Meg Functionality Mask Change, R7FT-3R Technology from Fab4	Jun 05

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose:	Device Functionality Mask Change on 18Meg to ½ Meg Synchronous Dual-Port RAM Family & options, R7FT-3R	
Marketing Part #:	CY7C0830/1/2/3/7AV, CY7C0850/1/2/3AV, CYD01/2/4/9S18V, CYD01/2/4/9S36V, CYD18S36V CYD04/9S72V, CYD18S72AV	
Device Description:	Synchronous Dual Port RAM, 3.3V, Commercial and Industrial available in 120/176-Lead TQFP, 144/172/256/484-Ball FBGA package.	
Cypress Division:	Cypress Semiconductor Corporation –Data Com Division (DCD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. B
What ID markings on Die:	7C08524B	

TECHNOLOGY/FAB PROCESS DESCRIPTION – R7FT-3R			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 150Å Ti / 4,200Å Al / 300Å TiW Metal 2: 150Å Ti /4,200 Å Al / 300Å TiW Metal 3: 150Å Ti / 8,000Å Al / 300Å TiW
Passivation Type and Materials:			1000Å TEOS / 9000Å PECVD Nitride
Free Phosphorus contents in top glass layer (%):			0%
Number of Transistors in Device			62 million
Number of Gates in Device			112K
Generic Process Technology/Design Rule (-drawn):			CMOS, Triple Metal /0.18 um
Gate Oxide Material/Thickness (MOS):			SiO_2, 32Å
Name/Location of Die Fab (prime) Facility:			Cypress Semiconductor -- Bloomington, MN
Die Fab Line ID/Wafer Process ID:			RAM7FT-3R

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
144/172/256/484-Ball BGA	**ASE Taiwan**
120/176-Lead TQFP	**ASE Taiwan**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB172
Package Outline, Type, or Name:	172-ball, Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	PLASKON SMT-B-1
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	Solder Ball, 63%Sn, 37%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8355F
Die Attach Method:	Silver Epoxy
Bond Diagram Designation:	10-04267
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	17C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41020
Name/Location of Assembly (prime) facility:	ASE Taiwan

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	ASE Taiwan (TAIWN-G), KYEC, CHIPMOS
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.3V, 150^{0}C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 2.3V, 150^{0}C	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max = 3.63V, 150^{0}C	P
High Accelerated Saturation Test (HAST)	130^{0}C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220^{0}C +0, -5^{0}C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65^{0}C to 150^{0}C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220^{0}C +0, -5^{0}C	P
Pressure Cooker	121^{0}C, 100%RH Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220□C+0, -5^{0}C	P
High Temperature Storage	150^{0}C, No bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JESD22, Method A114-B	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1,100V, 2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101C	P
Age Bond Strength	200C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Dynamic Latch up	In accordance with JEDEC 17	P
Static Latch up	125C, 300mA In accordance with JEDEC 17	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate[1]	996 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1, 2] Long Term Failure Rate	445,840 DHRs	0	0.7	170	12 FIT

[1] A production burn-in of 30 Hrs at 125C, 2.7V is required for the product.
[2] Assuming an ambient temperature of 55C and a junction temperature rise of 15C.
[3] Chi-squared 60% estimations used to calculate the failure rate.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism. k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #:014807

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C0852V (7C08523A)	4130707	*610133760L1*	TAIWAN-G	COMP	15	0	
CY7C0852V (7C08523A)	4131840	*610135256*	TAIWAN-G	COMP	15	0	
CY7C0852V (7C08523A)	4131841	*610137123L1*	TAIWAN-G	COMP	15	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.3V, Vcc Max							
CY7C0852V (7C08523A)	4131841	*610137123L1*	TAIWAN-G	48	772	0	
CY7C0852V (7C08523A)	4141878	*610145152*	TAIWAN-G	96	455	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.3V, Vcc Max							
CY7C0852V (7C08523A)	4131840	*610135256*	TAIWAN-G	80	300	0	
CY7C0852V (7C08523A)	4131840	*610135256*	TAIWAN-G	500	274	0	
CY7C0852V (7C08523A)	4131841	*610137123L1*	TAIWAN-G	80	400	0	
CY7C0852V (7C08523A)	4131841	*610137123L1*	TAIWAN-G	500	193	0	
CY7C0852V (7C08523A)	4133371	*610137695*	TAIWAN-G	80	400	0	
CY7C0852V (7C08523A)	4133371	*610137695*	TAIWAN-G	500	385	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 1,100V							
CY7C0852V (7C08523A)	4133371	*610137695*	TAIWAN-G	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C0852V (7C08523A)	4133371	*610137695*	TAIWAN-G	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 10V, +/300mA							
CY7C0852V (7C08523A)	4130707	*610133760L1*	TAIWAN-G	COMP	3	0	
CY7C0852V (7C08523A)	4131840	*610135256*	TAIWAN-G	COMP	3	0	
STRESS: AGE BOND STRENGTH							
CY7C0852V (7C08523A)	4130707	*610133760L1*	TAIWAN-G	COMP	5	0	
CY7C0852V (7C08523A)	4131840	*610135256*	TAIWAN-G	COMP	6	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C0852V (7C08523A)	4128335	*610130788*	TAIWAN-G	500	48	0	
CY7C0852V (7C08523A)	4128335	*610130788*	TAIWAN-G	1000	48	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 3.63V, Vcc MAX							
CY7C0852V (7C08523A)	4130707	*610133760L1*	TAIWAN-G	80	78	0	
CY7C0852V (7C08523A)	4130707	*610133760L1*	TAIWAN-G	168	76	0	

Reliability Test Data

QTP #:014807

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C0852V (7C08523A)	4131840	*610135256*	TAIWAN-G	168	47	0	
CY7C0852V (7C08523A)	4131841	*610137123L1*	TAIWAN-G	168	48	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C0852V (7C08523A)	4131840	*610135256*	TAIWAN-G	128	48	0	
CY7C0852V (7C08523A)	4131841	*610137123L1*	TAIWAN-G	128	46	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C0852V (7C08523A)	4130707	*610133760L1*	TAIWAN-G	300	47	0	
CY7C0852V (7C08523A)	4130707	*610133760L1*	TAIWAN-G	500	46	0	
CY7C0852V (7C08523A)	4130707	*610133760L1*	TAIWAN-G	1000	45	0	
CY7C0852V (7C08523A)	4131841	*610137123L1*	TAIWAN-G	300	46	0	
CY7C0852V (7C08523A)	4131841	*610137123L1*	TAIWAN-G	500	45	0	

Reliability Test Data

QTP #:044102

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C0852AV (7C08523D)	4452211	*610507578*	TAIWAN-G	COMP	15	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C0852AV (7C08523D)	4452211	*610507578*	TAIWAN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V							
CY7C0852AV (7C08523D)	4452211	*610507578*	TAIWAN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C0852AV (7C08523D)	4452211	*610507578*	TAIWAN-G	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING (125C, 7.5V, +/-300mA)							
CY7C0852AV (7C08523D)	4452211	*610507578*	TAIWAN-G	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.3V, Vcc Max							
CY7C0832AV (7C08323C)	4508357	*610519474*	TAIWAN-G	96	101	0	
CY7C0832AV (7C08323C)	4508357	*610518574*	TAIWAN-G	96	895	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C0852AV (7C08523D)	4452211	*610507578*	TAIWAN-G	168	48	0	
CY7C0852AV (7C08523D)	4452211	*610507578*	TAIWAN-G	288	48	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C0852AV (7C08523D)	4452211	*610507578*	TAIWAN-G	300	48	0	
CY7C0852AV (7C08523D)	4452211	*610507578*	TAIWAN-G	500	48	0	
CY7C0852AV (7C08523D)	4452211	*610507578*	TAIWAN-G	1000	48	0	

Document History Page

Document Title: QTP # 044102 : SYNCHRONOUS DUAL PORT RAM FAMILY (CY7C085XV / CY7C083XV / CYDXXS18V / CYDXXS36V / CYDXXS72V), R7FT-3R TECHNOLOGY, FAB 4
Document Number: 001-87913

Rev.	ECN No.	Orig. of Change	Description of Change
**	4026890	ILZ	Initial Spec Release Qualification report published on Cypress.com is documented on memo LGQ-279 in spec format. Initiated spec for QTP 044102 data from LGQ-279 was transferred to qualification report spec template. Deleted package qualification details on package qualification history table Deleted Cypress reference Spec and replaced with Industry Standards Updated package availability based on current qualified test & assembly site

Distribution: WEB

Posting: None