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Cypress Semiconductor
Product Qualification Report
QTP# 041608 VERSION*C
February 2025

1/2/4 Meg Synchronous SRAM Family Technology R9T-3R, Fab4	
CY7C1212H	1-Mbit (64K x 18) Pipelined Sync SRAM
CY7C1214H	1-Mbit (32K x 32) Flow-Through Sync SRAM
CY7C1215H	1-Mbit (32K x 32) Pipelined Sync SRAM
CY7C1217H	1-Mbit (32K x 36) Flow-Through Sync SRAM
CY7C1218H	1-Mbit (32K x 36) Pipelined Sync SRAM
CY7C1219H	1-Mbit (32K x 36) Pipelined DCD Sync SRAM
CY7C1297H	1-Mbit (64K x 18) Flow-Through Sync SRAM
CY7C1298H	1-Mbit (64K x 18) Pipelined DCD Sync SRAM
CY7C1223H	2-Mbit (128K x 18) Pipelined DCD Sync SRAM
CY7C1231H	2-Mibt (128K x 18) Flow Through SRAM with NoBL™ Architecture
CY7C1324H	2-Mbit (128K x 18) Flow-Through Sync SRAM
CY7C1325H	256Kx18 Flow-Through Synchronous SRAM
CY7C1326H	2-Mbit (128K x 18) Pipelined Sync SRAM
CY7C1329H	2-Mbit (64K x 32) Pipeline Sync SRAM
CY7C1333H	2-Mbit (64K x 32) Flow-Through SRAM with NoBL™ Architecture
CY7C1334H	2-Mbit (64K x 32) Pipelined SRAM with NoBL™ Architecture
CY7C1336H	2-Mbit (64K x 32) Flow-Through Sync SRAM
CY7C1344H	2-Mbit (64K x 36) Flow-Through Sync SRAM
CY7C1346H	2-Mbit (64K x 36) Pipelined Sync SRAM
CY7C1325G	256Kx18 Flow-Through Synchronous SRAM
CY7C1327G	256Kx18 Pipelined Synchronous SRAM
CY7C1328G	256Kx18 Pipelined Double-Cycle-Deselect Synchronous SRAM
CY7C1338G	128Kx32 Flow-Through Synchronous SRAM
CY7C1339G	128Kx32 Pipelined Synchronous SRAM
CY7C1340G	128Kx32 Pipelined Double-Cycle-Deselect Synchronous SRAM
CY7C1345G	128Kx36 Flow-Through Synchronous SRAM
CY7C1347G	128Kx36 Pipelined Synchronous SRAM
CY7C1348G	128Kx36 Pipelined Double-Cycle-Deselect Synchronous SRAM
CY7C1350G	128Kx36 Pipelined Synchronous SRAM with NoBLTM Architecture
CY7C1351G	128Kx36 Flow-Through Synchronous SRAM with NoBLTM Architecture
CY7C1352G	256Kx18 Pipelined Synchronous SRAM with NoBLTM Architecture
CY7C1353G	256Kx18 Flow-Through Synchronous SRAM with NoBLTM Architecture

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
033302	New Technology R9T-3R, Fab 4, and New Device CY7C137*/138*D (18Meg) Synchronous product family	Sept 04
041608	New Device CY7C1347G Synchronous product family in R9T-3R Technology, Fab 4	Sept 04
071007	Double Via Mask Layer Change (550GGC (MM2), 560GGC (VIM2), 570GGB (MM3) for R9T-3R	Apr 07

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product.

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualify CY7C1347G and product family in qualified technology R9T-3R, Fab 4	
Marketing Part #:	CY7C1231H, CY7C1325G, CY7C1327G, CY7C1328G, CY7C1338G, CY7C1339G, CY7C1340G, CY7C1345G, CY7C1347G, CY7C1348G, CY7C1350G, CY7C1351G, CY7C1352G, CY7C1353G, CY7C1212H, CY7C1214H, CY7C1215H, CY7C1217H, CY7C1218H, CY7C1219H, CY7C1223H, CY7C1297H, CY7C1298H, CY7C1324H, CY7C1325H,CY7C1326H, CY7C1329H, CY7C1333H, CY7C1334H, CY7C1336H, CY7C1344H, CY7C1346H
Device Description:	1.8V, 2.5V, 3.3V, Commercial and Industrial
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION – R9T-3R			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 150Å Ti /3200Å Al / 300Å TiW Metal 2: 150Å Ti /6000 Å Al / 300Å TiW Metal 3: 150Å Ti / 8,000Å Al / 300Å TiW
Passivation Type and Materials:			1000Å Oxide TEOS / 9000Å Nitride
Generic Process Technology/Design Rule (□-drawn):			CMOS, Triple Metal, 90 nm
Gate Oxide Material/Thickness (MOS):			Nitridized SiO_2, 23Å
Name/Location of Die Fab (prime) Facility:			Cypress Semiconductor -- Bloomington, MN
Die Fab Line ID/Wafer Process ID:			Fab4/R9T-3R

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
100-Lead TQFP	**JCET-China (JT)**

Note: Package Qualification details upon request.

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	A100
Package Outline, Type, or Name:	100-Pin Thin Quad Flat Pack (TQFP)
Mold Compound Name/Manufacturer:	Hitachi CEL9200HF9-Uv80
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Dexter
Die Attach Material:	QMI 509
Die Attach Method:	Epoxy
Bond Diagram Designation:	10-06166
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0mil
Thermal Resistance Theta JA °C/W:	41.7°C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	JCET-China (JT)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Cypress Philippines (CML-R)

Note: Please contact a Cypress Representative for other package availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.25V, 150°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 2.25V, 150°C JESD22-A108	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max = 2.25V, 150°C JESD22-A108	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 6.50V, -30°C JESD22-A108	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130°C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
Pressure Cooker	JESD22-A102: 121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
High Temperature Storage	JESD22-A103: 150°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020	P
Dynamic Latch up	JESD78	P
Static Latch up	125C, ± 300mA JESD78	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	8,331 Devices	2	N/A	N/A	240 PPM
High Temperature Operating Life[1, 2] Long Term Failure Rate	485,000 DHRs	0	0.7	170	11 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
K = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1470-AC (7C1470A)	4330156	*610417279*	CML-PHIL	COMP	15	0	
CY7C1470-AC (7C1470A)	4321389	*610417280*	CML-PHIL	COMP	15	0	
CY7C1470-AC (7C1470A)	4323794	*610348235*	ASE-TAIWN	COMP	15	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Core							
CY7C1370-AC (7C1370E)	4345377	*610424939*	CML-PHIL	48	193	0	
CY7C1370-AC (7C14E0E)	4345377	*610422227*	CML-PHIL	48	951	0	
CY7C1370-AC (7C1370E)	4406200	*610435906*	CML-PHIL	48	1246	0	
CY7C1370-AC (7C1370E)	4410258	*610437891*	CML-PHIL	48	1382	1	Non-Visual
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.25V, Vcc Core							
CY7C1370-AC (7C1370E)	4345377	*610424939*	CML-PHIL	500	170	0	
CY7C1370-AC (7C1370E)	4406200	*610435906*	CML-PHIL	500	400	0	
CY7C1370-AC (7C1370E)	4410258	*610437891*	CML-PHIL	500	400	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 6.50V, Vcc							
CY7C1470-AC (7C1470A)	4333765	*610349455*	CML-PHIL	500	45	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1470-AC (7C1470A)	4352888	*610425832*	ASE-TAIWN	COMP	3	0	
CY7C1470-AC (7C1470A)	4401980	*610425833*	ASE-TAIWN	COMP	3	0	
CY7C1370-AC (7C1370E)	4345377	*610417723*	CML-PHIL	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1470-AC (7C1470A)	4352888	*610425832*	ASE-TAIWN	COMP	9	0	
CY7C1470-AC (7C1470A)	4401980	*610425833*	ASE-TAIWN	COMP	9	0	
CY7C1370DV33 (7C1370E)	4421235	*610446833*	CML-R	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1470-AC (7C1470A)	4352888	*610425832*	ASE-TAIWN	COMP	9	0	
CY7C1470-AC (7C1470A)	4401980	*610425833*	ASE-TAIWN	COMP	9	0	
CY7C1370-AC (7C1370E)	4345377	*610417723*	CML-PHIL	COMP	9	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/300mA							
CY7C1470-AC (7C1470A)	4352888	*610425832*	ASE-TAIWN	COMP	3	0	
CY7C1470-AC (7C1470A)	4401980	*610425833*	ASE-TAIWN	COMP	3	0	
CY7C1370-AC (7C1370E)	4345377	*610417723*	CML-PHIL	COMP	3	0	
STRESS: AGE BOND STRENGTH							
CY7C1370-AC (7C1370E)	4421235	*610447674*	CML-PHIL	COMP	5	0	
CY7C1370-AC (7C1370E)	4406200	*610435906*	CML-PHIL	COMP	5	0	
CY7C1370-AC (7C1370E)	4410258	*610437891*	CML-PHIL	COMP	5	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1470-AC (7C1470A)	4323794	*610348234*	ASE-TAIWN	500	47	0	
CY7C1470-AC (7C1470A)	4323794	*610348234*	ASE-TAIWN	1000	47	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1470-AC (7C1470A)	4405088	*610418824*	ASE-TAIWN	80	85	0	
CY7C1470-AC (7C1470A)	4405088	*610418824*	ASE-TAIWN	168	85	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370-AC (7C1370E)	4345377	*610422227*	CML-PHIL	168	50	0	
CY7C1370-AC (7C1370E)	4406200	*610435906*	CML-PHIL	168	50	0	
CY7C1470-AC (7C1470A)	4321389	*610417278*	CML-PHIL	168	43	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370-AC (7C1370E)	4406200	*610435906*	CML-PHIL	128	50	0	
CY7C1470-AC (7C1470A)	4321389	*610417278*	CML-PHIL	128	47	0	
CY7C1470-AC (7C1470A)	4330156	*610417279*	CML-PHIL	128	44	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1370-AC (7C1370E)	4345377	*610422227*	CML-PHIL	300	50	0	
CY7C1470-AC (7C1470A)	4330156	*610417279*	CML-PHIL	300	43	0	
CY7C1470-AC (7C1470A)	4321389	*610417280*	CML-PHIL	300	34	0	

Reliability Test Data

QTP #: 041608

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Core							
CY7C1350G-AC (7C1350G)	4417192	*610430020*	CML-PHIL	48	3078	1	Non-visual
CY7C1350G-AC (7C1350G)	4417192	*610431300*	CML-PHIL	48	1479	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1350G-AC (7C1350G)	4421308	*610444228*	CML-PHIL	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1350G-AC (7C1350G)	4421308	*610444228*	CML-PHIL	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1350G-AC (7C1350G)	4421308	*610444228*	CML-PHIL	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8V, +/300mA							
CY7C1350G-AC (7C1350G)	4421308	*610444228*	CML-PHIL	COMP	3	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1350G-AC (7C1350G)	4417192	*610430020*	CML-PHIL	168	50	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1350G-AC (7C1350G)	4417192	*610430020*	CML-PHIL	300	50	0	

Reliability Test Data

QTP #: 071007

Device	Fab Lot #	Assy Lot #	Duration	Results
STRESS: CLASS YIELD				
7C1347G	4538418	VARIOUS	COMP	COMPARABLE
STRESS: SORT YIELD				
7C1347G	4538418	VARIOUS	COMP	COMPARABLE

Document History Page

Document Title: QTP 041608: 1/2/4 MEG SYNCHRONOUS SRAM FAMILY TECHNOLOGY R9T-3R, FAB4
Document Number: 001-84623

Rev.	ECN No.	Orig. of Change	Description of Change
**	3810634	NSR	Initial Spec Release.
*A	4039427	JYF	Added CY7C1325H part no. in the qual report device coverage; Updated Assembly Site Facility from CML-R to JCET-China (JT) in Package Availability table; Updated Major Package Information table: - Deleted obsolete spec 11-21009 and replaced with 001-64160; - Deleted CML-R and replaced with JCET-China (JT).
*B	4577791	JYF	Sunset review: Updated QTP title page for template alignment.
*C	8101861	JYF CHONGK AHHUAN	Sunset review: Removed obsolete spec 001-64160 Updated logo to IFX on header. Removed Distribution and Posting in document history page.