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Cypress Semiconductor
Product Qualification Report

QTP# 033302
February 2013

18 Meg Synchronous SRAM Family Technology R9T-3R, Fab4	
CY7C1370D CY7C1372D	18-Mbit (512K x 36/1M x 18) Pipelined SRAM with NoBL™ Architecture
CY7C1370DV25 CY7C1372DV25	18-Mbit (512K x 36/1M x 18) Pipelined SRAM with NoBL™ Architecture
CY7C1371D CY7C1373D	18-Mbit (512K x 36/1M x 18) Flow-Through SRAM with NoBL™ Architecture
CY7C1371DV25 CY7C1373DV25	18-Mbit (512K x 36/1M x 18) Flow-Through SRAM with NoBL™ Architecture
CY7C1371DV33	18-Mbit (512 K X 36) Flow-Through SRAM with NoBL™ Architecture
CY7C1380D, CY7C1380F CY7C1382D, CY7C1382F	18-Mbit (512K x 36/1M x 18) Pipelined SRAM
CY7C1380DV25 CY7C1382DV25 CY7C1380DV33	18-Mbit (512K x 36/1M x 18) Pipelined SRAM
CY7C1381D, CY7C1381F CY7C1383D, CY7C1383F	18-Mbit (512K x 36/1M x 18) Flow-Through SRAM
CY7C1381DV25 CY7C1383DV25	18-Mbit (512K x 36/1M x 18) Flow-Through SRAM
CY7C1386D CY7C1387D	18-Mbit (512K x 36/1M x 18) Pipelined DCD Sync SRAM
CY7C1386DV25 CY7C1387DV25	18-Mbit (512K x 36/1M x 18) Pipelined DCD Sync SRAM
CY7C1384D	18M 3.3V Sync 512x32 Pipeline
CY7C1385D	18M 3.3V Sync 512x32 Flowthrough

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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Quality Engineering Director
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Principal Reliability Engineer
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PRODUCT QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
033302		New Technology R9T-3R, Fab 4, and New Device CY7C137*/138*E (18Meg) Synchronous product family		Sep 04
042205		New Device CY7C1360C, (9 Meg) Synchronous Product Family in R9T-3R Technology, Fab 4		Sep 04
053405		CY7C1360CC, 9Meg Synchronous Product Family in R9T-3R Technology, GOOBI		Sep 05

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product.

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: Qualify CY7C1360C Synchronous Product Family in qualified Technology R9T-3R, Fab 4			
Marketing Part #:	CY7C1354C, CY7C1355C, CY7C1356C, CY7C1357C, CY7C1354CV25, CY7C1356CV25, CY7C1360C, CY7C1361C, CY7C1362C, CY7C1363C, CY7C1364C, CYC71365C, CY7C1366C, CYC71367C, CY7C1368C, CYC71378C, CY7C1379C, CY7C1371DV33, CY7C1380DV33		
Device Description:	2.5V, 3.3V, Commercial and Industrial		
Cypress Division:	Cypress Semiconductor Corporation –Memory & Image Division (MID)		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. C	
What ID markings on Die:	7C1360C		

TECHNOLOGY/FAB PROCESS DESCRIPTION – R9T-3R			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 100ª CoTi, 3200ª Al, 300ª TiW Metal 2: 150Å Ti / 6000Å Al / 300Å TiW Metal 3: 150Å Ti / 8000Å Al / 300Å TiW
Passivation Type and Materials:		1000Å Oxide TEOS / 9000Å Nitride	
Free Phosphorus contents in top glass layer (%):		0%	
Number of Transistors in Device		~5.8.E+07	
Number of Logic Gates in Device		~1.2.E+06	
Generic Process Technology/Design Rule (µ-drawn):		CMOS, Triple Metal, 90 nm	
Gate Oxide Material/Thickness (MOS):		Nitridized SiO_2, 23Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor – Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R9T-3R	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
100-Lead TQFP	**CML-R**
119/165-Ball BGA	**TAIWN-G**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION		
Package Designation:	BG119	BY119
Package Outline, Type, or Name:	119-Ball BGA	
Mold Compound Name/Manufacturer:	G770-J	
Mold Compound Flammability Rating:	V-O per UL94	
Oxygen Rating Index:	NA	
Lead Frame Material:	BT Resin (Substrate)	
Lead Finish, Composition / Thickness:	SnPb	SnAgCu
Die Backside Preparation Method/Metallization:	Backgrind	
Die Separation Method:	100% Sawing	
Die Attach Supplier:	Ablebond	
Die Attach Material:	2100A	
Die Attach Method:	Epoxy Dispense	
Bond Diagram Designation:		
Wire Bond Method:	Thermosonic	
Wire Material/Size:	Au. 1.0mil	
Thermal Resistance Theta JA °C/W:	18.6°C/W	
Package Cross Section Yes/No:	N/A	
Assembly Process Flow:	49-41046	
Name/Location of Assembly (prime) facility:	Taiwan-G	
MSL Level	3	3
Reflow Profile	220C	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Cypress Philippines (CML-R),

Note: Please contact a Cypress Representative for other packages availability

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	A100
Package Outline, Type, or Name:	100-Thin Quad Flat Pack (TQFP)
Mold Compound Name/Manufacturer:	Hitachi CEL9200HF9-Uv80
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Ni-Pd-Au
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Dexter
Die Attach Material:	QMI 509
Die Attach Method:	Epoxy
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au. 1.0mil
Thermal Resistance Theta JA °C/W:	28.66°C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	Cypress Philippines (CML-R)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Cypress Philippines (CML-R)

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.25V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max=2.25V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max=2.25V, 150°C	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 6.50V, -30°C	P
High Accelerated Saturation Test (HAST)	130°C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Pressure Cooker	121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow**, 260°C**+0, -5°C	P
High Temperature Storage	150°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114-B	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020	P
Dynamic Latchup	JESD78	P
Static Latchup	125C, ± 300mA JESD78	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	3,772 Devices	1	N/A	N/A	265 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	485,000 DHRs	0	0.7	170	11 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
K = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4323794	*610348235*	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1370DV33 (7C1370E)	4421235	*610447674*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	COMP	5	0	
STRESS: BALL SHEAR							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: BOND PULL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4421235	*610446833*	CML-R	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	9	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	500	47	0	
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	1000	47	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	48	193	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	48	951	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	48	1246	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	48	1382	1	Non-Visual
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	500	170	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	500	400	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	500	400	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	80	85	0	
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	168	85	0	
STRESS: INTERNAL VISUAL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	5	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 6.50V, Vcc							
CY7C1470V33 (7C1470A)	4333765	*610349455*	CML-R	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	168	50	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	168	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	168	43	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	128	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	128	47	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	128	44	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/300mA							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	

Reliability Test Data
QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	300	50	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	500	49	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	1000	49	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	300	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	500	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	1000	42	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	300	34	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	500	33	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	1000	33	0	
STRESS: THERMAL SHOCK							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	100	46	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	200	46	0	
STRESS: X-RAY							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	15	0	

Reliability Test Data

QTP #: 071009

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Results
STRESS: CLASS YIELD					
CY7C1370DV33 (7C1370E)	4533948	*VARIOUS*	CML-R	COMP	COMPARABLE
STRESS: SORT YIELD					
CY7C1370DV33 (7C1370E)	4533948	*VARIOUS*	CML-R	COMP	COMPARABLE

Document History Page

Document Title: QTP 033302: 18 MEG SYNCHRONOUS SRAM FAMILY, TECHNOLOGY R9T-3R, FAB4
Document Number: 001-76177

Rev.	ECN No.	Orig. of Change	Description of Change
**	3527621	NSR	Initial spec release. Previous Qual report revision is posted in memo HGA-462. Added CY7C1371DV33 and CY7C1380DV33 devices in the title page.
*A	3631220	NSR	Added Marketing Part Numbers CY7C1384D and CY7C1385D in the title page as per memo GRW-382. Removed Version 8.2 in the title page.
*B	3906564	NSR	Removed obsolete Cypress specs 10-06814, 49-41025, 10-05376, 11-20046 and 001-00293. Removed reference Cypress specs in the reliability tests performed table and replaced with reference industry standard.

Distribution: WEB

Posting: None