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Cypress Semiconductor
Product Qualification Report

QTP# 032003 VERSION *C
August 2014

36 Meg Synchronous SRAM Family Technology R9T-3R, Fab4	
CY7C1440AV25 CY7C1442AV25 CY7C1446AV25	36-Mbit (1M x 36/2M x 18/512K x 72) Pipelined Sync SRAM
CY7C1441AV25 CY7C1443AV25 CY7C1447AV25	36-Mbit (1M x 36/2M x 18/512K x 72) Flow Through SRAM
CY7C1444AV25 CY7C1445AV25	36-Mbit (1M x 36/2M x 18) Pipelined DCD Sync SRAM
CY7C1460AV25 CY7C1462AV25 CY7C1464AV25	36-Mbit (1M x 36/2M x 18/512 x 72) Pipelined SRAM with NoBL™ Architecture
CY7C1461AV25 CY7C1463AV25 CY7C1465AV25	36-Mbit (1M x 36/2M x 18/512 x 72) Flow-Through SRAM with NoBL™ Architecture
CY7C1440AV33 CY7C1442AV33 CY7C1446AV33	36-Mbit (1M x 36/2M x 18/512K x 72) Pipelined Sync SRAM
CY7C1441AV33 CY7C1443AV33 CY7C1447AV33	36-Mbit (1M x 36/2M x 18/512K x 72) Flow Through SRAM
CY7C1444AV33 CY7C1445AV33	36-Mbit (1M x 36/2M x 18) Pipelined DCD Sync SRAM
CY7C1460AV33 CY7C1462AV33 CY7C1464AV33	36-Mbit (1M x 36/2M x 18/512 x 72) Pipelined SRAM with NoBL™ Architecture

CY7C1461AV33 CY7C1463AV33 CY7C1465AV33	**36-Mbit (1M x 36/2M x 18/512 x 72) Flow-Through SRAM with NoBL™ Architecture**
CY7C1460BV25 CY7C1462BV25	**36-Mbit (1M x 36/2M x 18/512 x 72) Pipelined SRAM with NoBL™ Architecture**

FOR ANY QUESTIONS ON THIS REPORT, PLEAE CONTACT
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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
044403	New Device CY7C147*/7C148* AC (72Meg) Device Family, R9T-3R Technology @ Fab4	Nov 04
032003	New Device CY7C144*/7C146* AC, (36Meg) device family, R9T-3R Technology fabricated at Fab4	Nov 04

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product.

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose:	Qualify CY7C144*A/146*A Synchronous product family in qualified technology R9FT-3R, Fab 4
Marketing Part #:	CY7C1440/2/6AV25, CY7C1441/3/7AV25, CY7C1444/5AV25, CY7C1460/2/4AV25, CY7C1461/3/5AV25, CY7C1440/2/6AV33, CY7C1441/3/7AV33, CY7C1444/5AV33, CY7C1460/2/4AV33, CY7C1461/3/5AV33
Device Description:	2.5V, 3.3V, Commercial, Industrial
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION – R9T-3R			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 150Å Ti /3200Å Al / 300Å TiW Metal 2: 150Å Ti /6000 Å Al / 300Å TiW Metal 3: 150Å Ti / 8,000Å Al / 300Å TiW
Passivation Type and Materials:		1000Å Oxide TEOS / 9000Å Nitride	
Generic Process Technology/Design Rule (□-drawn):		CMOS, Triple Metal, 90 nm	
Gate Oxide Material/Thickness (MOS):		Nitridized SiO_2, Thin GOX 22A, Thick GOx	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor -- Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R9T-3R	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
100-Lead TQFP	**CML-R**
165-Ball FBGA	**TAIWAN-G**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	A100
Package Outline, Type, or Name:	100-Lead Thin Quad Flat Pack (TQFP)
Mold Compound Name/Manufacturer:	Hitachi CEL 9200HF9-U (V80)
Mold Compound Flammability Rating:	UL 94-V-0
Oxygen Rating Index:	53%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	Grinding
Die Separation Method:	Step-Cut
Die Attach Supplier:	Dexter
Die Attach Material:	QMI 509
Die Attach Method:	Silver Epoxy
Bond Diagram Designation:	10-06069
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0 mil
Thermal Resistance Theta JA °C/W:	24.63°C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	Cypress Philippines (CML-R)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-R, TAIWAN-G & CHIPMOS (for BGA), KYEC

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max (Core) = 2.2V, 150°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max (Core)=2.25V, 150°C JESD22-A108	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 2.25V, 150°C JESD22-A108	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 2.45V, -30°C JESD22-A108	P
High Accelerated Saturation Test (HAST)	130°C, 3.63V, 85%RH , JEDEC STD 22-A110 Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
Pressure Cooker	121°C, 100%RH, 15 Psig, JESD22-A102 Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
High Temperature Storage	150°C ± 5°C, no bias, JESD22-A103	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114-B	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
Dynamic Latch up	JESD78B	P
Static Latch up	125C, ± 200/300mA JESD78B	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	2,597 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	594,000 DHRs	0	0.7	170	9 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 044403

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	COMP	15	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	15	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	COMP	5	0	
CY7C1470V33 (7C1470A)	4321389	*610354349*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4323794	*610348235*	TAIWN-G	COMP	3	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1470V33 (7C1470A)	4333765	*610349455*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1470V33 (7C1470A)	4333765	*610349455*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PERJEDEC EIA/JESD22-A114B, 2,200V							
CY7C1470V33 (7C1470A)	4333765	*610349455*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V							
CY7C1470V33 (7C1470A)	4423022	*610453316*	TAIWN-G	48	447	0	
CY7C1470V33 (7C1470A)	4425478	*610451858*	TAIWN-G	48	833	0	
CY7C1470V33 (7C1470A)	4425554	*610453022*	TAIWN-G	48	560	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.25V							
CY7C1470V33 (7C1470A)	4423022	*610453316*	TAIWN-G	500	397	0	
CY7C1470V33 (7C1470A)	4425478	*610451858*	TAIWN-G	500	397	0	
CY7C1470V33 (7C1470A)	4425554	610453022	TAIWN-G	500	394	0	

Reliability Test Data

QTP #: 044403

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc MAX							
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	80	85	0	
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	168	85	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.6V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1470V33 (7C1470A)	4321389	*610417278*	TAIWN-G	128	47	0	
CY7C1470V33 (7C1470A)	4414234	*610446423*	TAIWN-G	128	49	0	
CY7C1470V33 (7C1470A)	4414234	*610446424*	TAIWN-G	128	46	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	500	47	0	
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	1000	47	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.45 Vcc							
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1470V33 (7C1470A)	4321389	*610417278*	TAIWN-G	168	43	0	
CY7C1470V33 (7C1470A)	4414234	*610446423*	TAIWN-G	168	50	0	
CY7C1470V33 (7C1470A)	4414234	*610446424*	TAIWN-G	168	51	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7V, +/300mA							
CY7C1470V33 (7C1470A)	4333765	*610349455*	TAIWN-G	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/300mA							
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH, MSL3							
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	300	48	0	
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	500	48	0	
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	1000	48	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	300	50	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	500	50	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	1000	50	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	300	50	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	500	50	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	1000	50	0	

Reliability Test Data

QTP #: 032003

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1460AV33 (7C1460B)	4423933	*610446379*	CML-R	COMP	15	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1460AV33 (7C1460B)	4423933	*610446379*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1460AV33 (7C1460B)	4423933	*610446379*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1460AV33 (7C1460B)	4423933	*610446379*	CML-R	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V							
CY7C1460AV33 (7C1460B)	4429670	*610457634*	CML-R	48	2597	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1460AV33 (7C1460B)	4423933	*610451166*	CML-R	168	44	0	
***STRESS: STATIC LATCH-UP TESTING, 125C, 8.0V,* and +/300mA**							
CY7C1460AV33 (7C1460B)	4423933	*610446379*	CML-R	COMP	3	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1460AV33 (7C1460B)	4423933	*610446379*	CML-R	300	49	0	
CY7C1460AV33 (7C1460B)	4423933	*610446379*	CML-R	500	48	0	
CY7C1460AV33 (7C1460B)	4423933	*610446379*	CML-R	1000	48	0	

History Page

Document Title: QTP 032003: 36 MEG SYNCHRONOUS SRAM FAMILY, TECHNOLOGY R9T-3R, FAB4
Document Number: 001-81773

Rev.	ECN No.	Orig. of Change	Description of Change
**	3701632	NSR	Initial spec release. Changes on the previous qual report revision released in memo LGQ-724. - Updated the QTP# 032003 VERSION 3.0 to VERSION 4.0 - Added the CY7C1460BV25 and CY7C1462BV25 devices in the title page in reference to memo GRW-389. - Updated the product division from MID to MPD. - Removed the obsolete assembly process flow spec 11-21009. - Removed the reference Cypress specs on the Reliability Tests Performed table and replaced with the industry standards. - Removed the reference QTP# 071011 in the history page and in the QTP data.
*A	3802383	NSR	Removed VERSION 4.0 in the title page.
*B	4079974	HSTO	Sunset Review Updated test location facility based on current qualified test site.
*C	4475040	HSTO	Align qualification report based on the new template in the front page

Distribution: WEB

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