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Continuity of ordering part numbers
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Cypress Semiconductor
Product Qualification Report

QTP# 012705 VERSION*A
June, 2014

1MEG SRAM FAST ASYNCHRONOUS FAMILY R52FFD-3 TECHNOLOGY , FAB 4	
CY7C1021BV33	**64K x 16 Static RAM**
CY7C1019BV33	**128K x 8 Static RAM**

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
000505	New 1Meg Asynchronous, CY7C1021BV33, R52FD-3	Oct 00
011205	New Technology Derivative R52FFD-3, Fab 4 / New 1Meg, GB/s Quad Port Switch CY7C04312BV/ CY7C04314BV	Jun 01
012705	Transfer of CY7C1021BV33 from Technology R52FD-3 to R52FFD-3	Apr 02

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product**.**

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6,000Å Al-0.5%Cu/300Å TiW Metal 2: 300Å Ti/8,000Å Al-0.5%Cu/300Å TiW
Passivation Type and Materials:		1,000Å Oxide / 9,000 Å Nitride	
Free Phosphorus contents in top glass layer(%):		0%	
Die Coating(s), if used:		N/A	
Number of Transistors:		25.2 million	
Number of Gates:		8.4 million	
Generic Process Technology/Design Rule (∝-drawn):		CMOS, Double Metal, 0.25 □m	
Gate Oxide Material/Thickness (MOS):		SiO_2 55Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor – Bloomington,	
MN Die Fab Line ID/Wafer Process ID:		Fab4/R52FFD-3	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
44-pin SOJ (extended qual. to 32-pin)	Cypress Philippines (CML-R)
44-pin TSOP II	Cypress Philippines (CML-R)
48-Ball FBGA	Cypress Philippines (CML-R), ASE Taiwan (TAIWAN-G)

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	ZS444
Package Outline, Type, or Name:	44-lead Thin Small Outline Package (TSSOP II)
Mold Compound Name/Manufacturer:	Hitachi CEL 9200
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plate, 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Dexter
Die Attach Material:	QMI 509
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	47°C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	Cypress Philippines (CML-R)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-RA, CHINA-JT
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, 3.8V, 150°C, Vcc Max Dynamic Operating Condition, 3.8V, 125°C, Vcc Max JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, 3.8V, 150°C, Vcc Max Dynamic Operating Condition, 3.8V, 125°C, Vcc Max JESD22-A108	P
High Temperature Steady State Life	Static Operating Condition, 3.8 V,150°C, >Vcc Max JESD22-A108	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 140°C, 85%RH, 3.63V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 220°C Reflow)	P
Pressure Cooker	JESD22-A102, 12°C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 220°C Reflow)	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 220°C Reflow)	P
Low Temperature Operating Life	Dynamic Operating Condition, -30°C, 4.3V, f = 4MHz JESD22-A108	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114	P
Acoustic Microscopy, MSL3	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 220°C Reflow)	P
SEM X-Section	MIL-STD-883, Method 2018.2	P
Static Latch-up Sensitivity	+/-300mA, In accordance with JEDEC 17	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate[5]
High Temperature Operating Life Early Failure Rate	4,192		N/A	N/A	0 PPM
High Temperature Operating Life[1],[2], Long Term Failure Rate	1,210,836 DHRs		0.7	55-170	8 FIT

1 A production burn-in of 12 Hrs at 150C, 4.5V is required for the product.
2 Assuming an ambient temperature of 55C and a junction temperature rise of 15C.
3 Chi-squared 60% estimations used to calculate the failure rate.
4 Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] EFR and LFR Failure Rate based on QTP #012705, QTP #011205

Reliability Test Data

QTP #: 012705

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS:	***HIGH TEMP DYNAMIC OPERTING LIFE - EARLY FAILURE RATE, 150C, 3.8V, VCC MAX***						
CY7C1021BV33-ZSC (7C1321F)	4103583	*610112752*	CSPI-R	48	1500	0	
CY7C1021BV33-ZSC (7C1321F)	4103618	*610113224*	CSPI-R	48	1488	0	
STRESS:	***HIGH TEMP DYNAMIC OPERTING LIFE-LATENT FAILURE RATE, 150C, 3.8V, Vcc Max***						
CY7C1021BV33-ZSC (7C1321F)	4103583	*610112752*	CSPI-R	80	390	0	
CY7C1021BV33-ZSC(7C1321F)	4103583	*610112752*	CSPI-R	500	390	0	
CY7C1021BV33-ZSC (7C1321F)	4103618	*610113224*	CSPI-R	80	398	0	
CY7C1021BV33-ZSC (7C1321F)	4103618	*610113224*	CSPI-R	500	398	0	
STRESS	***ESD-CHARGE DEVICE MODE, 500V***						
CY7C1021BV33-ZSC (7C1321F)	4103583	*610112752*	CSPI-R	COMP	9	0	
STRESS	***ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V***						
CY7C1021BV33-ZSC (7C1321F)	4103583	*610112752*	CSPI-R	COMP	9	0	
STRESS	***STATIC LATCH-UP TESTING, +/-300mA***						
CY7C1021BV33-ZSC (7C1321F)	4103583	*610112752*	CSPI-R	COMP	3	0	

Reliability Test Data

QTP #: 012705

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C0430BV-BGI (7C04301A)	4044731	*610051943*	TAIWN-G	COMP	15	0	
CY7C0430BV-BGI (7C04301A)	4045135	*610101405*	TAIWN-G	COMP	15	0	
CY7C0430BV-BGI (7C04301A)	4047508	*610103357*	TAIWN-G	COMP	15	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 3.8V, Vcc Max							
CY7C0430BV-BGI (7C04301A)	4049157	*610108702*	TAIWN-G	96	700	0	
CY7C0430BV-BGI (7C04301A)	4101120	*610110033*	TAIWN-G	96	504	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 3.8V, Vcc Max							
CY7C0430BV-BGI (7C04301A)	4049157	*610108702*	TAIWN-G	168	410	0	
CY7C0430BV-BGI (7C04301A)	4049157	*610108702*	TAIWN-G	500	409	0	
CY7C0430BV-BGI (7C04301A)	4049157	*610108702*	TAIWN-G	1000	408	0	
CY7C0430BV-BGI (7C04301A)	4101120	*610110033*	TAIWN-G	168	410	0	
CY7C0430BV-BGI (7C04301A)	4101120	*610110033*	TAIWN-G	500	409	0	
CY7C0430BV-BGI (7C04301A)	4101120	*610110033*	TAIWN-G	1000	407	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C0430BV-BGI (7C04301A)	4101120	*610110033*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C0430BV-BGI (7C04301A)	4101120	*610110033*	TAIWN-G	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 10V, +/300mA							
CY7C0430BV-BGI (7C04301A)	4101120	*610110033*	TAIWN-G	COMP	3	0	
STRESS: LOW TEMPERATURE OPERATING LIFE, -30C, 4.3V							
CY7C0430BV-BGI (7C04301A)	4025035	*610044436*	TAIWN-G	500	48	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V), PRE COND 192 HR 30C/60%RH, MSL3							
CY7C0430BV-BGI (7C04301A)	4044731	*610051943*	TAIWN-G	128	46	0	
CY7C0430BV-BGI (7C04301A)	4045135	*610101405*	TAIWN-G	128	57	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C0430BV-BGI (7C04301A)	4044731	*610051943*	TAIWN-G	168	48	0	
CY7C0430BV-BGI (7C04301A)	4045135	*610101405*	TAIWN-G	168	50	0	

Reliability Test Data

QTP #: 011205

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH, MSL3							
CY7C0430BV-BGI (7C04301A)	4044731	*610051943*	TAIWN-G	300	48	0	
CY7C0430BV-BGI (7C04301A)	4044731	*610051943*	TAIWN-G	500	48	0	
CY7C0430BV-BGI (7C04301A)	4044731	*610051943*	TAIWN-G	1000	47	0	
CY7C0430BV-BGI (7C04301A)	4045135	*610101405*	TAIWN-G	300	50	0	
CY7C0430BV-BGI (7C04301A)	4045135	*610101405*	TAIWN-G	500	50	0	
CY7C0430BV-BGI (7C04301A)	4045135	*610101405*	TAIWN-G	1000	50	0	
***STRESS: TC COND. C -65C TO 150C**							
CY7C0430BV-BGI (7C04301A)	4049157	*610108702*	TAIWN-G	300	48	0	
CY7C0430BV-BGI (7C04301A)	4049157	*610108702*	TAIWN-G	500	48	0	
CY7C0430BV-BGI (7C04301A)	4049157	*610108702*	TAIWN-G	1000	47	0	
CY7C0430BV-BGI (7C04301A)	4101120	*610110033*	TAIWN-G	300	48	0	
CY7C0430BV-BGI (7C04301A)	4101120	*610110033*	TAIWN-G	500	48	0	
CY7C0430BV-BGI (7C04301A)	4101120	*610110033*	TAIWN-G	1000	47	0	

***Note: No precondition performed.**

Document History Page

Document Title: QTP # 012705 : 1MEG SRAM FAST ASYNCHRONOUS FAMILY (CY7C1019BV33/CY7C1021BV33) R52FFD-3 TECHNOLOGY , FAB 4
Document Number: 001-88019

Rev.	ECN No.	Orig. of Change	Description of Change
**	4033719	ILZ	Initial Spec Release Qualification report published on Cypress.com is not in spec format. Initiated spec for QTP 012705 and removed all Cypress reference spec and replaced with Industry standard. Updated package availability based on current qualified assembly
*A	4417735	JYF	Sunset review: Updated QTP title page and Reliability Tests Performed table (EFR/LFR, HTSSL, HAST, PCT, TCT, LTOL, ESD-CDM/HBM, Acoustic Microscopy, SEM X-Section, Static Latch-Up) for template alignment.

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