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Cypress Semiconductor
Product Qualification Report

QTP# 004803 VERSION*A
June, 2014

FAST ASYNCHRONOUS STATIC RAM R52D-3 TECHNOLOGY, FAB 4	
CY7C1399B	**32K x 8 STATIC RAM**

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
99311	New Technology R52D-3 /New Product, 2Meg,CY7C1329 SRAM	Aug 99
004803	New Product, Fast Asynchronous SRAM,CY7C1399B	May 01

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product.

PRODUCT DESC IPTION (for ualification)		
Qualification Purpose: To qualify new Fast Asynchronous SRAM, CY7C1399B in Qualified R52D-3 Technology, Fab 4.		
Marketing Part #:	CY7C1399B	
Device Description:	3.3V, Commercial and Industrial available in 28-lead SOJ and 28-lead TSOP Package.	
Cypress Division:	Cypress Semiconductor Corporation – Memory Product Division (MPD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification		Rev.H
What ID markings on Die:	7C1399D	

TECHNOLOGY/FAB PROCESS DESCRIPTION - R52D-3			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6000Å Al-.5%Cu/300Å TiW Metal 2: 300Å CoTi/8000Å Al-.5%Cu/300Å TiW
Passivation Type and Materials:			1KÅ Oxide + 9KÅ Nitride
Die coating(s)			N/A
Generic Process Technology/Design Rule (µ-drawn):			CMOS, Double Metal /0.25 µm/0.3 FETs
Gate Oxide Material/Thickness (MOS):			SiO_2 / 55Å
Name/Location of Die Fab (prime) Facility:			Cypress Semiconductor - Bloomington, MN
Die Fab Line ID/Wafer Process ID:			Fab4/R52D-3

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
28 lead TSOP	**CHINA-JT, TAIWAN-T**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	V2839
Package Outline, Type, or Name:	28-lead Plastic Small Outline J-Bend (SOJ)
Mold Compound Name/Manufacturer:	Hitachi CEL9200IV77
Mold Compound Flammability Rating:	V-O per UL 94
Oxygen Rating Index:	＞28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	90%Sn, 10%Pb, range thickness: 410um-437um
Die Backside Preparation Method/Metallization:	Backgrind Fine Finish/Silicon
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8361H
Wire Bond Method:	Ultrasonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	59.2°C/W
Package Cross Section Yes/No:	Yes
Name/Location of Assembly (prime) facility:	Cypress Philippines (CSPI-R)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	KYEC,TAIWAN
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C Dynamic Operating Condition, Vcc = 4.5V, 150°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C JESD22-A108	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 3.63V, 150°C JESD22-A108	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 140°C, 85%RH, 3.63V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 220°C Reflow)	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 220°C Reflow)	P
Pressure Cooker Test	JESD22-A102, 121°C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 220°C Reflow)	P
High Temp Storage	JESD22-A103:165°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Aged Bond Pull	200°C, 4HRS MIL-STD-883, Method 2011	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260C Reflow)	P
Latch-up Sensitivity	In accordance with JEDEC 17	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate[5]
High Temperature Operating Life Early Failure Rate[1]	11,345	1	N/A	N/A	88 PPM
High Temperature Operating Life[2,3] Long Term Failure Rate	1,794,740DHRs	3	0.7	170	14 FIT

[1] A production burn-in of 12 Hrs at 150C, 4.5V is required for the product.
[2] Assuming an ambient temperature of 55C and a junction temperature rise of 15C.
[3] Chi-squared 60% estimations used to calculate the failure rate.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] EFR Failure Rate based on QTP #004803 and QTP #99311
[4] LFR Failure Rate based on QTP #99311

Reliability Test Data

QTP #: 004803

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY7C1399B-VC (7C1399H)	4051552	*610109433/5/6*	CSPI-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY7C1399B-VC (7C1399H)	4051552	*610109433/5/6*	CSPI-R	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 10V, +/300mA)							
CY7C1399B-VC (7C1399H)	4051552	*610109433/5/6*	CSPI-R	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V, Vcc Max)							
CY7C1399B-VC (7C1399H)	4051552	*610109433/34/35*	CSPI-R	48	3028	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 192 HR 30C/60%RH							
CY7C1399B-VC (7C1399H)	4051552	*610109433/34/35*	CSPI-R	168	50	0	
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH (MSL3)							
CY7C1399B-VC (7C1399H)	4051552	*610109433/34/35*	CSPI-R	300	50	0	

Reliability Test Data

QTP #: 99311

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 4.5V)							
CY7C1329-AC (7C1329D)	CSPI-R	4905886	619909761	48	2988	0	
CY7C1329-AC (7C1329D)	CSPI-R	4905886	619909761	48	1205	0	
CY7C1329-AC (7C1329D)	CSPI-R	4905886	619909776	48	871	0	
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911324	48	1584	1	1 PARTICLE DEFECT
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911327	48	1669	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	1000V	3	0	
CY7C1329-AC (7C1329D)	CSPI-R	4901357	619903817	750V	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	2200V	3	0	
CY7C1329-AC (7C1329D)	CSPI-R	4901357	619903817	2200V	3	0	
STRESS: STATIC LATCH-UP TESTING (125C, 10V, +/-200mA)							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C/85%RH/3.63V), PRECOND. 192 HRS 30C/60%RH							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	128	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	256	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4901357	619903817	128	48	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY7C1329-AC (7C1329D)	CSPI-R	4842121	619815465	336	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4843204	619815797	336	48	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V)							
CY7C1329-AC (7C1329D)	CSPI-R	4842121	619815465	80	80	0	
CY7C1329-AC (7C1329D)	CSPI-R	4842121	619815465	168	80	0	
CY7C1329-AC (7C1329D)	CSPI-R	4843204	619815797	80	80	0	
CY7C1329-AC (7C1329D)	CSPI-R	4843204	619815797	168	80	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V)							
CY7C1329-AC (7C1329D)	CSPI-R	4905886	619909761	80	1196	0	
CY7C1329-AC (7C1329D)	CSPI-R	4905886	619909761	500	799	0	
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911324	80	1491	1	1 UNKNOWN CAUSE
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911324	500	1199	1	1 UNKNOWN CAUSE
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911327	80	1640	0	
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911327	500	1451	1	1 UNKNOWN CAUSE

Reliability Test Data

QTP #: 99311

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	168	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4901357	619903817	168	46	0	
STRESS: STATIC LATCH-UP TESTING (+/-200 mA)							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	9.98V	3	0	
CY7C1329-AC (7C1329D)	CSPI-R	4901357	619903817	9.96V	3	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH (MSL 3)							
CY7C1329-AC (7C1329D)	CSPI-R	4842121	619815465	300	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4842121	619815465	1000	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4843204	619815797	300	45	0	
CY7C1329-AC (7C1329D)	CSPI-R	4843204	619815797	1000	45	0	

Document History Page

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Rev.	ECN No.	Orig. of Change	Description of Change
**	4033719	ILZ	Initial Spec Release Qualification report published on Cypress.com is not in spec format. Initiated spec for QTP 004803 and removed all Cypress reference spec and replaced with Industry standard. Updated package availability based on current qualified assembly
*A	4417735	JYF	Sunset review: Updated QTP title page and Reliability Tests Performed table (EFR/LFR, HTSSL, HAST, TCT, PCT, HTS, ESD-HBM, ESD-CDM, Current Density, Aged Bond Pull, Acoustic Microscopy) for template alignment.

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