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Cypress Semiconductor
Product Qualification Report

QTP# 000301 VERSION *A
July 2014

4 Meg Asynchronous RAM R52D-5R Technology, Fab 4	
CY7C1041B	256K x 16 Static RAM
CY7C1046B	1M x 4 Static RAM
CY7C1049B	512K x 8 Static RAM

FOR ANY QUESTIONS ON THIS REPORT, PLEAE CONTACT
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Product Qualification History

Qual Report	*Description of Qualification Purpose*	Date Comp
000301	New Technology Derivative R52D-5R /New 4Meg, Async SRAM CY7C149B	Apr 00

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: Qualify Technology R52D-5R in Fab4. and Asynchronous SRAM CY7C149B and its product family.			
Marketing Part #:	CY7C1049B		
Device Description:	5V, Commercial available in SOJ and TSOP Package		
Cypress Division:	Cypress Semiconductor Corporation – MPD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. C	
What ID markings on Die:	7C1041A/7C1046A/7C1049A		

TECHNOLOGY/FAB PROCESS DESCRIPTION - R52D-5R			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500 Å TiW/6000 Å Al-.5%Cu/300 Å TiW Metal 2: 300Å CoTi/8000Å Al-.5%Cu/300Å TiW
Passivation Type and Materials:			1000Å of TEOS + 9000Å SiN
Free Phosphorus contents in top glass layer (%):			0%
Number of Transistors in Device:			26 million
Number of Gates in Device:			4.5 million
Generic Process Technology/Design Rule (□-			CMOS, Double Metal /0.25 ∝m
Gate Oxide Material/Thickness (MOS):			55 Å
Name/Location of Die Fab (prime) Facility:			Cypress Semiconductor -- Bloomington, MN
Die Fab Line ID/Wafer Process ID:			Fab4/R52D-5R

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY FACILITY SITE
44-lead TSOP II	**JCET , CML-RA**
44-lead SOJ	**JCET**

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	V3644
Package Outline, Type, or Name:	36-lead Plastic Small Outline J-Bend (SOJ)
Mold Compound Name/Manufacturer:	Hitachi CEL9200
Mold Compound Flammability Rating:	V-O per UL 94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8361H
Bond Diagram Designation	10-03636
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	50.3 °C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	Cypress Philippines (CSPI-R)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	KYEC, CML-RA
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 5.75 V 150C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 5.75 V 150C	P
High Accelerated Saturation Test (HAST)	130C, 5.5V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220C+5, -0C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65C to 150C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220C+5, -0C	P
Pressure Cooker Test	No bias, 121C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220C+5, -0C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD- CDM)	500V , JESD22-C101C	P
High Temperature Storage	150C+/-5C no bias	P
C-SAM	MIL-STD 883 Method 2018-2	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Low Temperature Operating Life	-30C, 6.5V, 8 MHZ	P
Age Bond	200C,4hrs MIL-STD-883, Method 883-2011	P
High Temp. Steady State Life Test	Static Operating Condition, Vcc = 5.5 V 150C	P
Acoustic Microscopy, MSL3	J-STD-020	P
Latchup Sensitivity	12C, 11,5V, ±300mA In accordance with JEDEC 17.	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Failure Rate[4]
High Temperature Operating Life Early Failure Rate1	3000	1	N/A	N/A	333 PPM
High Temperature Operating Life2,3 Long Term Failure Rate	792,900 DHRs	0	0.7	170	7 FIT

1 A production burn-in of 24 Hrs at 150C, 7.0V is required for the product.
2 Assuming an ambient temperature of 55C and a junction temperature rise of 15C.
3 Chi-squared 60% estimations used to calculate the failure rate.
4 Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 000301

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
CY7C1049B-VC (7C1549C)	4944781	*610003706*	CSPI-R	48	1000	1	1-Particle
CY7C1049B-VC (7C1549C)	4946002	*610004242*	CSPI-R	48	1000	0	
CY7C1049B-VC (7C1549C)	4941240	*619938804*	CSPI-R	48	1000	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C1049B-VC (7C1549C)	4944781	*610003706*	CSPI-R	80	530	0	
CY7C1049B-VC (7C1549C)	4944781	*610003706*	CSPI-R	500	529	0	
CY7C1049B-VC (7C1549C)	4946002	*610004242*	CSPI-R	80	530	0	
CY7C1049B-VC (7C1549C)	4946002	*610004242*	CSPI-R	500	529	0	
CY7C1049B-VC (7C1549C)	4941240	*619938804*	CSPI-R	80	530	0	
CY7C1049B-VC (7C1549C)	4941240	*619938804*	CSPI-R	500	527	0	
STRESS: ESD-CHARGE DEVICE MODEL (1,000V)							
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	1000V	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (4,400V)							
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	4400V	3	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 5.5V), PRE COND 192 HR 30C/60%RH							
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	128	47	0	
CY7C1049B-VC (7C1549C)	4944781	*610003706*	CSPI-R	128	49	0	
STRESS: HIGH TEMPERATURE STORAGE, (150C)							
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	336	48	0	
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	500	48	0	
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	1000	48	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.5V, Vcc MAX)							
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	80	80	0	
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	168	80	0	

Reliability Test Data

QTP #:000301

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: LOW TEMPERATURE OPERATING LIFE (-30C, 6.50V)							
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	500	46	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 192 HR 30C/60%RH							
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	168	48	0	
CY7C1049B-VC (7C1549C)	4920692	*619933105*	CSPI-R	168	47	0	
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH (MSL3)							
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	300	48	0	
CY7C1049B-VC (7C1549C)	4919497	*619925326*	CSPI-R	500	48	0	
CY7C1049B-VC (7C1549C)	4920692	*619933105*	CSPI-R	300	47	0	

Document History Page

Document Title: QTP#000301:4 Meg Asynchronous RAM "CY7C1041B/46B/49B" R52D-5R Technology, Fab 4
Document Number: 001-88063

Rev.	ECN No.	Orig. of Change	Description of Change
**	4037517	HSTO	Initial Spec Release Qualification report published on Cypress.com was transferred to qualification report spec template. Deleted Cypress obsolete referenced spec in Major package qualification details. Updated package availability based on current qualified test & assembly site. Deleted Cypress reference Spec and replaced with Industry Standards in Reliability Test Performed Table.
*A	4431902	HSTO	Align qualification report based on the new template in the front page

Distribution: WEB

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