Cypress Semiconductor
Qualification Report

QTP# 98357 VERSION 1.1
May, 1999

4 Meg SRAM With NoBL™ Architecture R42D Technology, Hot Aluminum	
CY7C1350	128K x 36 Pipelined SRAM
CY7C1351	128K x 36 Flow-Through SRAM
CT7C1352	256K x 18 Pipelined SRAM
CY7C1353	256K x 18 Flow-Through SRAM

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CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Ed Russell
Reliability Director
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PRODUCT DESCRIPTION (for qualification)		
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied: qualify 4 Meg SRAM with NoBL Architecture in R42D technology with Hot Al.		
Marketing Part #:	CY7C1350/CY7C1352	
Package:	100 pins TQFP	
Device Description:	1 Meg SRAM with NoBL Architecture, R42D Technology with Hot Al	
Cypress Division:	Cypress Semiconductor Corporation	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A
What ID markings on Die:	7C1350A/7C1352A	

TECHNOLOGY/FAB PROCESS DESCRIPTION - R42D			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6000Å Al -5%Cu/1200Å TiW Metal 2: 500Å TiW/8000Å Al -5%Cu/300Å TiW
Passivation Type and Materials:		7000Å SiO_2 + 6000Å Si_3N_4	
Free Phosphorus contents in top glass layer(%):		0%	
Die Coating(s), if used:	N/A		
Generic Process Technology/Design Rule (µ-drawn):		CMOS, Double Metal /0.35 µm	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 70Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor - Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R42D (with Hot AL)	

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	100-pins TQFP		
Mold Compound Name/Manufacturer:	Hitachi-9200		
Lead Frame material:	Copper Alloy 194		
Lead Finish, composition:	Solder Plated, 90%Sn, 10%Pb		
Die Attach Area Plating:	None		
Die Attach Method:	Silver Epoxy	Die Attach Material:	Ablestik 8361H
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.3 mil
JESD22-A112 Moisture Sensitivity Level:	Level 3		
Name/Location of Assembly (prime) facility:	Cypress Philippines (CSPI-R)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.8 V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, 85%RH, 3.63V Precondition: JESD22 Moisture Sensitivity MSL 3 (192 Hrs, 30C/60%RH)	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 (192 Hrs, 30C/60%RH)	P
Latchup Sensitivity	In accordance with JEDEC 17. Cypress Spec. 01-00081	9.9V ±200mA
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	4,400V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	500V
Pressure Cooker Test	No bias, 121°C, 100%RH	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate[5]
High Temperature Operating Life Early Failure Rate[1]	1500	0	N/A	N/A	0 PPM
High Temperature Operating Life[2,3] Long Term Failure Rate	412,168 DHRs	1	0.7	170	29 FIT

[1] A production burn-in of 53 Hrs at 150°C, 4.3V is required for the product.
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

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DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V)							
CY7C1350-AC	CSPI-R	4812418	619805770	48	750	0	
CY7C1350-AC		4815594	619807192	48	288	0	
CY7C1350-AC		4815594	619807192	48	396	0	
CY7C1352-AC	CSPI-R	4824383	619809153	48	66	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY7C1352-AC	CSPI-R	4824383	619809153	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (4,400V)							
CY7C1352-AC	CSPI-R	4824383	619809153	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 3.63V), PRECOND. 192 HRS 30C/60%RH							
CY7C1350-AC	CSPI-R	4816713	619808643	128	48	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V)							
CY7C1350-AC	CSPI-R	4812418	619805770	80	392	1	1 EOS, 1 UNKNOWN CAUSE
CY7C1350-AC	CSPI-R	4812418	619805770	500	390	0	
CY7C1350-AC	CSPI-R	4815594	619807192	80	396	0	
CY7C1350-AC	CSPI-R	4815594	619807192	548	396	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C1352-AC	CSPI-R	4816713	619808642	168	45	0	
CY7C1352-AC	CSPI-R	4816713	619808642	288	45	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH (MSL 3)							
CY7C1350-AC	CSPI-R	4812418	619805769	300	45	0	
CY7C1350-AC	CSPI-R	4812418	619805770	300	45	0	
CY7C1350-AC	CSPI-R	4815594	619807192	300	45	0	