Cypress Semiconductor
Technology Derivative Qualification Report

QTP# 014807 VERSION 2.0
June 2005

Technology Derivative R7FT-3R, Fab4 Synchronous Dual-Port RAM CY7C085xV / CY7C083xV	
CY7C0851V	**64K x 36**
CY7C0831V	**128K x 18**
CY7C0852V	**128K x 36**
CY7C0832V	**256K x 18**
CY7C0853V	**256K x 36**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
014807	New Technology Derivative R7FT-3R (Hot Al) / Synchronous Dual-Port RAM CY7C0852V, product family and package option.	Feb 02

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify new Technology Derivative R7FT-3R, Fab 4, CY7C0852V and its product family.		
Marketing Part #:	CY7C10831V, CY7C0832, CY7C0851V, CY7C0852V, CY7C0853V	
Device Description:	Synchronous Dual Port RAM, 3.3V, Commercial and Industrial available in 120/176-lead TQFP and 172-ball BGA package.	
Cypress Division:	Cypress Semiconductor Corporation –Data Com Division (DCD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A
What ID markings on Die:	7C08523VA	

TECHNOLOGY/FAB PROCESS DESCRIPTION – R7FT-3R			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 150Å Ti / 4,200Å Al / 300Å TiW Metal 2: 150Å Ti /4,200 Å Al / 300Å TiW Metal 3: 150Å Ti / 8,000Å Al / 300Å TiW
Passivation Type and Materials:		1000Å TEOS / 9000Å PECVD Nitride	
Free Phosphorus contents in top glass layer(%):		0%	
Number of Transistors in Device		62 million	
Number of Gates in Device		112K	
Generic Process Technology/Design Rule (□-drawn):		CMOS, Triple Metal /0.18 um	
Gate Oxide Material/Thickness (MOS):		SiO_2, 32Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor -- Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		RAM7FT-3R	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
172-ball BGA	**ASE Taiwan**
120/176-lead TQFP	**ASE Taiwan**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB172
Package Outline, Type, or Name:	172-ball, Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	PLASKON SMT-B-1
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	Solder Ball, 63%Sn, 37%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8355F
Die Attach Method:	Silver Epoxy
Bond Diagram Designation:	10-04267
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	17°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41020
Name/Location of Assembly (prime) facility:	ASE Taiwan

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	ASE Taiwan (TAIWN-G), CML-R
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	A176
Package Outline, Type, or Name:	176-pin Thin Quad Flat Pack (TQFP)
Mold Compound Name/Manufacturer:	Sumitomo EME 7320A
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plate, 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8361H
Bond Diagram Designation	10-04107
Wire Bond Method:	Thermosonic
Wire Material/Size:	Gold/ 1.2mil
Thermal Resistance Theta JA °C/W:	36°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41004
Name/Location of Assembly (prime) facility:	ASE Taiwan (TAIWN-G)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	ASE Taiwan (TAIWN-G), CML-R
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.3V, , 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 2.3V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max = 3.63V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, 3.63V,85%RH Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C	P
Pressure Cooker	121°C, 100%RH Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C	P
High Temperature Storage	150°C ± 5°C no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1,100V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Age Bond Strength	200C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy, Level 3	Cypress Spec. 25-00104	P
Current Density	Cypress Spec 22-00029	P
Dynamic Latchup	In accordance with JEDEC 17. Cypress Spec. 01-00081	P
Static Latchup	125C, 10V, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate[1]	1,227	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	445,840 DHRs	0	0.7	170	12 FIT

[1] A production burn-in of 30 Hrs at 125°C, 2.7V is required for the product.
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate..
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 014807

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C0852V-BC(7C08523A)	4130707	*610133760L1*	ASE-TAIWN	COMP	15	0	
CY7C0852V-BC(7C08523A)	4131840	*610135256*	ASE-TAIWN	COMP	15	0	
CY7C0852V-BC(7C08523A)	4131841	*610137123L1*	ASE-TAIWN	COMP	15	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.3V, Vcc Max							
CY7C0852V-BC(7C08523A)	4131841	*610137123L1*	ASE-TAIWN	48	772	0	
CY7C0852V-BC(7C08523A)	4141878	*610145152*	ASE-TAIWN	96	455	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.3V, Vcc Max							
CY7C0852V-BC(7C08523A)	4131840	*610135256*	ASE-TAIWN	80	300	0	
CY7C0852V-BC(7C08523A)	4131840	*610135256*	ASE-TAIWN	500	274	0	
CY7C0852V-BC(7C08523A)	4131841	*610137123L1*	ASE-TAIWN	80	400	0	
CY7C0852V-BC(7C08523A)	4131841	*610137123L1*	ASE-TAIWN	500	193	0	
CY7C0852V-BC(7C08523A)	4133371	*610137695*	ASE-TAIWN	80	400	0	
CY7C0852V-BC(7C08523A)	4133371	*610137695*	ASE-TAIWN	500	385	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 1,100V							
CY7C0852V-BC(7C08523A)	4133371	*610137695*	ASE-TAIWN	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C0852V-BC(7C08523A)	4133371	*610137695*	ASE-TAIWN	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 10V, +/300mA							
CY7C0852V-BC(7C08523A)	4130707	*610133760L1*	ASE-TAIWN	COMP	3	0	
CY7C0852V-BC(7C08523A)	4131840	*610135256*	ASE-TAIWN	COMP	3	0	
STRESS: AGE BOND STRENGTH							
CY7C0852V-BC(7C08523A)	4130707	*610133760L1*	ASE-TAIWN	COMP	5	0	
CY7C0852V-BC(7C08523A)	4131840	*610135256*	ASE-TAIWN	COMP	6	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C0852V-BC(7C08523A)	4128335	*610130788*	ASE-TAIWN	500	48	0	
CY7C0852V-BC(7C08523A)	4128335	*610130788*	ASE-TAIWN	1000	48	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 3.63V, Vcc MAX							
CY7C0852V-BC(7C08523A)	4130707	*610133760L1*	ASE-TAIWN	80	78	0	
CY7C0852V-BC(7C08523A)	4130707	*610133760L1*	ASE-TAIWN	168	76	0	

Reliability Test Data

QTP #: 014807

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRESSURE COOKER TEST, 121C, 100%RH,, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C0852V-BC(7C08523A)	4131840	*610135256*	ASE-TAIWN	168	47	0	
CY7C0852V-BC(7C08523A)	4131841	*610137123L1*	ASE-TAIWN	168	48	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C0852V-BC(7C08523A)	4131840	*610135256*	ASE-TAIWN	128	48	0	
CY7C0852V-BC(7C08523A)	4131841	*610137123L1*	ASE-TAIWN	128	46	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C0852V-BC(7C08523A)	4130707	*610133760L1*	ASE-TAIWN	300	47	0	
CY7C0852V-BC(7C08523A)	4130707	*610133760L1*	ASE-TAIWN	500	46	0	
CY7C0852V-BC(7C08523A)	4130707	*610133760L1*	ASE-TAIWN	1000	45	0	
CY7C0852V-BC(7C08523A)	4131841	*610137123L1*	ASE-TAIWN	300	46	0	
CY7C0852V-BC(7C08523A)	4131841	*610137123L1*	ASE-TAIWN	500	45	0	