Cypress Semiconductor
Technology Qualification Report

QTP# 001004 VERSION 1.0
January, 2001

0.5um TLM Technology, Fab HME **Dual Port SRAM with PCI Bus Controller**	
CY7C09449PV-AC	**128K, 50MHz**

PCI-DP™ family is trademark of Cypress Semiconductor

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
001004	New 0.5um TLM Technology/New CY7C09449PV-AC Product Qualification	Aug 00

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: To qualify 0.5umTLM Technology,.Fab HME and CY7C09449PV-AC Product.		
Marketing Part #:	CY7C09449PV-AC	
Device Description:	3.3V, PCI-DP™ Dual Port SRAM, Commercial available in 160-pin TQFP Package.	
Cypress Division:	Cypress Semiconductor Corporation – Interface Product Division (IPD)	
Overall Die (or Mask) REV:		Rev. B
What ID markings on Die:	GVS791K1	

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	3	Metal Composition:	Metal 1: (Ti/TiN)/Ti/Al-1%Si-0.5%Cu/Ti/TiN Metal 2: (Ti/TiN)/Ti/Al-1%Si-0.5%Cu/Ti/TiN Metal 3: (Ti/TiN)/Ti/Al-1%Si-0.5%Cu/TiN
Passivation Type and Materials:		Silicon Nitride	
Free Phosphorus contents in top glass layer (%)		Zero	
Generic Process Technology/Design Rule (µ-drawn):		CMOS / 0.5 micron	
Gate Oxide Material/Thickness (MOS):		SiO2 / 95 A	
Name/Location of Die Fab (prime) Facility:		Hyundai / Cheong Ju, Korea	
Die Fab Line ID/Wafer Process ID:		CF4 / HL50 (Hyundai)	

PACKAGE AVAILABILITY

PACKAGE TYPE	ASSEMBLY SITE FACILITY
160-pin TQFP	**Seoul Korea (SEOL-L)**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Outline, Type, or Name:	160-pin Thin Plastic Quad Flatpack (TQFP)
Mold Compound Name/Manufacturer:	Sumitomo 7320CR
Mold Compound Flammability Rating:	V-O per UL 94
Oxygen Rating Index:	>28%
Lead Frame Material:	EFTEC 64T
Lead Finish, Composition / Thickness:	Solder Plate, 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	84-1
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.2um
Thermal Resistance Theta JA °C/W:	39.9°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	Hyundai-turn-key
Name/Location of Assembly (prime) facility:	Seoul Korea (SEOL-L)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Seoul Korea (SEOL-L)
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 135°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 135°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity, MSL3 192 Hrs., 30°C/60%RH+3IR-Reflow, 220°C+5, -0°C	P
Pressure Cooker Test	No bias, 121°C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL3 192 Hrs., 30°C/60%RH+3IR-Reflow, 220°C+5, -0°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7 2,200V	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020 500V	P
Latchup Sensitivity	125C, 10V, ±300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate	1,824	1	N/A	N/A	548 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate	113,008 DHRs	0	0.7	88	92 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 001004

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERTING LIFE - EARLY FAILURE RATE, 135C, 3.8V, VCC MAX							
CY7C09449PV-AC		*800001208*	SEOL-L	96	140	0	
CY7C09449PV-AC		*800001208/2791*	SEOL-L	96	488	0	
CY7C09449PV-AC		*800002104*	SEOL-L	96	1196	1	* *UNKNOWN, NOT VISUAL*
STRESS: HIGH TEMP DYNAMIC OPERTING LIFE-LATENT FAILURE RATE, 135C, 3.8V, Vcc Max							
CY7C09449PV-AC		*800002104*	SEOL-L	168	118	0	
CY7C09449PV-AC		*800002104*	SEOL-L	1000	112	0	
STRESS: ESD-CHARGE DEVICE MODEL, 750V							
CY7C09449PV-AC		*800002104*	SEOL-L	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C09449PV-AC		*800002104*	SEOL-L	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 10V, +/-300mA							
CY7C09449PV-AC		*800002104*	SEOL-L	COMP	3	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH), PRE COND 192HRS 30C/60%RH, MSL3							
CY7C09449PV-AC		*800002104*	SEOL-L	168	47	0	
STRESS: TC CONDITION C, -65C TO 150C, PRE COND. 192 HRS 30C/60% RH, MSL3							
CY7C09449PV-AC		*800002104*	SEOL-L	300	48	0	
CY7C09449PV-AC		*800002104*	SEOL-L	500	47	0	
CY7C09449PV-AC		*800002104*	SEOL-L	1000	45	0	

****A CAR #20001905 was issued to HME**