# Product Roadmap: Timing Solutions

Q1 2024

public

# Timing solutions

## Programmable | High-performance | EMI reduction | Automotive

| | Clock synthesizers | Oscillators | Clock buffers |
|---|---|---|---|
| **High Performance** | **CY27410**<br>4-PLL; Max Freq: 700 MHz<br>12 Outputs; Diff[1] & SE[1]; PCIe 3.0<br>VCXO[2]; EMI[3]; 0.7-ps RMS Jitter[4]<br>1.8 V/2.5 V/3.3 V; Ind[5]; 48-QFN<br><br>**CY27430**<br>4-PLL; Max Freq: 700 MHz<br>8 Outputs; Diff & SE; PCIe 3.0<br>VCXO; EMI; 0.7-ps RMS Jitter<br>1.8 V/2.5 V/3.3 V; Auto A[6] S[7]; 48-QFN<br><br>**CY29430**<br>1-PLL; Max Freq: 2.1 GHz<br>1 Output; Diff & SE; 40/100 GbE<br>VCXO; 0.11-ps RMS Jitter; Ind<br>16-QFN | **CY51x7**<br>1-PLL; Max Freq: 2.1 GHz<br>1 Output; Diff & SE; 40/100 GbE<br>VCXO; 0.11-ps RMS Jitter; Ind<br>1.8 V/2.5 V/3.3 V; WAFER/DIE | |
| **Standard Performance** | **CY254x/CY251x**<br>1–4 PLL; Max Freq: 200 MHz<br>3–9 Outputs; I²C; EMI; Low Power[9]<br>100-ps CCJ[10]; Ind; 1.8/2.5/3.0/3.3 V<br>8-SOIC; 8/16/20-TSSOP; 24-QFN<br><br>**CY229x/CY22381x**<br>3–4 PLL; Max Freq: 166 MHz<br>3–8 Outputs; CMOS; Low Power<br>200-ps PPJ[11]; VCXO; Ind; 3.3/5 V<br>8/16/20-SOIC; 16-TSSOP<br><br>**CY2239x**<br>3–4 PLL; Max Freq: 400 MHz<br>5–8 Outputs; LVPECL, CMOS; I²C<br>400-ps PPJ; VCXO; 3.3 V<br>Ind; 16-TSSOP; 32-QFN<br><br>**CY22800/801**<br>1-PLL; Max Freq: 200 MHz<br>1-3 Outputs; CMOS; EMI<br>110-ps CCJ; VCXO; Ind<br>3.3 V; 8-SOIC; 8-TSSOP<br><br>**CY22050/150**<br>1-PLL; Max Freq: 200 MHz<br>6 Outputs; CMOS; I²C<br>250-ps PPJ; Ind[5]<br>2.5/3.3 V; 16-TSSOP | **CY2037/ 5037**<br>1-PLL; Max Freq: 133 MHz<br>1 Output; CMOS<br>100-ps CCJ; Ind<br>3.3/5.0 V; WAFER<br><br>**CY5057**<br>1-PLL; Max Freq: 170 MHz<br>1 Output; CMOS; EMI<br><200-ps CCJ; Ind<br>3.3/5.0 V; WAFER | **CY230x/EP0x (Zero Delay)**<br>Max Freq: 220 MHz<br>2–9 Outputs; LVCMOS ; 2.5/3.3/5 V<br>22-ps CCJ; Ind[5]; Auto A<br>8/16-SOIC; 16-TSSOP; WAFER<br><br>**CY230xNZ/ 2994x (Non-Zero Delay)**<br>Max Freq: 200 MHz<br>4–18 Outputs; LVCMOS<br>100-ps Op-Op Skew; Ind<br>2.5/3.3 V; 8-TSSOP, 16-SOIC<br><br>**CY23S05 (Zero Delay)**<br>Max Freq: 133 MHz<br>5 Outputs; LVCMOS<br>Spread Aware; 200-ps CCJ; Ind<br>3.3 V; 8,16-SOIC<br><br>**CY23S09 (Zero Delay)** Q424<br>Max Freq: 133 MHz<br>9 Outputs; LVCMOS<br>Spread Aware; 200-ps CCJ; Ind<br>3.3 V; 8,16-SOIC; 16-TSSOP |

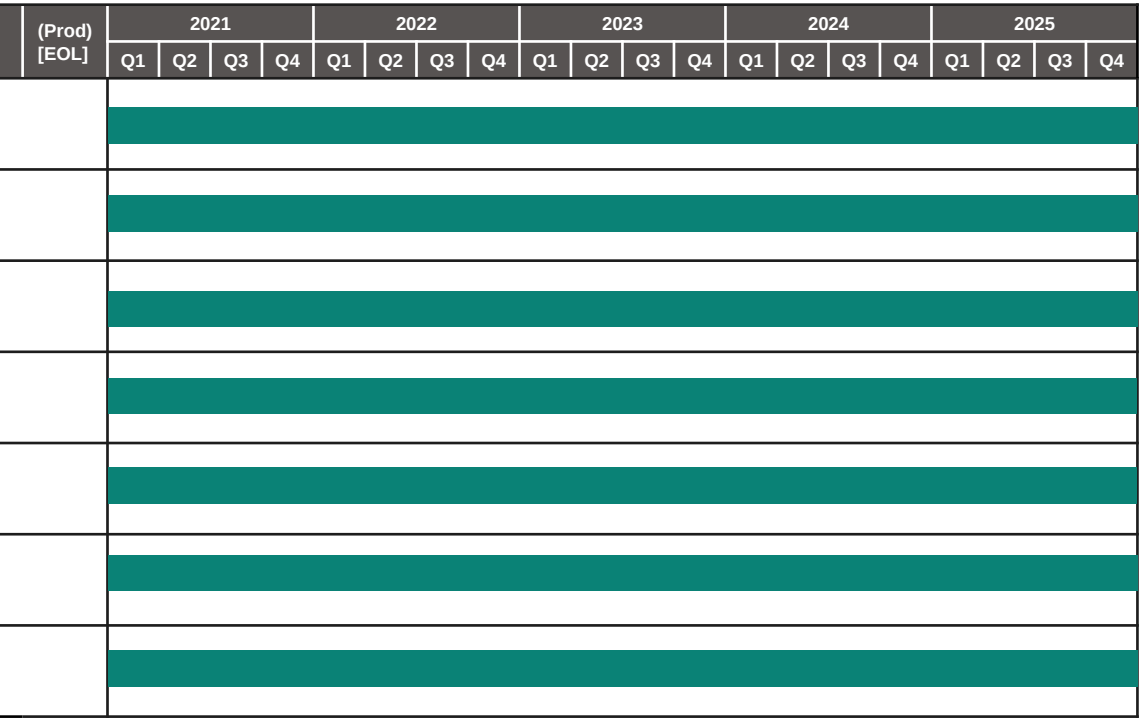
[1] Differential and single-ended outputs
[2] Voltage Controlled Crystal Oscillation
[3] Electromagnetic interference reduction using Lexmark profile
[4] Integrated phase noise across 12-kHz to 20-MHz offset
[5] Industrial grade: -40 °C to +85 °C
[6] AEC-Q100: -40 °C to +85 °C
[7] AEC-Q100: -40 °C to +105 °C
[8] Additive RMS phase jitter
[9] Power Management options
[10] Cycle-to-cycle jitter
[11] Peak-to-peak period jitter
[12] AEC-Q100: -40 °C to +125 °C

| | Concept | Development | Samples | Production |
|---|---|---|---|---|
| Status | | | | |
| Availability | | | QQYY | QQYY |
| EOL (Last Time Ship) | | | | QQYY |
| Automotive | | | | |


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# Clock synthesizer roadmap

| | Product Family | Features | (Prod) [EOL] |
|---|---|---|---|
| High Performance | CY27430 | 4-PLL; Maximum frequency: 700 MHz<br>12 outputs; Diff[1] & SE[1]; PCIe 3.0;<br>VCXO[2]; EMI[3]; 0.7-ps RMS Jitter[4]<br>1.8 V/2.5 V/3.3 V; Ind[5]; 48-QFN | |
| | CY27410 | 4-PLL; Maximum frequency: 700 MHz<br>8 outputs; Diff & SE; PCIe 3.0;<br>VCXO; EMI; 0.7-ps RMS Jitter<br>1.8 V/2.5 V/3.3 V; Auto A[6] S[7]; 48-QFN | |
| | CY254x/CY251x | 1-4 PLL; Maximum frequency: 200 MHz<br>3-9 outputs; I²C; EMI; Low Power[8]<br>100-ps CCJ[9]; Ind; 1.8 V/2.5 V/3.0 V/3.3 V<br>8-SOIC; 8/16/20-TSSOP; 24-QFN | |
| Standard Performance | CY229x/CY22381x | 3-4 PLL; Maximum frequency: 166 MHz<br>3-8 outputs; CMOS; Low power<br>200-ps PPJ[10]; VCXO; Ind; 3.3 V/5 V<br>8/16/20-SOIC; 16-TSSOP | |
| | CY2239x | 3-4 PLL; Maximum frequency: 400 MHz<br>5-8 outputs; LVPECL, CMOS; I²C<br>400-ps PPJ; VCXO; 3.3 V<br>Ind; 16-TSSOP; 32-QFN | |
| | CY22800/801 | 1-PLL; Maximum frequency: 200 MHz<br>1-3 outputs; CMOS; EMI<br>110-ps CCJ; VCXO; Ind;<br>3.3 V; 8-SOIC; 8-TSSOP | |
| | CY22050/150 | 1-PLL; Maximum frequency: 200 MHz<br>6 outputs; CMOS; I²C<br>250-ps PPJ; Ind<br>2.5 V/3.3 V; 16-TSSOP | |




[1] Differential and single-ended outputs
[2] Voltage-controlled crystal oscillation
[3] Electromagnetic interference reduction using Lexmark profile
[4] Integrated phase noise across 12-kHz to 20-MHz offset
[5] Industrial grade: -40 °C to +85 °C
[6] AEC-Q100: -40 °C to +85 °C
[7] AEC-Q100: -40 °C to +105 °C
[8] Power management options
[9] Cycle-to-cycle Jitter
[10] Peak-to-peak period Jitter
[11] AEC-Q100: -40 °C to +125 °C

Concept | Samples | Production | EOL - LOD | EOL - LDD


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# Oscillator roadmap

| | Product Family | Features | (Prod) [EOL] | 2021 Q1 | 2021 Q2 | 2021 Q3 | 2021 Q4 | 2022 Q1 | 2022 Q2 | 2022 Q3 | 2022 Q4 | 2023 Q1 | 2023 Q2 | 2023 Q3 | 2023 Q4 | 2024 Q1 | 2024 Q2 | 2024 Q3 | 2024 Q4 | 2025 Q1 | 2025 Q2 | 2025 Q3 | 2025 Q4 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| High Performance | CY294x | 1-PLL; Maximum frequency: 2.1 GHz<br>1 output; Diff[1] & SE[1]; 40/100 GbE;<br>VCXO[2]; 0.11-ps RMS Jitter[3]; Ind[4];<br>16-QFN | | | | | | | | | | | | | | | | | | | | | |
| | CY51x7 | 1-PLL; Maximum frequency: 2.1 GHz<br>1 output; Diff & SE; 40/100 GbE;<br>VCXO; 0.11-ps RMS Jitter; Ind;<br>1.8 V/2.5 V/3.3 V; WAFER/DIE | | | | | | | | | | | | | | | | | | | | | |
| Standard Performance | CY2037 / 5037 | 1-PLL; Maximum frequency: 133 MHz<br>1 output; CMOS; 100-ps CCJ; Ind;<br>3.3 V/5.0 V; WAFER | | | | | | | | | | | | | | | | | | | | | |
| | CY5057 | 1-PLL; Maximum frequency: 170 MHz<br>1 output; CMOS; EMI; <200-ps CCJ;<br>Ind; 3.3 V/5.0 V; WAFER | | | | | | | | | | | | | | | | | | | | | |

[1] Differential and single-ended outputs
[2] Voltage-controlled crystal oscillation
[3] Integrated phase noise across 12-kHz to 20-MHz offset
[4] Industrial grade: -40 °C to +85 °C
[5] Electromagnetic interference reduction using Lexmark profile
[6] Cycle-to-cycle Jitter

Concept
Samples
Production
EOL - LOD
EOL - LDD


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# Clock buffer roadmap

| Product Family | Features | (Prod) [EOL] | 2021 Q1 | 2021 Q2 | 2021 Q3 | 2021 Q4 | 2022 Q1 | 2022 Q2 | 2022 Q3 | 2022 Q4 | 2023 Q1 | 2023 Q2 | 2023 Q3 | 2023 Q4 | 2024 Q1 | 2024 Q2 | 2024 Q3 | 2024 Q4 | 2025 Q1 | 2025 Q2 | 2025 Q3 | 2025 Q4 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CY230x/EP0x (Zero Delay)** | Maximum frequency: 220 MHz<br>2–9 outputs; LVCMOS; 2.5 V/3.3 V/5 V<br>22-ps CCJ[3]; Ind; Auto A[4]<br>8/16-SOIC; 16-TSSOP; WAFER | | | | | | | | | | | | | | | | | | | | | |
| **CY230xNZ (Non-Zero Delay)** | Maximum frequency: 200 MHz<br>4–18 outputs; LVCMOS<br>100-ps Op-Op Skew; Ind<br>2.5 V/3.3 V; 8-TSSOP, 16-SOIC | | | | | | | | | | | | | | | | | | | | | |
| **CY23S05 (Zero Delay)** | Maximum frequency: 133 MHz<br>9 outputs; LVCMOS<br>Spread Aware; 200-ps CCJ; Ind;<br>3.3 V; 8/16-SOIC | | | | | | | | | | | | | | | | | | | | | |
| **CY23S09 (Zero Delay)** | Maximum frequency: 133 MHz<br>9 outputs; LVCMOS<br>Spread Aware; 200-ps CCJ; Ind;<br>3.3 V; 8/16-SOIC; 16-TSSOP | | | | | | | | | | | | | | | | | | | | | |

Concept
Samples
Production
EOL - LOD
EOL - LDD

[1] Additive RMS Phase Jitter
[2] Industrial grade: -40 °C to +85 °C
[3] Cycle-to-cycle Jitter
[4] AEC-Q100: -40 °C to +85 °C


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# CY27410: High-performance 4-PLL clock generator

## Applications

Multifunction printers, digital TVs, Blu-ray recorders, home gateways, femtocells, routers, and switches

## Features

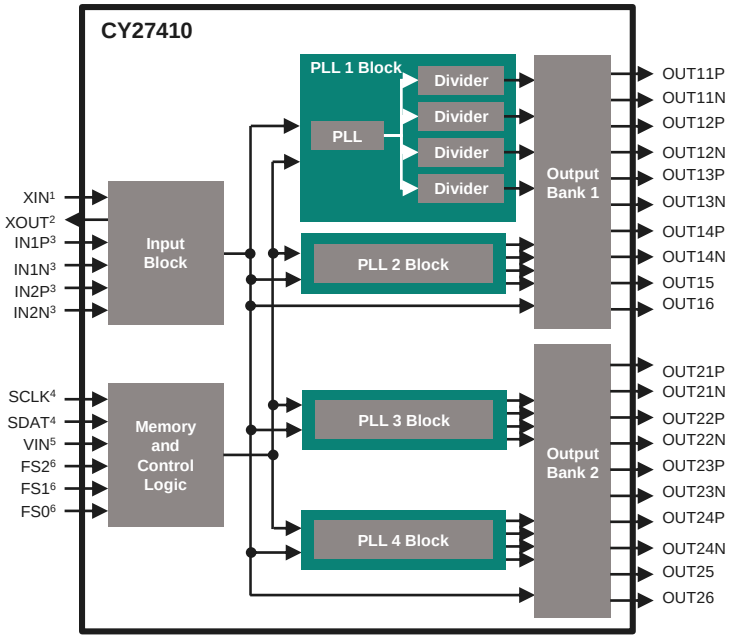
- **Twelve outputs**
  - Eight configurable (differential or single-ended)
  - Four single-ended
- **Specifications**
  - High frequency: 700-MHz differential, 250-MHz single-ended
  - RMS phase jitter <0.7 ps (typical)
  - Reference clock support for PCIe 3.0, SATA 2.0, and 10 GbE
  - Industrial temperature grade
- **Additional features**
  - Pin select and I²C programming
  - Configurable as zero or non-zero delay buffer
  - Glitch-free frequency switching
  - Frequency select option to choose from eight preprogrammed configurations
  - Early/late clocks
  - PLL cascading
  - Voltage-controlled frequency synthesis (VCFS)
- **RoHS-compliant package**
  - Available in a 7 mm x 7 mm 48-pin QFN package

## Collateral

**Datasheet**: 4-PLL High-Performance Clock Generator (CY27410)

[1] Crystal input
[2] Crystal output
[3] Reference clock inputs
[4] Serial port
[5] Voltage input pin for VCFS
[6] Frequency select inputs

## Four-PLL Spread-Spectrum clock generator




## Availability

**Production**: Now


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# CY27430: High-performance 4-PLL clock generator

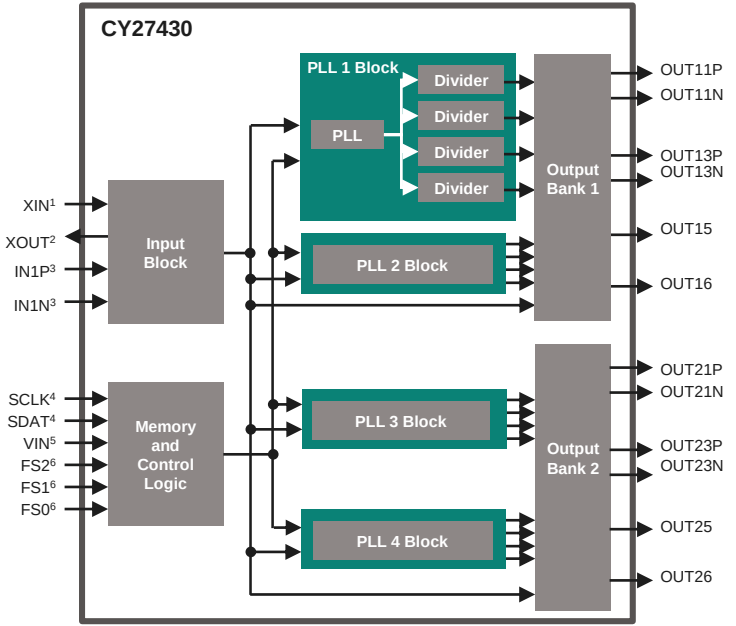
## Applications

Car infotainment and navigation systems

## Features

- **Eight outputs**
  - Four configurable (differential or single-ended)
  - Four single-ended
- **Specifications**
  - High frequency: 700-MHz differential, 250-MHz single-ended
  - RMS phase jitter <0.7 ps (typical)
  - Reference clock support for PCIe 3.0, SATA 2.0, and 10 GbE
  - AEC Q-100 qualified (-40 °C to +105 °C)
- **Additional features**
  - Pin select and $I^2C$ programming
  - Configurable as zero or non-zero delay buffer
  - Glitch-free frequency switching
  - Frequency select
  - Early/late clocks
  - PLL cascading
  - Voltage-controlled frequency synthesis (VCFS)
- **RoHS-compliant package**
  - Available in a 7 mm x 7 mm 48-pin QFN package

## Four-PLL Spread-Spectrum clock generator




## Collateral

**Datasheet**: 4-PLL high-performance clock generator (CY27430)

## Availability

**Production**: Now

[1] Crystal input
[2] Crystal output
[3] Reference clock inputs
[4] Serial port
[5] Voltage input pin for VCFS
[6] Frequency select inputs


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# CY29430: High-Performance 1-PLL Clock Synthesizer

## Applications

Routers, switches, base stations, storage area networks, network backplanes, wireless infrastructure, military/aerospace, video, test and measurement

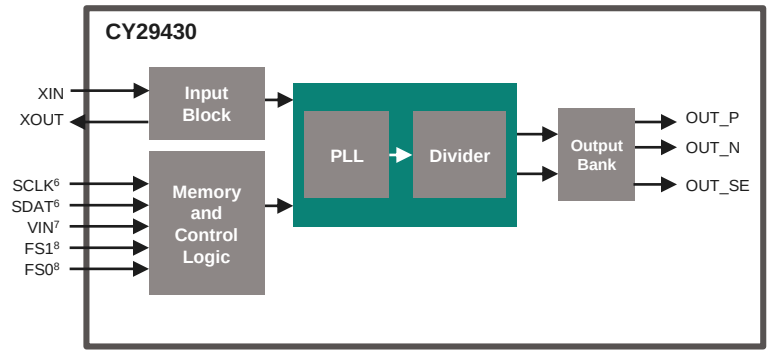
## Features

- **Outputs**
  - LVPECL[1], LVDS[2], HCSL[3],CML[4], and LVCMOS outputs
- **Specifications**
  - High frequency: 2.1-GHz differential, 250-MHz single-ended
  - RMS phase jitter[5]: ~110 fs typical (12-kHz to 20-MHz frequency offsets) for output greater than 150 MHz
  - Voltage-controlled frequency synthesis (VCFS) with tuneable pull range of 50 ppm to 275 ppm
  - Frequency Select option to choose from four pre-programmed configurations
  - Pin select and I²C programming
  - $V_{DD}$ support: 1.8 V, 2.5 V, and 3.3 V
  - Industrial temperature grades (-40 °C to +105 °C)
- **RoHS-Compliant Package**
  - Available in a 3 mm x 3 mm 16-pin QFN[9] package

## Collateral

**Datasheet**: 1-PLL High-Performance Clock Synthesizer (CY29430)

**High-Performance 1-PLL Clock Synthesizer**




## Availability

**Production**: Now

[1] Low-voltage positive emitter coupled logic
[2] Low-voltage differential signaling
[3] High-speed current steering logic
[4] Current mode logic
[5] The uncertainty of the clock rising and falling edge timing
[6] I²C input
[7] Voltage input pin for VCFS
[8] Frequency select inputs
[9] Quad Flat No-leads


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