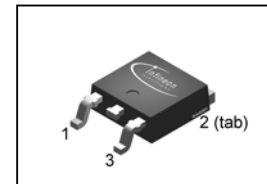


SIPMOS® Small-Signal-Transistor
Features

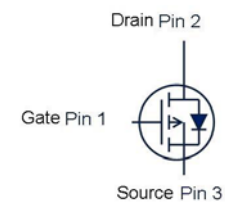
- P-Channel
- Enhancement mode
- Normal level
- Avalanche rated
- Pb-free lead plating; RoHS compliant
- ° Qualified according to AEC Q101


Product Summary

V_{DS}	-100	V
$R_{DS(on),max}$	0.24	Ω
I_D	-15	A

PG-TO252-3


Type	Package	Marking	Lead free	Packing
SPP15P10P G	PG-TO220-3	15P10P	Yes	Non dry
SPD15P10P G	PG-TO252-3	15P10P	Yes	Non dry


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	-15	A
		$T_C=100\text{ °C}$	-10.6	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}$	-60	
Avalanche energy, single pulse	E_{AS}	$I_D=-15\text{ A}$, $R_{GS}=25\text{ }\Omega$	230	mJ
Gate source voltage	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	128	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 175	°C
ESD Class			1C (1kV to 2kV)	
Soldering temperature			260 °C	
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - soldering point	R_{thJC}		-	-	1.17	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, steady state	-	-	75	
		6 cm ² cooling area ¹⁾ , steady state	-	-	45	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=-1\text{ mA}$	-100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-1.54\text{ mA}$	-4	-3	-2.1	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	-0.1	-1	μA
		$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$	-	-10	-100	
Gate-source leakage current	I_{GSS}	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-10\text{ V}$, $I_D=-10.6\text{ A}$	-	160	240	m Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=-10.6\text{ A}$	4.7	9.3	-	S

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=-25\text{ V},$ $f=1\text{ MHz}$	-	961	1280	pF
Output capacitance	C_{oss}		-	237	315	
Reverse transfer capacitance	C_{rss}		-	100	150	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-50\text{ V},$ $V_{GS}=-10\text{ V},$ $I_D=-15\text{ A}, R_G=6\ \Omega$	-	9.5	15.9	ns
Rise time	t_r		-	23	33	
Turn-off delay time	$t_{d(off)}$		-	33	43	
Fall time	t_f		-	16	20	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=-80\text{ V}, I_D=-15\text{ A},$ $V_{GS}=0\text{ to }-10\text{ V}$	-	5.4	7.2	nC
Gate to drain charge	Q_{gd}		-	18	27	
Gate charge total	Q_g		-	37	48	
Gate plateau voltage	$V_{plateau}$		-	5.9	-	V

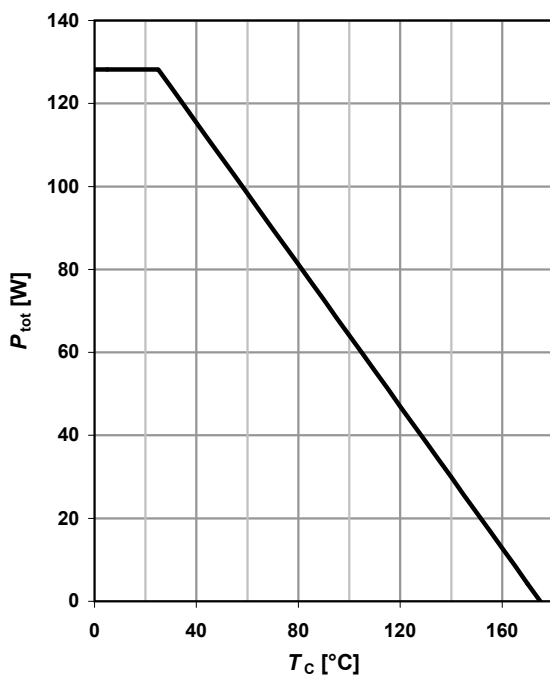
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	-15	A
Diode pulse current	$I_{S,pulse}$		-	-	60	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=-15\text{ A},$ $T_j=25\text{ °C}$	-	-0.94	-1.35	V
Reverse recovery time	t_{rr}	$V_R=50\text{ V}, I_F= I_S ,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	100	150	ns
Reverse recovery charge	Q_{rr}		-	419	628	nC

²⁾ See figure 16 for gate charge parameter definition

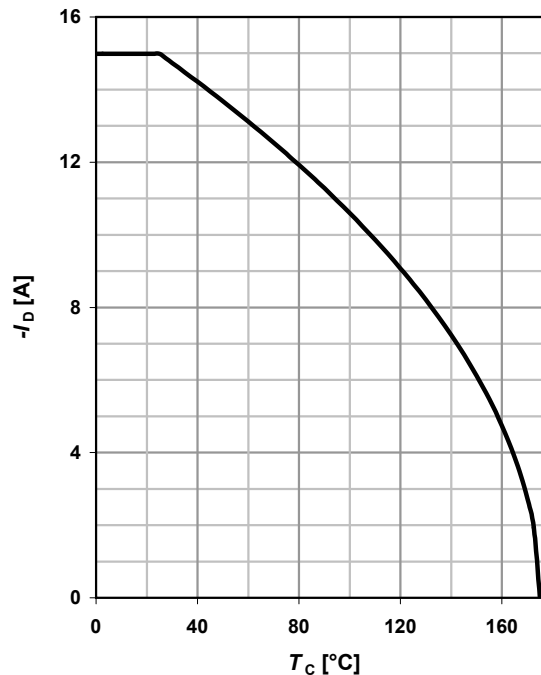
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

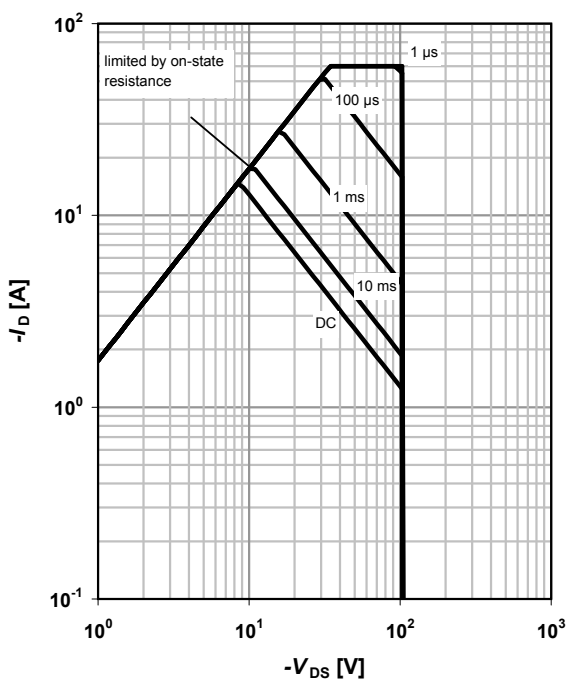
$$I_D = f(T_C); |V_{GS}| \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

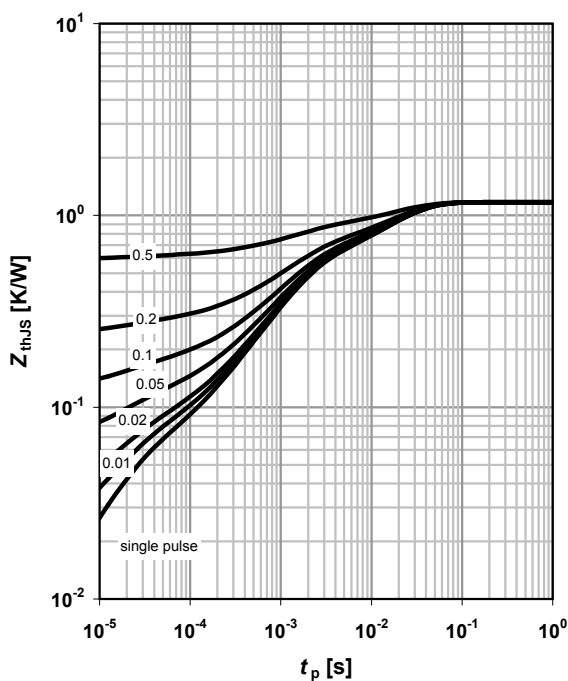
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

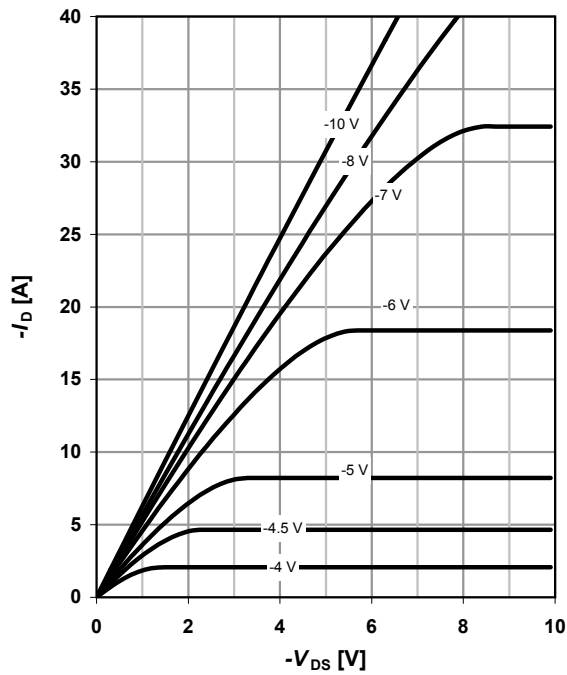
parameter: $D = t_p / T$



5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

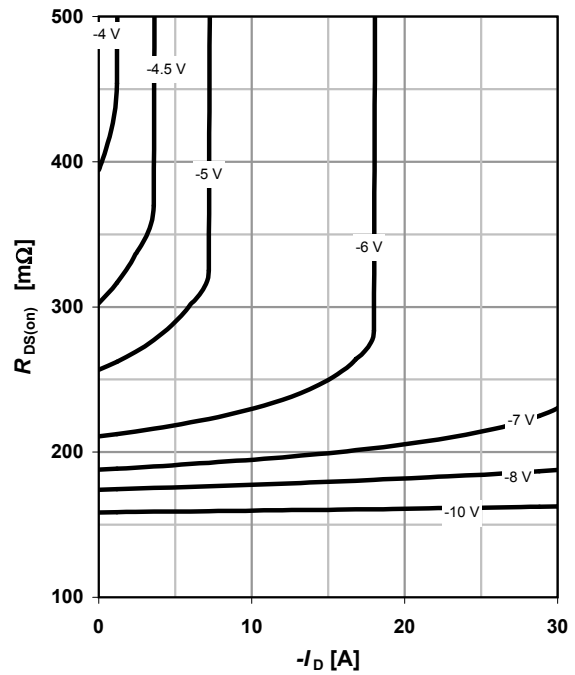
parameter: V_{GS}



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

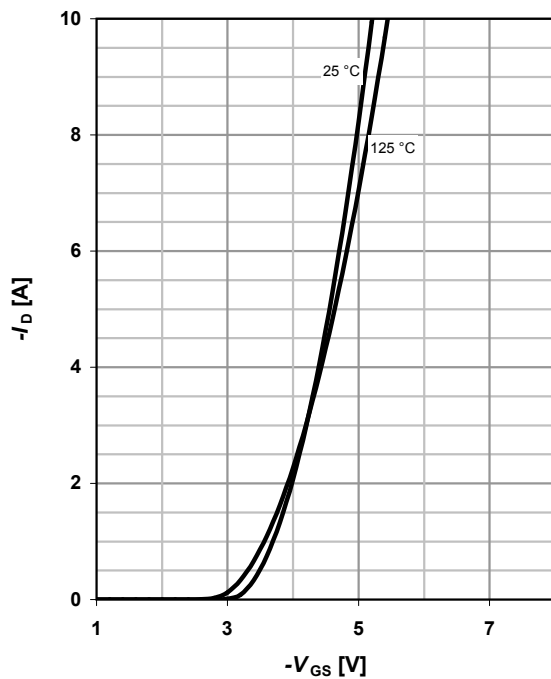
parameter: V_{GS}



7 Typ. transfer characteristics

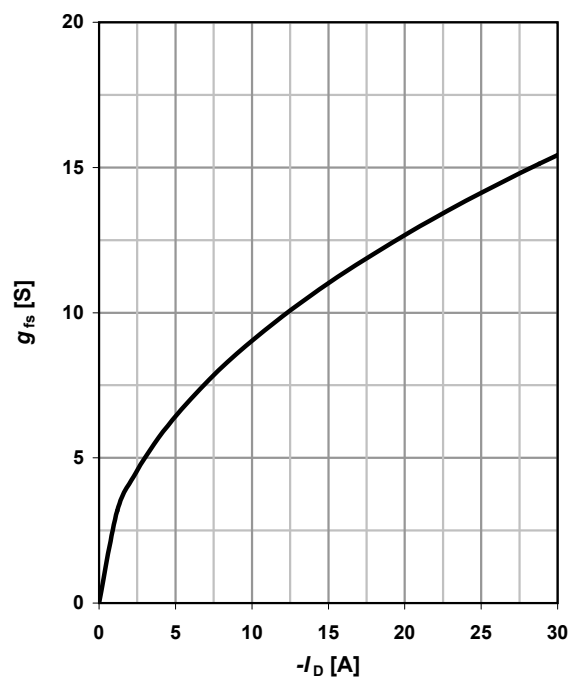
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

parameter: T_j



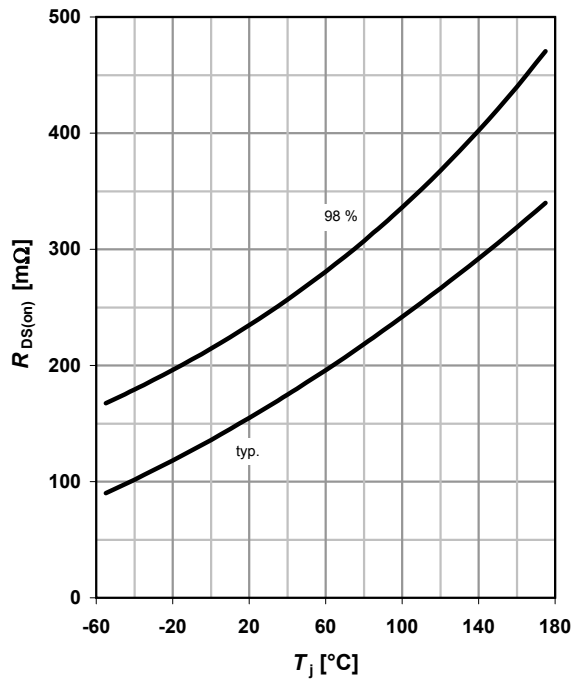
8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$



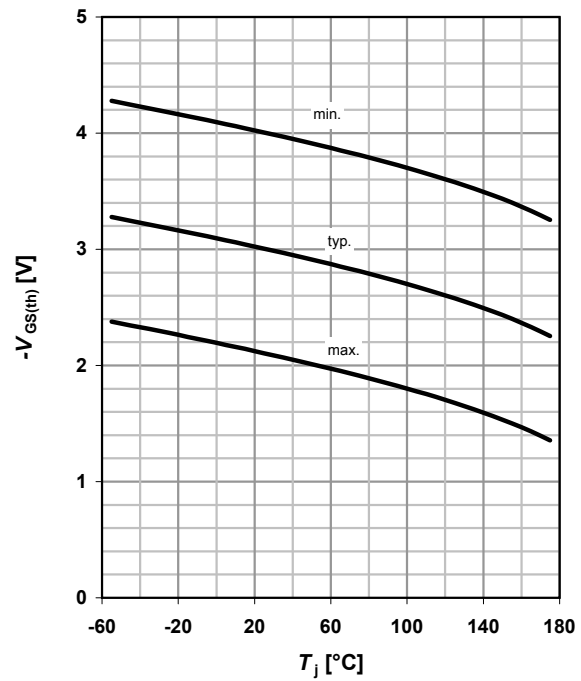
9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = -10.6 \text{ A}; V_{GS} = -10 \text{ V}$$



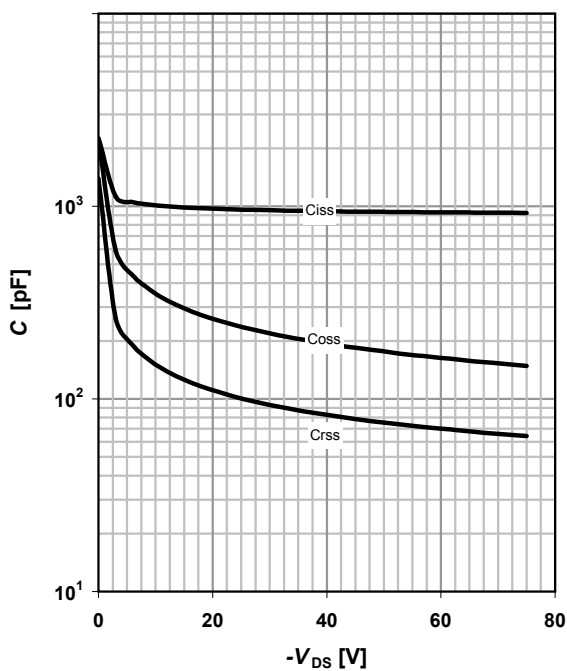
10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = -1.54 \text{ mA}$$



11 Typ. capacitances

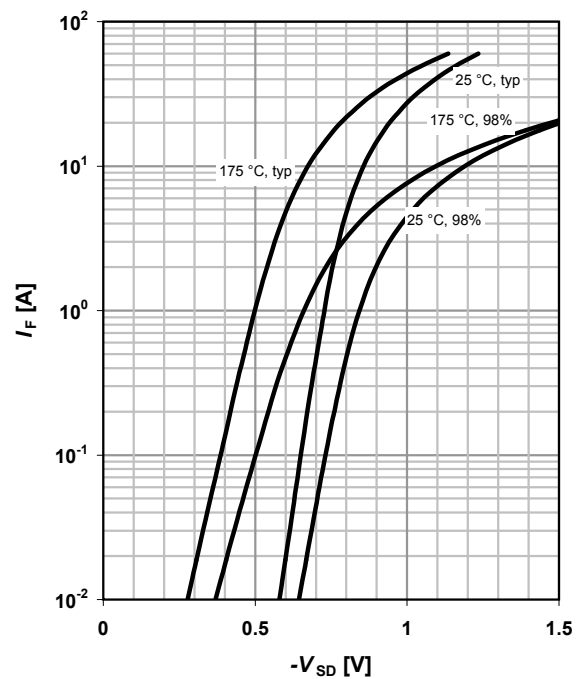
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

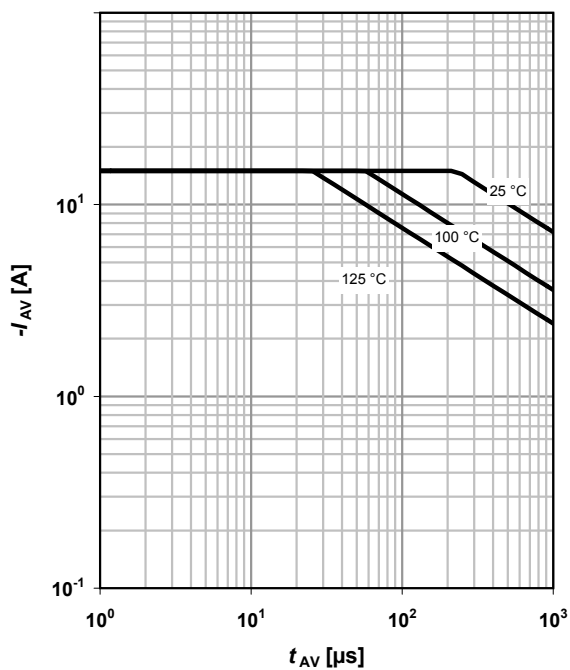
parameter: T_j



13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

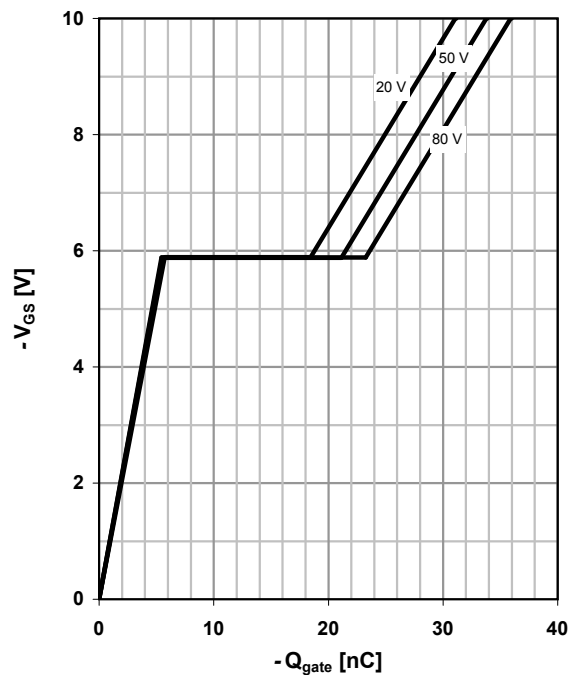
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

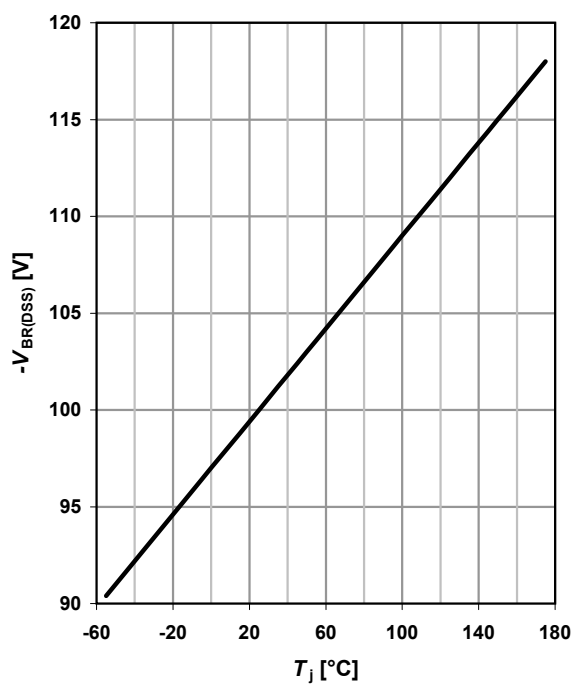
$$V_{GS}=f(Q_{\text{gate}}); I_D=-15\ \text{A pulsed}$$

parameter: V_{DD}

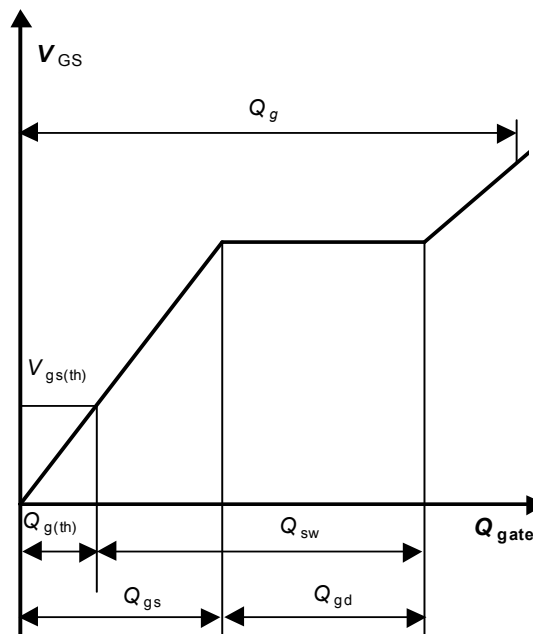


15 Drain-source breakdown voltage

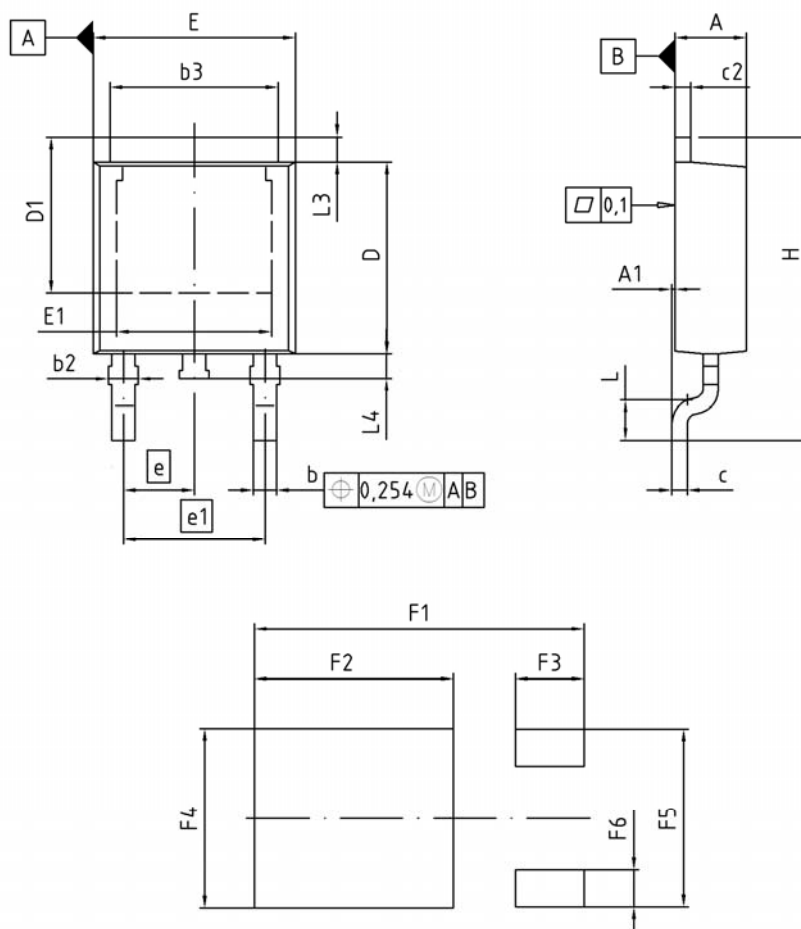
$$V_{BR(DSS)}=f(T_j); I_D=-1\ \text{mA}$$



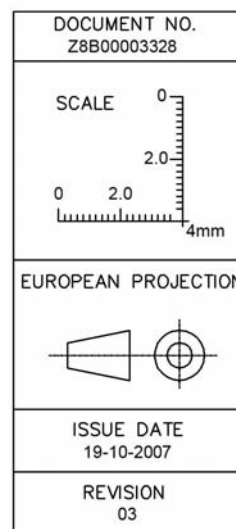
16 Gate charge waveforms

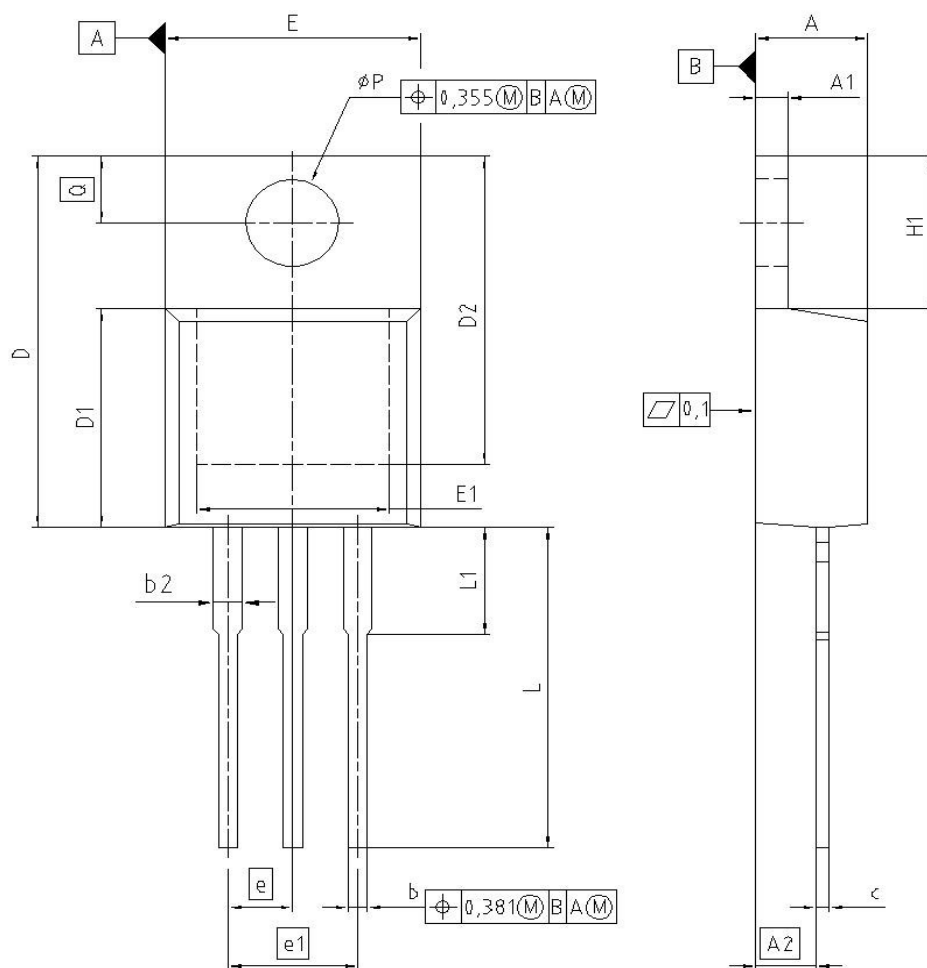


Package Outline: PG-TO-252-3

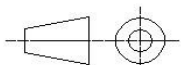


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051



PG-TO220-3: Outline


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	1.170	1.400	0.046	0.055
A2	2.215	2.718	0.087	0.107
b	0.650	0.864	0.026	0.034
b2	0.635	1.778	0.025	0.070
c	0.330	0.600	0.013	0.024
D	14.808	15.950	0.583	0.628
D1	8.509	9.450	0.335	0.372
D2	12.850	13.100	0.506	0.516
E	9.700	10.363	0.382	0.408
E1	6.500	8.600	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
N	3		3	
H1	5.900	6.900	0.232	0.272
L	13.000	14.000	0.512	0.551
L1	-	4.800	-	0.189
øP	3.700	3.886	0.146	0.153
Q	2.600	3.000	0.102	0.118

REFERENCE JEDEC TO220
SCALE 0 2.5 5mm
EUROPEAN PROJECTION 
ISSUE DATE 01-06-2005
FILE TO220_1

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