22 W auxiliary power supply for commercial air-conditioner using ICE5GR2280AG

REF_5GR2280AG_22W1

About this document

Scope and purpose

This document is a reference design for a 22 W auxiliary power supply for a commercial air-conditioner unit with the latest fifth-generation Infineon Fixed-Frequency (FF) CoolSET™ ICE5GR2280AG. The power supply is designed with a universal input compatible with most geographic regions and three outputs (+12 V/1 A isolated, +20 V/0.35 A isolated, +15 V/200 mA non-isolated) on a single-layer PCB.

Highlights of the auxiliary power supply for the commercial air-conditioner unit are:

- Tightly regulated output voltages, high efficiency under light load and low standby power
- Comprehensive protection feature CoolSET™ with integrated input Line Over Voltage Protection (LOVP) and externally implemented brown-in protection (GATE pin resistor to GND)
- Auto-restart protection scheme to minimize interruption and enhance end-user experience

Intended audience

This document is intended for power supply design engineers who are designing auxiliary power supplies for commercial air-conditioner units that are efficient, reliable and easy to design.

Table of contents

1 System introduction

With the growing household trend for internet-connected devices, the new generation of home appliances such as air-conditioners are equipped with advanced features such as wireless control and monitoring capability, smart sensors and touch screen display. These can transform a static product into an interactive and intelligent home appliance, capable of adapting to the smart-home theme. To support this trend, Infineon has introduced the latest fifth-generation FF CoolSET™ to address this need in an efficient and cost-effective manner.

An auxiliary SMPS is needed to power the various modules and sensors, which typically operate from a stable DC voltage source. The Infineon CoolSET™ (as shown in Figure 1) forms the heart of the system, providing the necessary protection and AC-DC conversion from the mains to multiple regulated DC voltages to power the various blocks.

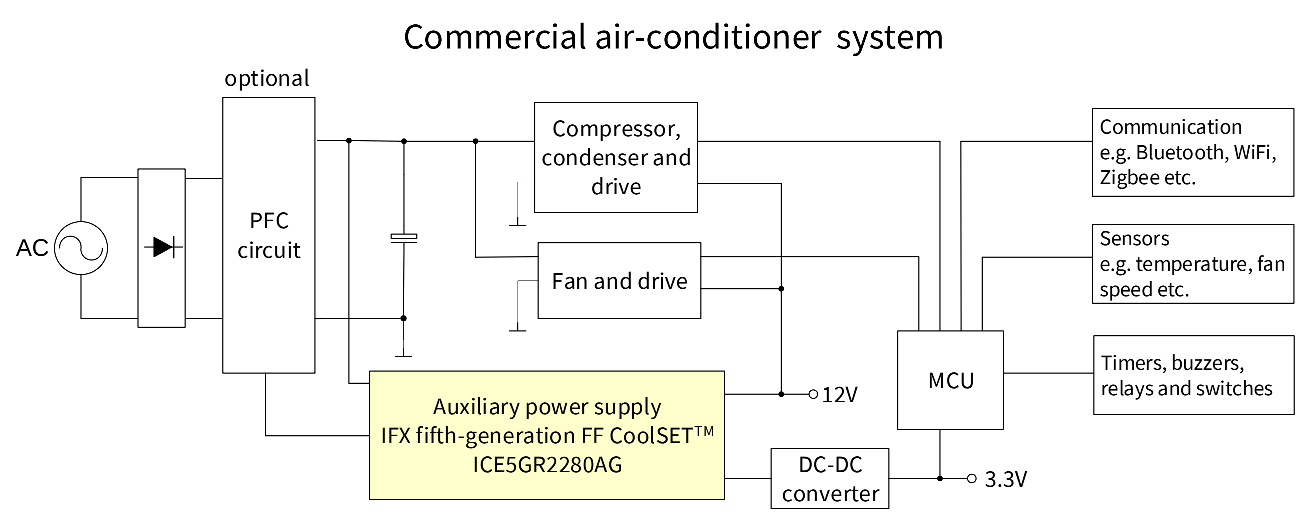


Figure 1 Simplified commercial air-conditioner unit system block diagram example

Table 1 lists the system requirements for auxiliary power supply for the commercial air-conditioner unit, and the corresponding Infineon solution is shown in the right-hand column.

Table 1 System requirements and Infineon solutions

	System requirement for commercial air-conditioner unit power supply	Infineon solution – ICE5GR2280AG
1	High efficiency under light load and low standby power	New FF control and Active Burst Mode (ABM)
2	Robust system and protection features	Comprehensive protection feature CoolSET™ in DSO-12 package with integrated LOVP and externally implemented brown-in protection
3	Auto-restart protection scheme to minimize interruption to enhance end-user experience	All protections are in auto-restart

1.1 High efficiency under light load and low standby power

During typical air-conditioner operation, the power requirement fluctuates according to various use cases. However, in most cases where room temperature is already stabilized, the indoor and outdoor air-conditioner units will reside in an idle state, in which the loading toward the auxiliary power supply is low. It is crucial that the auxiliary power supply operates as efficiently as possible, because it will be in this particular state for most of the period. Under light-load conditions, losses incurred with the power switch are usually dominated by the switching operation. The choice of switching scheme and frequency play a crucial role in ensuring high conversion efficiency.

In this reference design, ICE5GR2280AG was primarily chosen due to its frequency reduction switching scheme. Compared with a traditional FF Flyback, the CoolSET^{TM} reduces its switching frequency from medium to light load, thereby minimizing switching losses. Therefore, an efficiency of more than 80 percent is achievable under 25 percent loading conditions and nominal input voltages.

1.2 Simplified circuitry with good integration of power and protection features

To relieve the designer of the complexity of PCB layout and circuit design, CoolSET^{TM} is a highly integrated device with both a controller and a HV MOSFET integrated into a single, space-saving DSO-12 package. These certainly help the designer to reduce component count as well as simplifying the layout into a single-layer PCB design for ease of manufacturing, using the traditional cost-effective wave-soldering process.

The various protection features of the CoolSET™, such as integrated LOVP and externally implemented brown-in protection, boost the reliability of the power supply.

1.3 Auto-restart protection scheme to minimize interruption to enhance end-user experience

For a commercial air-conditioner unit, it would be annoying to both the end-user and the manufacturer if the system were to halt and latch after protection. Accessibility of the input AC plug may also be difficult; therefore, to minimize interruption, the CoolSET^{TM} implements auto-restart mode for all abnormal protections.

2 Reference board design

This document provides complete design details including specifications, schematics, Bill of Materials (BOM), PCB layout, and transformer design and construction information. Performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans and so on are also included.

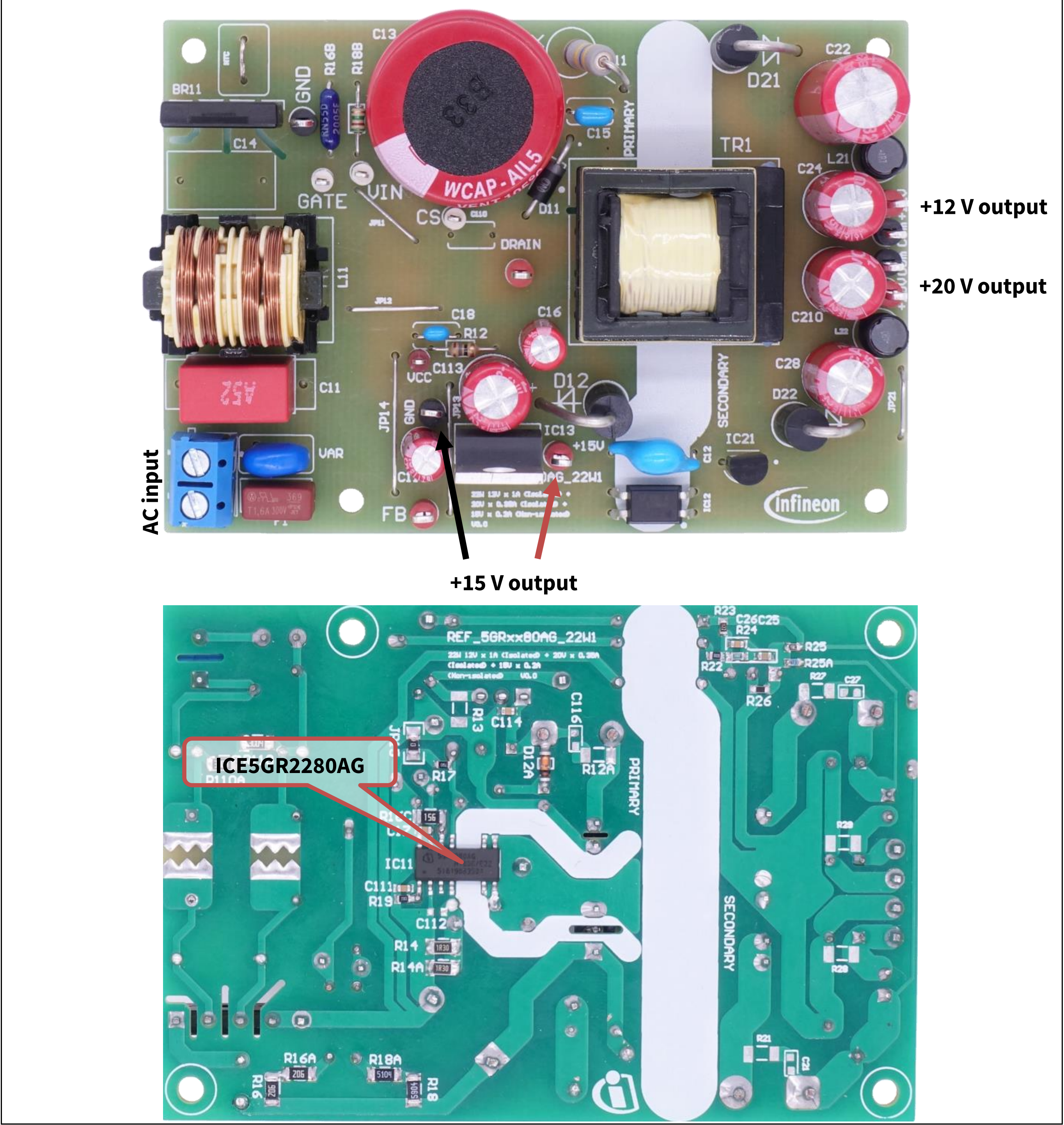


Figure 2 REF_5GR2280AG_22W1

3 Power supply specifications

The table below shows the minimum acceptable performance of the design at 25°C ambient temperature. Actual performance is listed in the measurements section.

Table 2 Specifications of REF_5GR2280AG_22W1

Description	Symbol	Min.	Type	Max.	Units	Comments
Input						
Voltage	V_{IN}	90	–	264	V AC	2 wires (no P.E.)
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load input power	P_{stby_NL}	–	–	120	mW	
600 mW load input power	P_{stby_ML}	–	–	1	W	
Brown-in	V_{BI}	–	75	–	V AC	
LOVP	V_{LOVP}	–	300	–	V AC	
Output						
Output voltage 1	V_{OUT1}	–	12	–	V	± 2 percent
Output current 1	I_{OUT1}	–	–	1	A	
Output voltage ripple 1	$V_{RIPPLE1}$	–	–	200	mV	
Output voltage 2	V_{OUT2}	–	15	–	V	± 1 percent
Output current 2	I_{OUT2}	–	–	0.2	A	
Output voltage ripple 2	$V_{RIPPLE2}$	–	–	200	mV	
Output voltage 3	V_{OUT3}	–	20		V	± 2 percent
Output current 3	I_{OUT3}	–	–	0.35	A	
Output voltage ripple 3	$V_{RIPPLE3}$	–	–	200	mV	
Output power	P_{OUT_Nom}		22	–	W	
Output over-current protection (+12 V)	I_{OCP}		2	–	A	0.2 A load on +15 V and 0.35 A load on +20 V load
Start-up time	t_{start_up}		–	350	ms	
Efficiency						
Maximum load	η	82	–	–	%	115 V AC/220 V AC
Average efficiency (25 percent, 50 percent, 75 percent, 100 percent)	η_{avg}	82	–	–	%	115 V AC/220 V AC
Environmental						
Conducted EMI			8		dB	Margin, CISPR 22 class B
ESD			±8		kV	EN 61000-4-2
Surge immunity						EN 61000-4-5
Differential mode			±2		kV	
Common mode			±4		kV	
PCB dimension			90 x 62 x 30		mm^3	L x W x H (single-layer PCB)

4 Circuit diagram

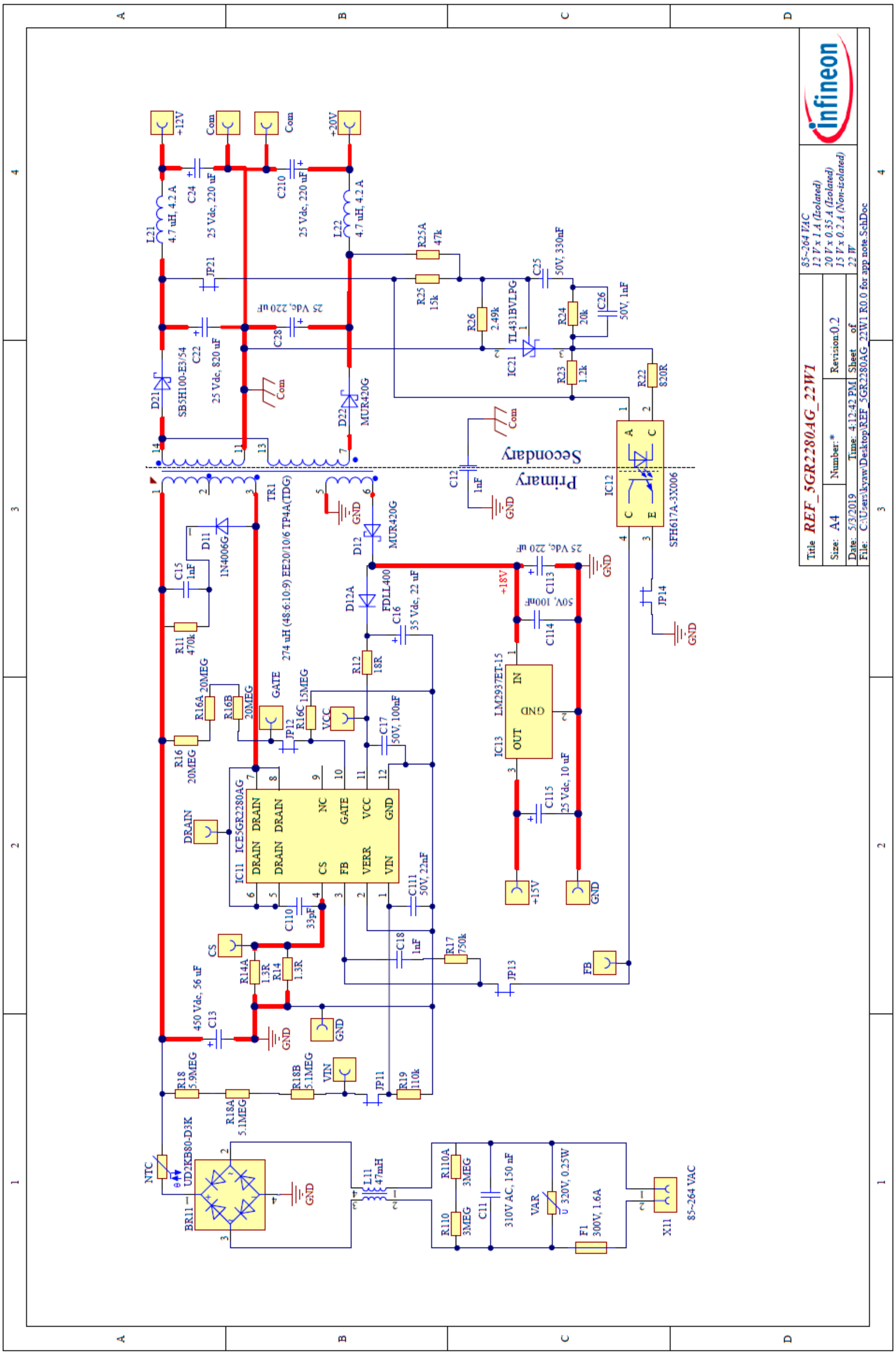


Figure 3 Schematic of REF_5GR2280AG_22W1

5 Circuit description

In this section, the design circuit for the SMPS unit will be briefly described by the different functional blocks. For details of the design procedure and component selection for the Flyback circuitry please refer to the IC design guide [2] and calculation tool [3].

5.1 EMI filtering and line rectification

The input of the power supply unit is taken from the AC power grid which is in the range of 90 V AC ~ 264 V AC. The fuse F1 is directly connected to the input line to protect the system in case of excess current entering the system circuit due to any fault. Following is the varistor VAR, which is connected across the input to absorb excess energy during line-surge transient. The X-capacitor C11 and Common Mode Choke (CMC) L11 reduce the EMI noise. R110 and R110A serve as the X-capacitor discharge resistor. The bridge rectifier BR11 rectifies the AC input into DC voltage, filtered by the bulk capacitor C13.

5.2 Flyback converter power stage

The Flyback converter power stage consists of transformer TR1, CoolSET™, secondary rectification diodes D21, D22 and D12, secondary output capacitors C22, C28 and C113 and output filter inductor L21 and L22.

When the primary HV MOSFET turns on, energy is stored in the transformer. When it turns off, the stored energy is discharged to the output capacitors and into the output load.

Secondary winding is sandwiched between two layers of primary winding to reduce leakage inductance. This improves efficiency and reduces voltage spikes.

For the output rectification, lower forward voltage and ultra-fast recovery diodes can improve efficiency. Capacitor C22, C28 stores the energy needed during output load jumps. LC filters L21/C24 and L22/C210 reduce the high-frequency ripple voltage.

The +15 V output is from the 15 V Low Drop-Out (LDO) regulator (IC13) with an input of +18 V. As such, this output should not be affected by cross-regulation. However, its input should be maintained within the operating range of the LDO.

5.3 Control of Flyback converter through fifth-generation FF CoolSET™ ICE5GR2280AG

5.3.1 Current Sensing (CS)

The ICE5GR2280AG is a current mode controller. The primary peak current is controlled cycle-by-cycle through the CS resistors R14 and R14A in the CS pin (pin 4). Transformer saturation can be avoided through Peak Current Limitation (PCL); therefore, the system is more protected and reliable.

5.3.2 Feedback and compensation network

Resistors R25 and R25A are used to sense the V_{OUT} and feedback (FB) to the reference pin (pin 1) of error amplifier IC21 with reference to the voltage at resistor R26. A type 2 compensation network C25, C26 and R24 is connected between the output pin (pin 3) and the reference pin (pin 1) of the IC21 to stabilize the system. The IC21 further connects to pin 2 of the optocoupler (IC12) with a series resistor R22 to convert the control signal to the primary side through the connection of pin 4 of the IC12 to ICE5GR2280AG FB pin (pin 3) and complete the control loop. Both the optocoupler IC12 and the error amplifier IC21 are biased by V_{OUT}; IC12 is a direct connection while IC21 is through an R23 resistor.

The FB pin of ICE5GR2280AG is a multi-function pin, which is used to select the entry burst power level (there are three levels available) through the resistor at the FB pin (R17) and also the burst-on/burst-off sense input during ABM.

5.4 Unique features of the fifth-generation FF CoolSET™ ICE5GR2280AG

5.4.1 Fast self-start-up and sustaining of V_{CC}

The IC uses a cascode structure to fast-charge the V_{CC} capacitor. Pull-up resistors R16, R16A and R16B connected to the GATE pin (pin 10) are used to initiate the start-up phase. At first, 0.2 mA is used to charge the V_{CC} capacitor from 0 V to 1.1 V. This is a protection which reduces the power dissipation of the power MOSFET during V_{CC} short-to-GND condition. Thereafter, a much higher charging current of 3.2 mA will charge the V_{CC} capacitor until the V_{CC_ON} is reached. Start-up time of less than 250 ms is achievable with a V_{CC} capacitor of 22 µF.

After start-up, the IC V_{CC} supply is usually sustained by the auxiliary winding of the transformer, which needs to support the V_{CC} to be above Under Voltage Lockout (UVLO) voltage (10 V typ.). In this reference board, the V_{CC} supply is tapped from the +18 V winding.

5.4.2 CCM, DCM operation with frequency reduction

ICE5GR2280AG can be operated in either Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM) with frequency-reduction features. This reference board is designed to operate in DCM at operating input voltage and load conditions. When the system is operating at high output load, the controller will switch at 125 kHz fixed frequency. In order to achieve a better efficiency between light load and medium load, frequency reduction is implemented as a function of V_{FB}, as shown in Figure 4. Switching frequency will not reduce further once the minimum switching frequency of 53 kHz is reached.

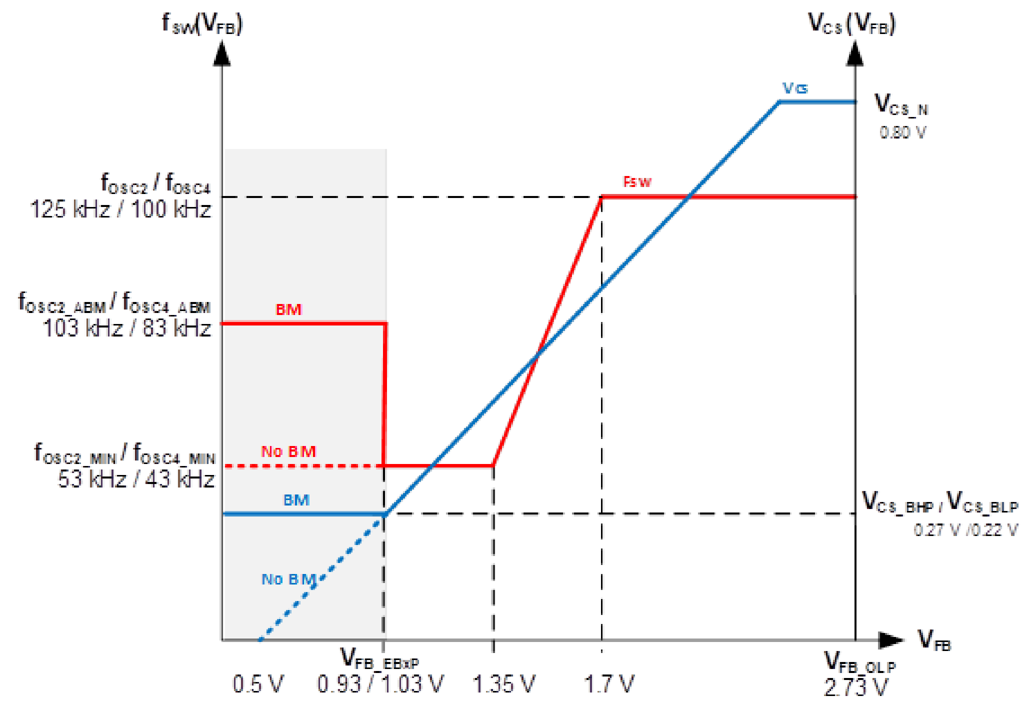


Figure 4 Frequency-reduction curve

5.4.3 Frequency jittering with modulated gate drive

The ICE5GR2280AG has a frequency jittering feature with modulated gate drive to reduce the EMI noise. The jitter frequency is internally set at 125 kHz (±4 percent), and the jitter period is 4 ms.

5.4.4 System robustness and reliability through protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. ICE5GR2280AG provides comprehensive protection to ensure the system is operating safely. This includes V_{IN} LOVP, V_{CC} OV and UV, over-load, over-temperature, CS short-to-GND and V_{CC} short-to-GND. When those faults are found, the system will enter protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and the failure conditions is shown in the table below.

Table 3 Protection functions of ICE5GR2280AG

Protection function	Failure condition	Protection mode
V_{CC} OV	V_{VCC} greater than 25.5 V	Odd-skip auto-restart
V_{CC} UV	V_{VCC} less than 10 V	Auto-restart
V_{IN} LOVP	V_{VIN} greater than 2.85 V	Non-switch auto-restart
Over-load	V_{FB} greater than 2.73 V and lasts for 54 ms	Odd-skip auto-restart
Over-temperature	T_J greater than 140°C (40°C hysteresis)	Non-switch auto-restart
CS short-to-GND	V_{CS} less than 0.1 V, lasts for 0.4 µs and three consecutive pulses	Odd-skip auto-restart
V_{CC} short-to-GND (V_{VCC} = 0 V, start-up = 50 MΩ and V_{DRAIN} = 90 V)	V_{VCC} less than 1.1 V, $I_{VCC\_Charge1} \approx -0.2$ mA	Cannot start up

5.5 Clamper circuit

A clamper network consisting of D11, C15 and R11 is used to reduce the switching voltage spikes across the DRAIN pin of the integrated HV MOSFET of the CoolSET™, which are generated by the leakage inductance of the transformer TR1. This is a dissipative circuit; therefore, R11 and C15 need to be fine-tuned depending on the voltage derating factor and efficiency requirement.

5.6 PCB design tips

For a good PCB design layout, there are several points to note.

- The switching power loop needs to be as small as possible (see Figure 5). There are four power loops in the reference design; one on the HV side and three on the output side. The HV side loop starts from the bulk capacitor (C13) positive terminal, primary transformer winding (pin 1 and pin 3 of TR1), CoolSET™, CS resistors and back to the C13 negative terminal. The first output side loop (+12 V output) starts at the transformer winding (pin 14 of TR1), output diode D21, output capacitor C22 and back to pin 11 of TR1. The second output side loop (+18 V output) starts at the transformer winding (pin 6 of TR1), output diode D12, output capacitor C113 and back to pin 5 of TR1. The third output side loop (+20 V output) starts at the transformer winding (pin 7 of TR1), output diode D22, output capacitor C28 and back to pin 11 of TR1.

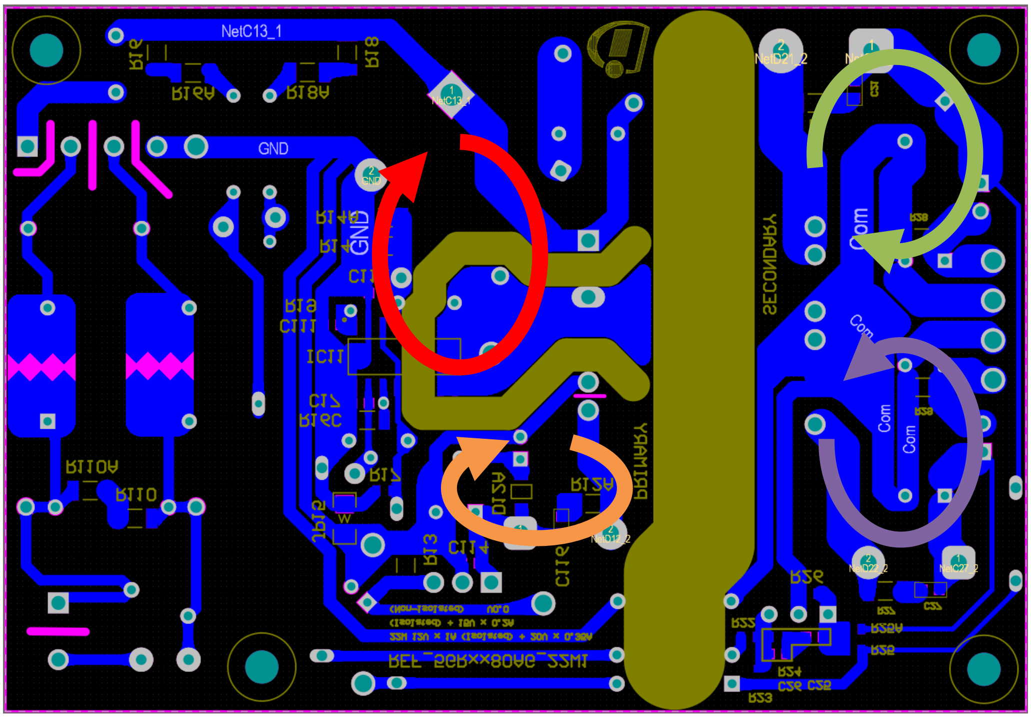


Figure 5 PCB layout tips

- Star-ground connection should be used to reduce High Frequency (HF) noise coupling that can affect the functional operation. The ground of the small-signal components, e.g. R16C, R17, R19, C17, C18 and C111, should connect directly to the IC ground (pin 12 of IC11).
- Separating the HV components and LV components, e.g. clamper circuit D11, C15 and R11, at the top part of the PCB and the other LV components at the lower part of the PCB can reduce the spark-over chance of the high energy surge during a lightning surge test.
- Make the PCB copper pour on the DRAIN pin of the MOSFET cover as wide an area as possible to act as a heatsink.

5.7 EMI reduction tips

EMI compliance is always a challenge for the power supply designer. There are several critical points to consider in order to achieve a satisfactory EMI performance.

- A proper transformer design can significantly reduce EMI. Low leakage inductance can incur a low switching spike and HF noise. Interlaced winding technique is the most common practice to reduce leakage inductance. Winding shield, core shield and whole transformer shield are also some of the techniques used to reduce EMI.
- Input CMC and X-capacitor greatly reduce EMI, but this is costly and impractical especially for low-power applications.
- Short-switching power-loop design in the PCB (as described in section 5.6) can reduce radiated EMI due to the antenna effect.
- An output diode snubber circuit can reduce HF noise.
- Ferrite beads can reduce HF noise, especially on critical nodes such as the DRAIN pin, clamper diode and output diode terminals. There is no ferrite bead used in this design, as this can reduce the efficiency due to additional losses, especially on high-current terminals.

6 PCB layout

6.1 Top side

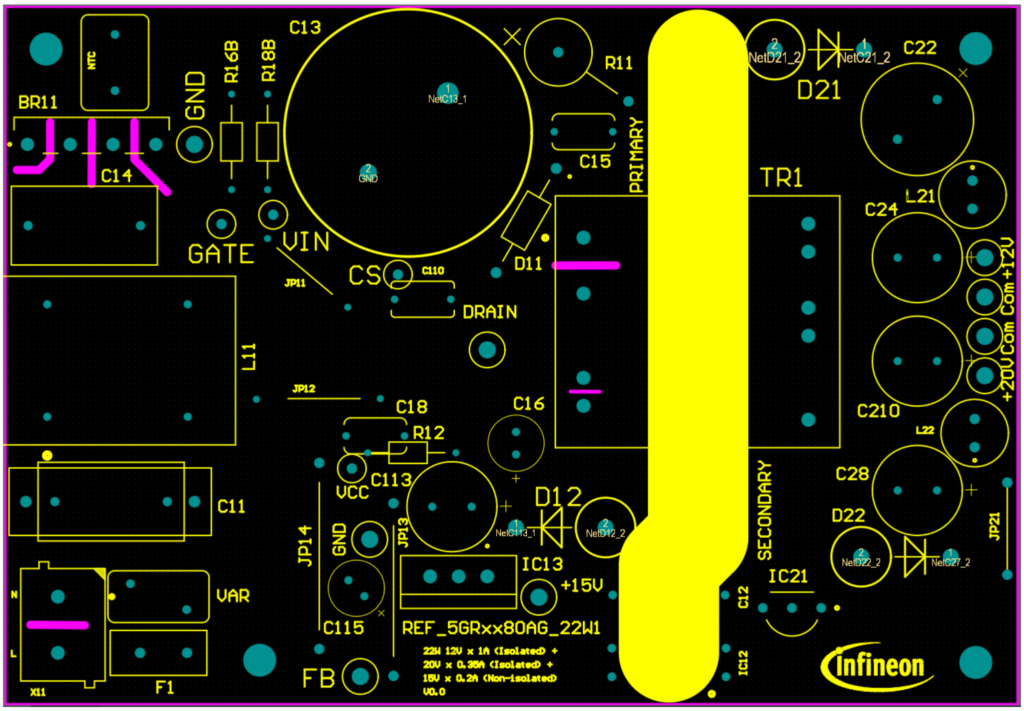


Figure 6 Top side component legend

6.2 Bottom side

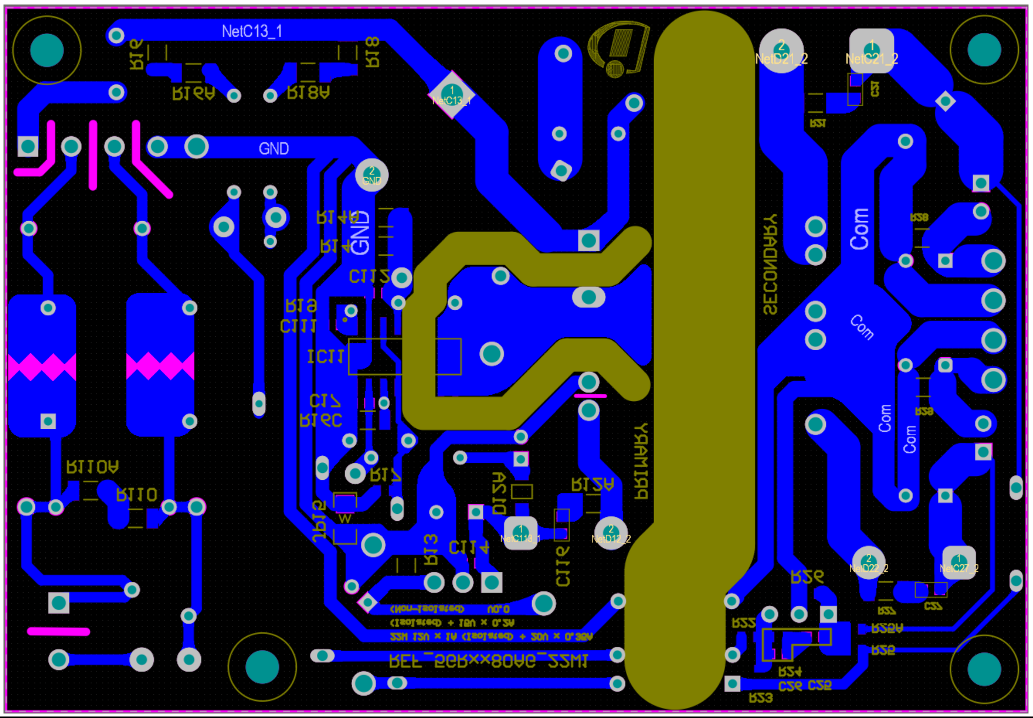


Figure 7 Bottom side copper and component legend

7 BOM

Table 4 BOM (V 0.2)

No.	Designator	Description	Part number	Manufacturer	Quantity
1	+20 V, +12 V, +15 V, DRAIN, FB	Connector	5010		5
2	C11	310 V AC, 150 nF	890334023025	Würth Elektronik	1
3	C12	1 nF	DE1E3RA102MA4BQ01F	Murata	1
4	C13	56 µF, 450 V	861111483003	Würth Elektronik	1
5	C15	1 kV, 1 nF	RDE7U3A102J2M1H03A	Murata	1
6	C16	35 V DC, 22 µF	860010572003	Würth Elektronik	1
7	C17, C114	50 V, 100 nF	885012206095	Würth Elektronik	2
8	C18	50 V, 1 nF	RDE5C1H102J0K1H03B	Murata	1
9	C22	25 V DC, 820 µF	860040475010	Würth Elektronik	1
10	C24, C113, C28, C210	25 V DC, 220 µF	860040474004	Würth Elektronik	4
11	C25	50 V, 330 nF	885012206121	Würth Elektronik	1
12	C26	50 V, 1 nF	885012206083	Würth Elektronik	1
13	C115	25 V DC, 10 µF	860010472002	Würth Elektronik	1
14	C111	50 V, 22 nF	885012206091	Würth Elektronik	1
15	Com, GND	Connector	5011		4
16	CS, GATE, V_{IN}	Connector	5002		3
17	D11	1N4006G	1N4006G		1
18	BR11	800 V, 1.2 A	UD2KB80-D3K	Shindengen	1
19	D21	100 V, 5 A	SB5H100-E3/54		1
20	D12A	150 V, 0.2 A	FDLL400		1
21	D12, D22	200 V, 4 A	MUR420G		2
22	F1	300 V, 1.6 A	36911600000		1
23	IC11	CoolSET™	ICE5GR2280AG	Infineon Technologies AG	1
24	IC12	SFH617A-3X006	SFH617A-3X006		1
25	IC13	LM2937ET-15	LM2937ET-15		1
26	IC21	TL431BVLPG	TL431BVLPG		1
27	JP11, JP12, JP21,JP13, JP14, NTC	Jumper			6
28	JP15	0 R, 0805			1
29	L11	47 mH, 0.75 A	750342434	Würth Elektronik	1
30	L21, L22	4.7 µH, 4.2 A	7447462047	Würth Elektronik	2
31	R11	470 k	PR02000204703JR500		1
32	R12	18 R	CFR-12JR-52-18R		1
33	R14, R14A	1.3 R	CRCW12061K30FKEA		2
34	R16, R16A	20 MEG	RC1206JR-0720ML		2
35	R16B	20 MEG	RN55D2005FB14		1
36	R16C	15 MEG	RC1206JR-0715ML		1
37	R17	750 k	CRCW0603750KFK		1
38	R18	5.9 MEG	CRCW12065M90FK		1
39	R18A	5.1 MEG	CRCW12065M10FK		1
40	R18B	5.1 MEG	299-5.1M-RC		1
41	R19	110 k	CRCW0603110KFK		1
42	R22	820 R	CRCW0603820RFK		1
43	R23	1.2 k	CRCW06031K20FK		1
44	R24	20 k	TNPW060320K0BY		1
45	R25	15 k	CRCW060315K0FKEB		1

46	R25A	47 k	CRCW060347K0FKEB		1
47	R26	2.49 k	CRCW06032K49FKEAC		1
48	R110, R110A	3 MEG	RC1206FR-073ML		2
49	TR1	274 µH (48:6:10:9) EE20/10/6 TP4A (TDG)	750344262 (R0.0)	Würth Elektronik	1
50	VAR	320 V, 0.25 W	B72207S2321K101	TDK Corporation	1
51	VCC	Connector	5000		1
52	X11	Connector	691 102 710 002	Würth Elektronik	1
53	PCB	90 mm x 62 mm (L x W) single layer, 2 oz, FR-4			1

8 Transformer specification

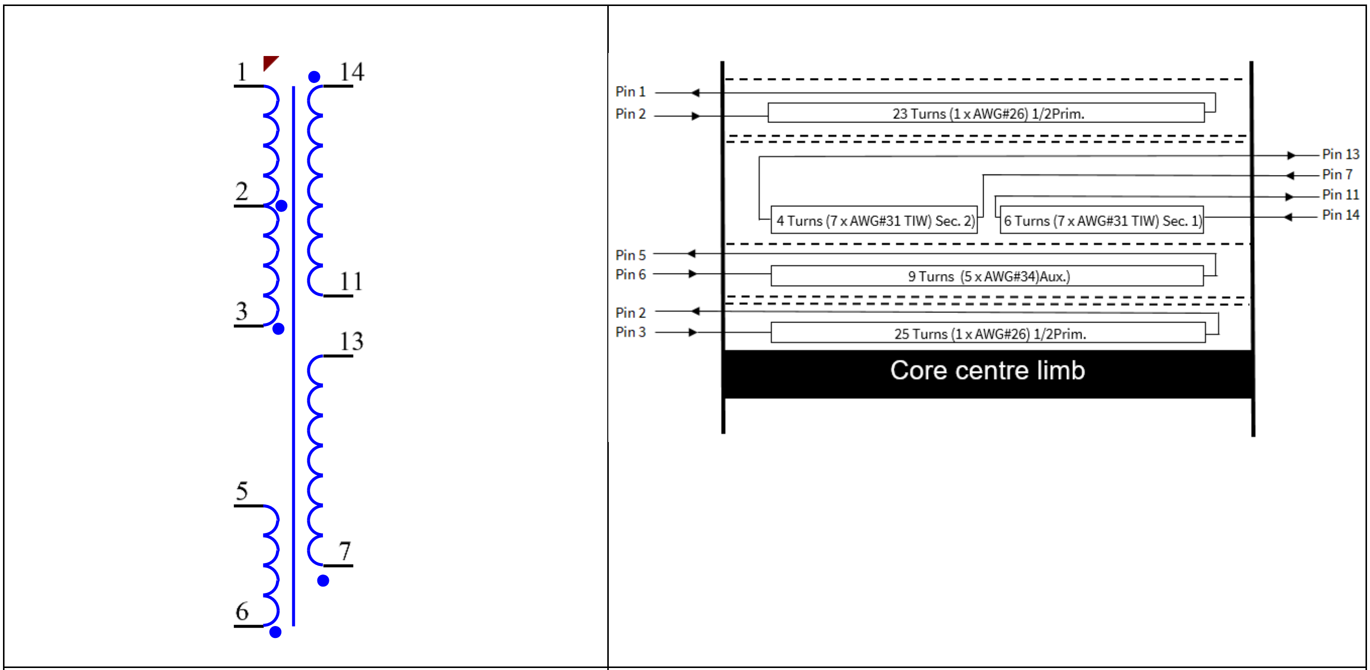
Refer to Appendix A for transformer design and Appendix B for WE transformer specification.

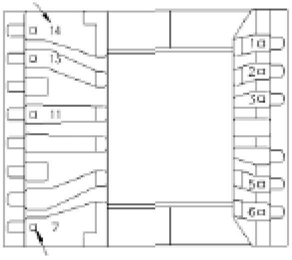
Core name and material: EE20/10/6, TP4A (TDG)

Würth Elektronik bobbin: 070-5643 (14-pin, THT, horizontal version)

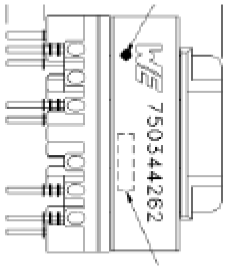
Primary inductance: $L_P = 274\ \mu H$ (±10 percent), measured between pin 1 and pin 3

Manufacturer and part number: Würth Elektronik Midcom (750344262) Rev. 00





Bottom view



Side view

Start	Stop	Turns	Wire size	Layer
3	2	25	1 x AWG#26	$^1/2$ Primary
6	5	9	5 x AWG#34	Auxiliary
14	11	6	7 x AWG#31 TIW	Secondary 1
7	13	4	7 x AWG#31 TIW	Secondary 2
2	1	23	1 x AWG#26	$^1/2$ Primary

Figure 8 **Transformer structure**

9 Measurement data and graphs

Table 5 Electrical measurements

Input (V AC/Hz)	P_{IN} (W)	+12 V_{OUT} (V)	+12 I_{OUT} (A)	+15 V_{OUT} (V)	+15 I_{OUT} (A)	+20 V_{OUT} (V)	+20 I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)	OLP P_{IN} (W)	OLP +12 I_{OUT} at 15 V/0.2 A and 20 V/0.35 A (A)
90 V AC/ 60 Hz	0.09	11.84	0.00	14.98	0.0000	20.19	0.00				33.70	1.38
	0.83	11.88	0.02	14.98	0.0100	20.06	0.01	0.59	70.84			
	6.75	11.82	0.25	15.00	0.0500	20.22	0.09	5.47	81.10	81.20		
	13.47	11.81	0.50	15.02	0.1000	20.24	0.18	10.95	81.28			
	20.03	11.80	0.75	15.03	0.1500	20.24	0.26	16.42	81.98			
	27.22	11.80	1.00	15.04	0.2000	20.24	0.35	21.89	80.43			
115 V AC/ 60 Hz	0.09	12.00	0.00	15.00	0.0000	20.00	0.00				33.30	1.46
	0.82	11.88	0.02	14.98	0.0100	20.06	0.01	0.59	71.71			
	6.68	11.83	0.25	15.00	0.0500	20.21	0.09	5.48	81.97	82.44		
	13.29	11.81	0.50	15.02	0.1000	20.00	0.18	10.91	82.07			
	19.68	11.80	0.75	15.03	0.1500	20.23	0.26	16.42	83.43			
	26.60	11.80	1.00	15.04	0.2000	20.24	0.35	21.89	82.30			
220 V AC/ 50 Hz	0.11	12.00	0.00	15.00	0.0000	20.00	0.00				34.60	1.61
	0.83	11.87	0.02	14.98	0.0100	20.07	0.01	0.59	70.83			
	6.69	11.83	0.25	15.00	0.0500	20.17	0.09	5.47	81.80	83.53		
	13.18	11.83	0.50	15.02	0.1000	20.19	0.18	10.95	83.08			
	19.36	11.81	0.75	15.02	0.1500	20.19	0.26	16.41	84.78			
	25.90	11.80	1.00	15.04	0.2000	20.20	0.35	21.88	84.47			
264 V AC/ 50 Hz	0.12	12.00	0.00	15.00	0.0000	20.00	0.00				35.70	1.70
	0.85	11.87	0.02	14.98	0.0100	20.08	0.01	0.59	69.18			
	6.74	11.84	0.25	15.00	0.0500	20.18	0.09	5.48	81.24	83.22		
	13.25	11.83	0.50	15.01	0.1000	20.18	0.18	10.95	82.62			
	19.40	11.82	0.75	15.02	0.1500	20.18	0.26	16.42	84.63			
	25.94	11.81	1.00	15.04	0.2000	20.19	0.35	21.88	84.37			

Minimum load condition: 12 V/20 mA, 15 V/10 mA, 20 V/10 mA

25 percent load condition: 12 V/0.25 A, 15 V/0.038 A, 20 V/90 mA

50 percent load condition: 12 V/0.50 A, 15 V/0.075 A, 20 V/0.18 A

75 percent load condition: 12 V/0.75 A, 15 V/0.113 A, 20 V/0.26 A

100 percent load condition: 12 V/1.00 A, 15 V/0.15 A, 20 V/0.35 A

9.1 Efficiency curve

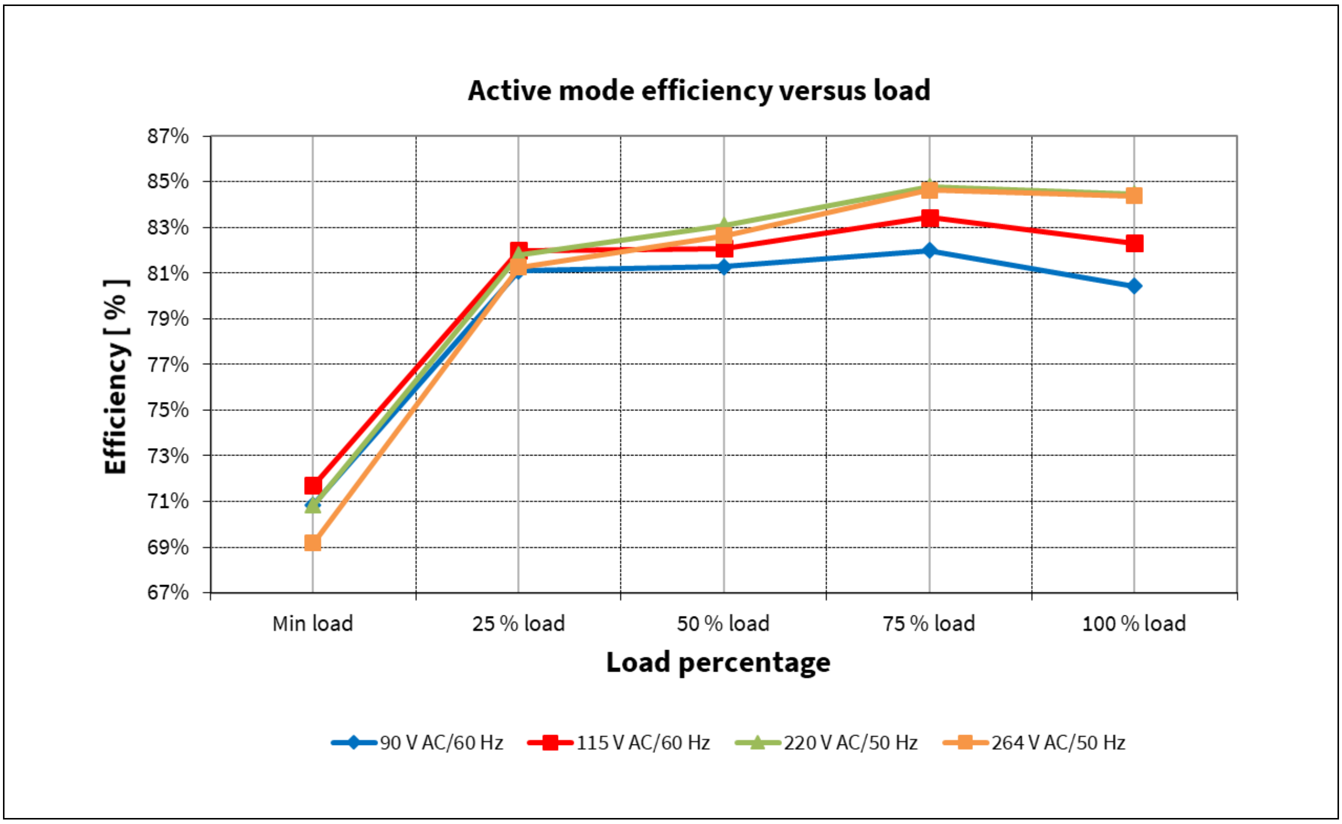


Figure 9 Efficiency vs. output load

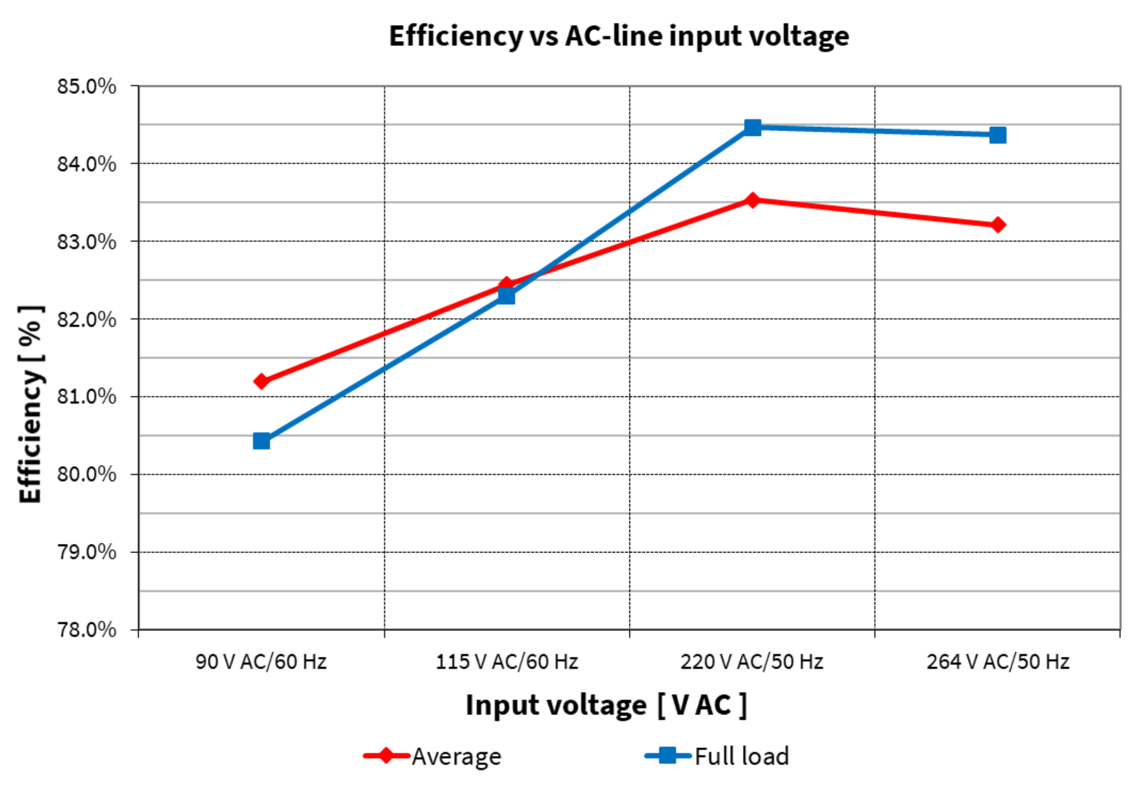


Figure 10 Efficiency vs. AC-line input voltage

9.2 Standby power

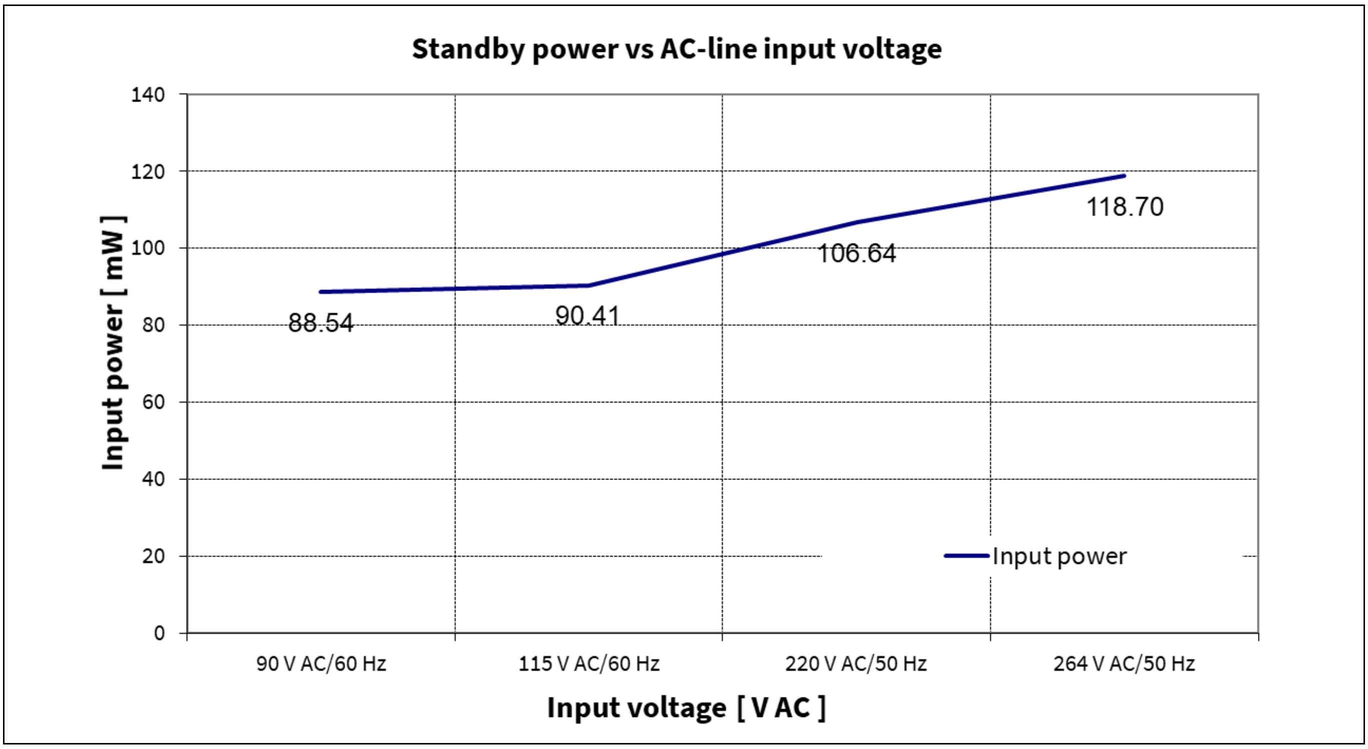


Figure 11 Standby power at no-load vs. AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)

9.3 Line and load regulation

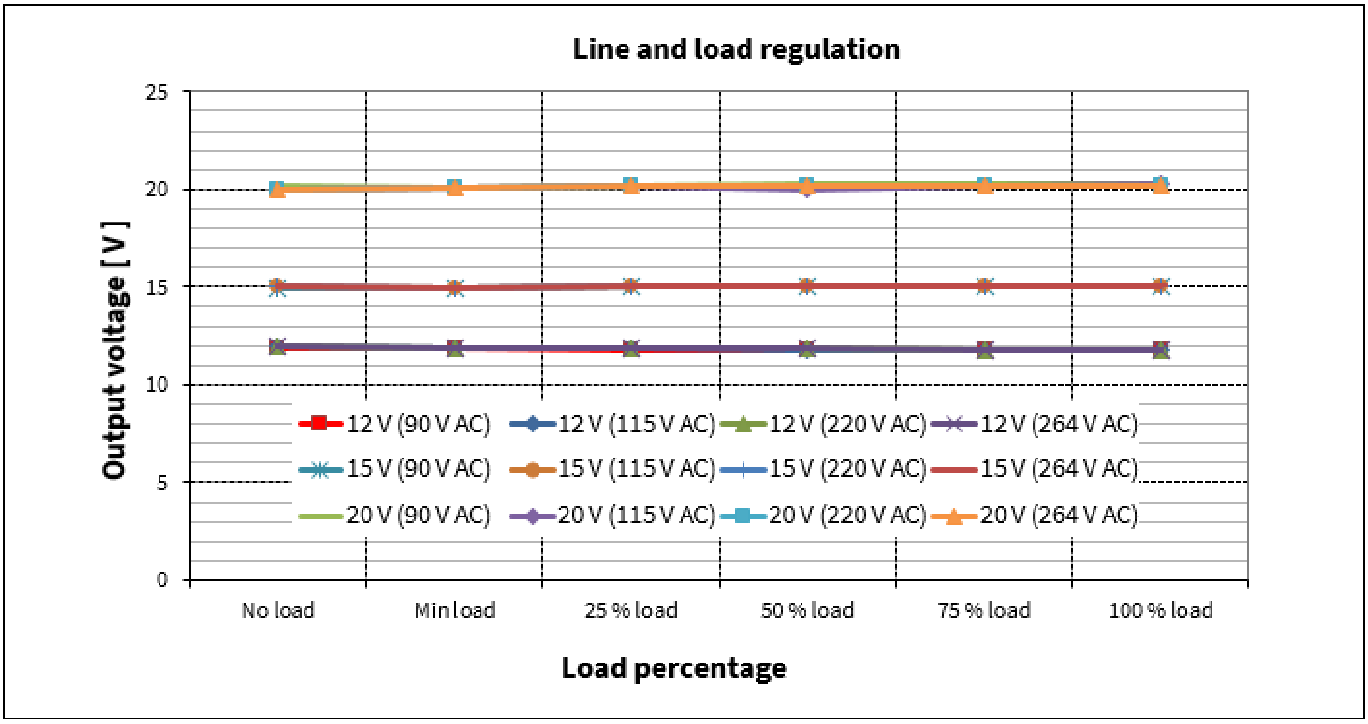


Figure 12 Output regulation vs. load at different AC-line input voltages

9.4 Maximum input power

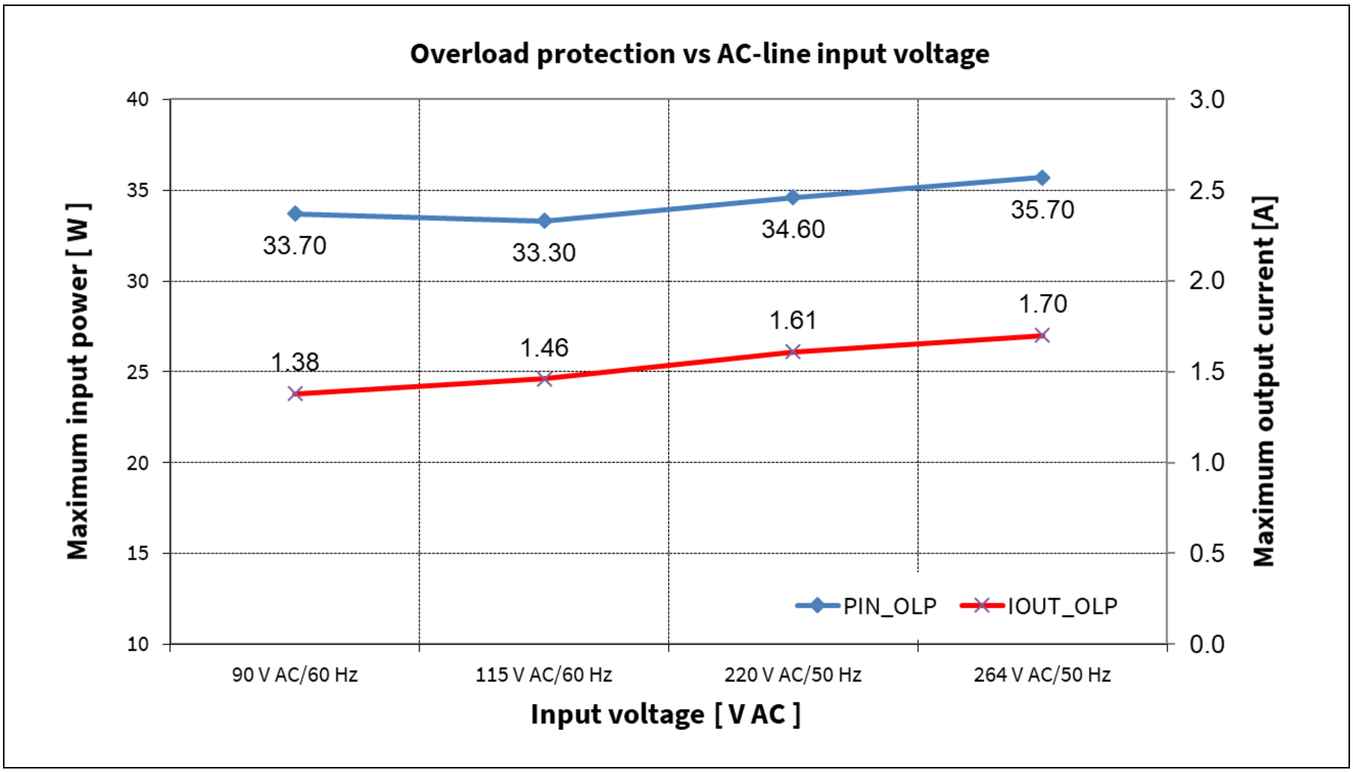


Figure 13 Maximum input power and output current (before over-load protection) vs. AC-line input voltage at 15 V/0.15 A load

9.5 Frequency reduction

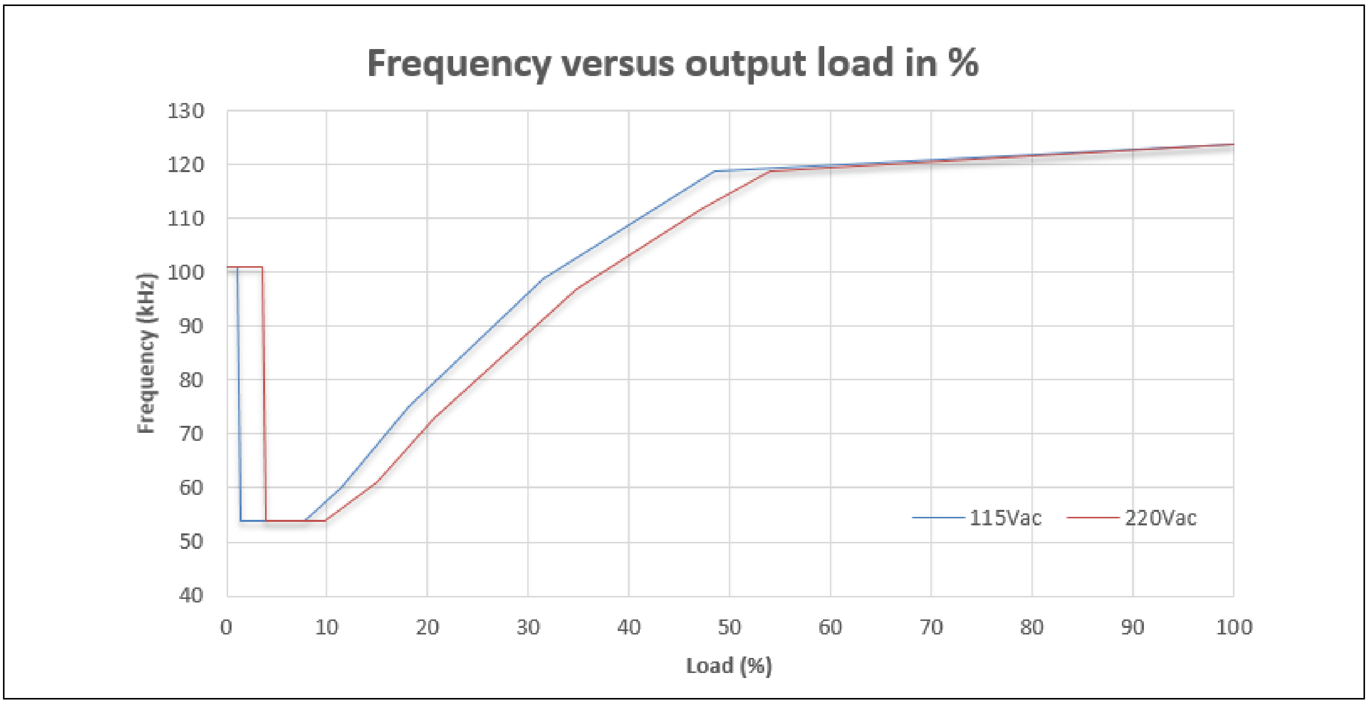


Figure 14 Frequency reduction curve vs. output load

9.6 ESD immunity (EN 61000-4-2)

This system was subjected to a ±8 kV ESD test according to EN 61000-4-2 for both contact and air discharge. A test failure was defined as non-recoverable.

- Air discharge: pass ±8 kV; contact discharge: pass ± 8 kV.

Table 6 System ESD test result

Description	ESD test	Level	Number of strikes			Test result
			+12 V_{OUT}	+20 V_{OUT}	Com	
115 V AC, 22 W	Contact	+8 kV	10	10	10	Pass
		-8 kV	10	10	10	Pass
	Air	+8 kV	10	10	10	Pass
		-8 kV	10	10	10	Pass
220 V AC, 22 W	Contact	+8 kV	10	10	10	Pass
		-8 kV	10	10	10	Pass
	Air	+8 kV	10	10	10	Pass
		-8 kV	10	10	10	Pass

9.7 Surge immunity (EN 61000-4-5)

The reference board was subjected to a surge immunity test (±2 kV DM and ±4 kV CM) according to EN 61000-4-5. It is tested at full load (22 W) using resistive load with LOVP disabled (add 2.4 V Zener diode at VIN pin to GND pin). A test failure was defined as non-recoverable.

- DM: pass ±2 kV[1]; CM: pass ±4 kV[1].

Table 7 System surge immunity test result

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
115 V AC, 22 W	DM	+2 kV	L → N	3	3	3	3	Pass[1]
		-2 kV	L → N	3	3	3	3	Pass[1]
	CM	+4 kV	L → G	3	3	3	3	Pass[1]
		+4 kV	N → G	3	3	3	3	Pass[1]
		-4 kV	L → G	3	3	3	3	Pass[1]
		-4 kV	N → G	3	3	3	3	Pass[1]
220 V AC, 22 W	DM	+2 kV	L → N	3	3	3	3	Pass[1]
		-2 kV	L → N	3	3	3	3	Pass[1]
	CM	+4 kV	L → G	3	3	3	3	Pass[1]
		+4 kV	N → G	3	3	3	3	Pass[1]
		-4 kV	L → G	3	3	3	3	Pass[1]
		-4 kV	N → G	3	3	3	3	Pass[1]

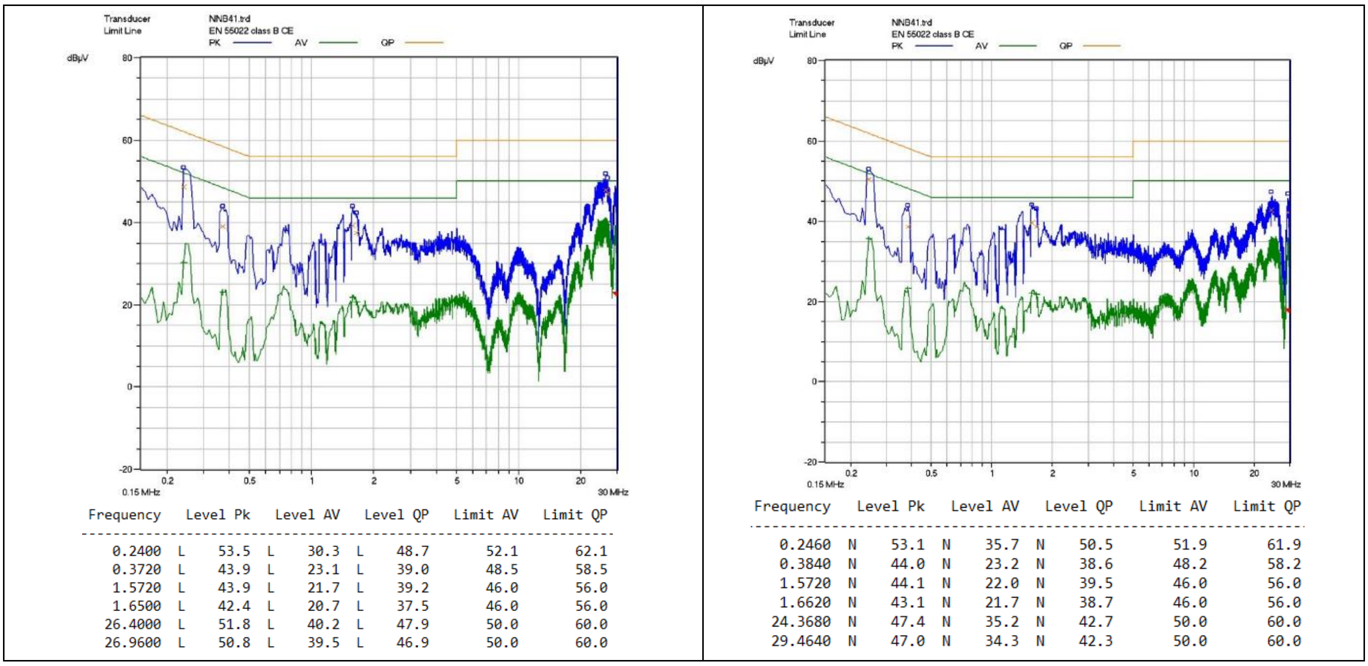
---

[1] Disable LOVP by clamping VIN pin voltage less than 2.75 V (add 2.4 V Zener diode at VIN pin to GND pin).

9.8 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The reference board is tested at full load (22 W) using resistive load at input voltage of 115 V AC and 220 V AC.

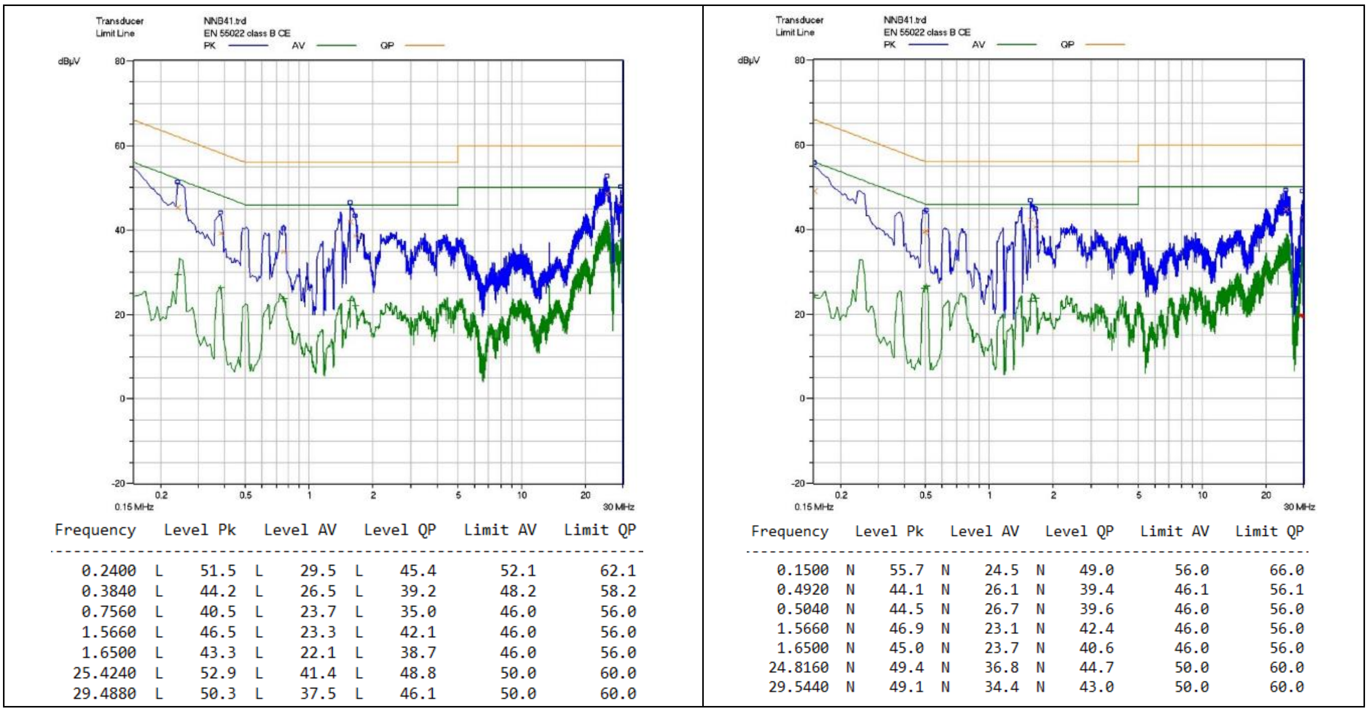
- 115 V AC: pass with greater than 10 dB margin for quasi-peak measurement
- 220 V AC: pass with greater than 10 dB margin for quasi-peak measurement



```
Frequency   Level Pk   Level AV   Level QP   Limit AV   Limit QP
-----------------------------------------------------------------
  0.2400  L   53.5  L    30.3  L    48.7       52.1       62.1
  0.3720  L   43.9  L    23.1  L    39.0       48.5       58.5
  1.5720  L   43.9  L    21.7  L    39.2       46.0       56.0
  1.6500  L   42.4  L    20.7  L    37.5       46.0       56.0
 26.4000  L   51.8  L    40.2  L    47.9       50.0       60.0
 26.9600  L   50.8  L    39.5  L    46.9       50.0       60.0
```

```
Frequency   Level Pk   Level AV   Level QP   Limit AV   Limit QP
-----------------------------------------------------------------
  0.2460  N   53.1  N    35.7  N    50.5       51.9       61.9
  0.3840  N   44.0  N    23.2  N    38.6       48.2       58.2
  1.5720  N   44.1  N    22.0  N    39.5       46.0       56.0
  1.6620  N   43.1  N    21.7  N    38.7       46.0       56.0
 24.3680  N   47.4  N    35.2  N    42.7       50.0       60.0
 29.4640  N   47.0  N    34.3  N    42.3       50.0       60.0
```

Figure 15 Conducted emissions at 115 V AC and full load on line (left) and neutral (right)



```
Frequency   Level Pk   Level AV   Level QP   Limit AV   Limit QP
-----------------------------------------------------------------
  0.2400  L   51.5  L    29.5  L    45.4       52.1       62.1
  0.3840  L   44.2  L    26.5  L    39.2       48.2       58.2
  0.7560  L   40.5  L    23.7  L    35.0       46.0       56.0
  1.5660  L   46.5  L    23.3  L    42.1       46.0       56.0
  1.6500  L   43.3  L    22.1  L    38.7       46.0       56.0
 25.4240  L   52.9  L    41.4  L    48.8       50.0       60.0
 29.4880  L   50.3  L    37.5  L    46.1       50.0       60.0
```

```
Frequency   Level Pk   Level AV   Level QP   Limit AV   Limit QP
-----------------------------------------------------------------
  0.1500  N   55.7  N    24.5  N    49.0       56.0       66.0
  0.4920  N   44.1  N    26.1  N    39.4       46.1       56.1
  0.5040  N   44.5  N    26.7  N    39.6       46.0       56.0
  1.5660  N   46.9  N    23.1  N    42.4       46.0       56.0
  1.6500  N   45.0  N    23.7  N    40.6       46.0       56.0
 24.8160  N   49.4  N    36.8  N    44.7       50.0       60.0
 29.5440  N   49.1  N    34.4  N    43.0       50.0       60.0
```

Figure 16 Conducted emissions at 220 V AC and full load on line (left) and neutral (right)

9.9 Thermal measurement

Thermal measurement was done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C taken after one hour running at full load. The temperature of the components was taken in an open-frame set-up.

Table 8 Thermal measurement of components (open-frame)

No.	Components	Temperature at 90 V AC (°C)	Temperature at 264 V AC (°C)
1	D21 (+12 V diode)	64.9	68.1
2	D22 (+20 V diode)	40.3	38.4
3	D12 (+18 V diode)	53.8	51.6
4	TR1 (transformer)	65.0	67.8
5	IC13 (15 V regulator)	74.3	72.5
6	IC11 (ICE5GR2280AG)	86.9	75.8

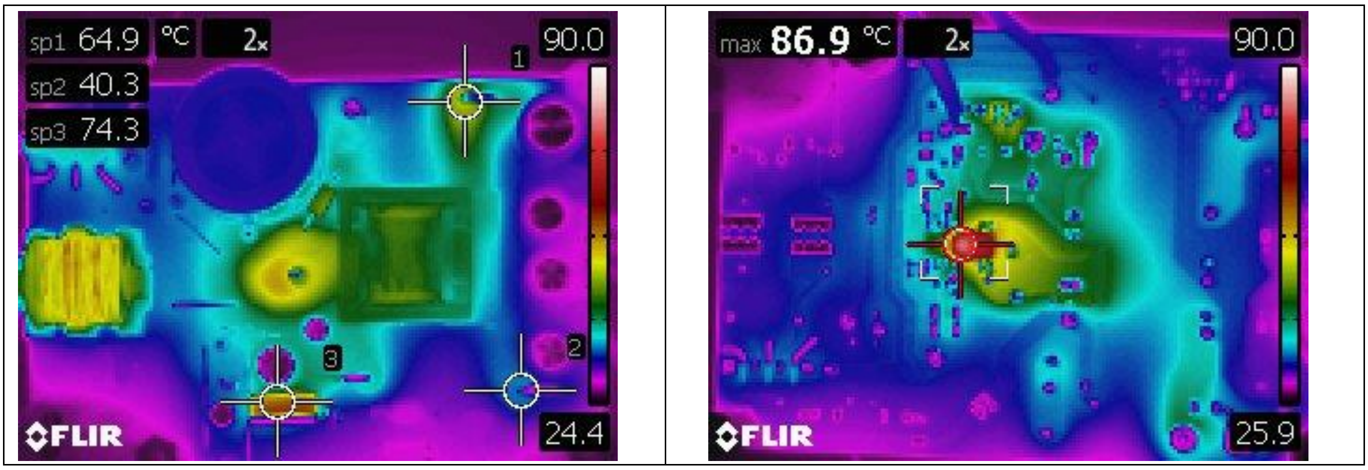


Figure 17 Top layer (left) and bottom layer (right) thermal image at 90 V AC input voltage

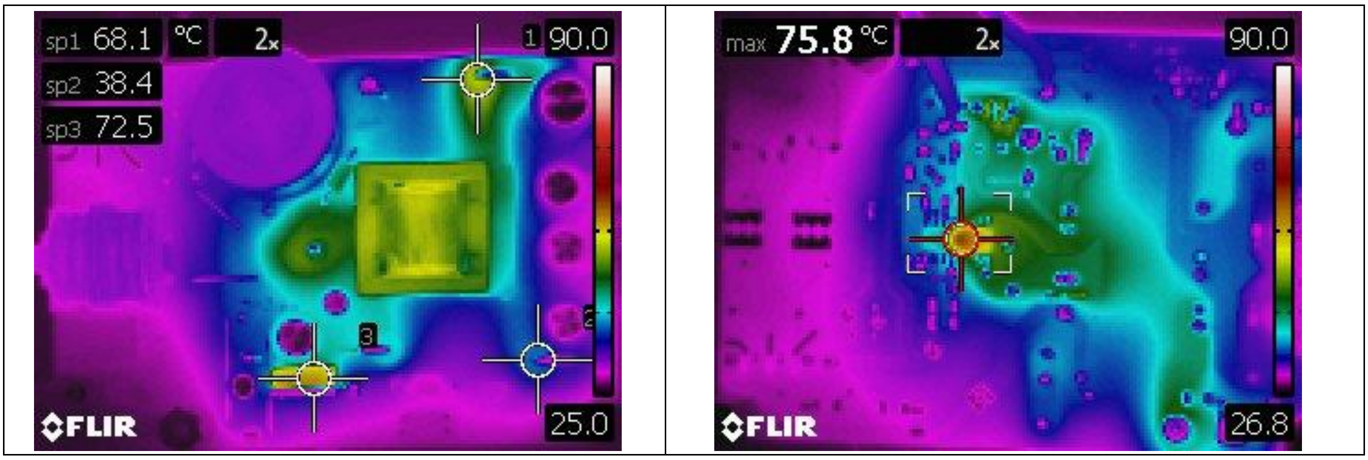


Figure 18 Top layer (left) and bottom layer (right) thermal image at 264 V AC input voltage

9.10 +18 V rail regulation (LDO input)

As the +15 V output via a LDO is derived from the +18 V rail from the transformer which is also shared by the CoolSET™ V_{CC}, there are several design goals to achieve during normal operating conditions:

- Avoid V_{CC} UVLO (10 V typ.)
- Avoid V_{CC} OVP (25.5 V typ.)
- Ensure that the +18 V rail does not exceed the specification of the LDO (V_{in_min}: 15.5 V and V_{in_max}: 26 V)

From the chart and table below, the +18 V rail is operating between 15.89 V and 22.84 V under different load combination and line conditions, which is well within the design objectives outlined above.

Table 9 **+18 V rail line and load regulation**

	12 V/0 A 20 V/0 A 15 V/0 A (V)	12 V/20 mA 20 V/10 mA 15 V/10 mA (V)	12 V/20 mA 20 V/10 mA 15 V/0.2 A (V)	12 V/20 mA 20 V/0.35 A 15 V/10 mA (V)	12 V/1 A 20 V/10 mA 15 V/10 mA (V)	12 V/1 A 20 V/0.35 A 15 V/0.2 A (V)
90 V AC/60 Hz	16.96	17.25	15.89	19.47	22.58	17.81
115 V AC/60 Hz	16.95	17.25	15.85	19.41	22.56	17.81
220 V AC/50 Hz	16.95	17.27	15.92	19.57	22.84	17.79
264 V AC/50 Hz	16.95	17.28	16.09	19.67	22.84	17.79

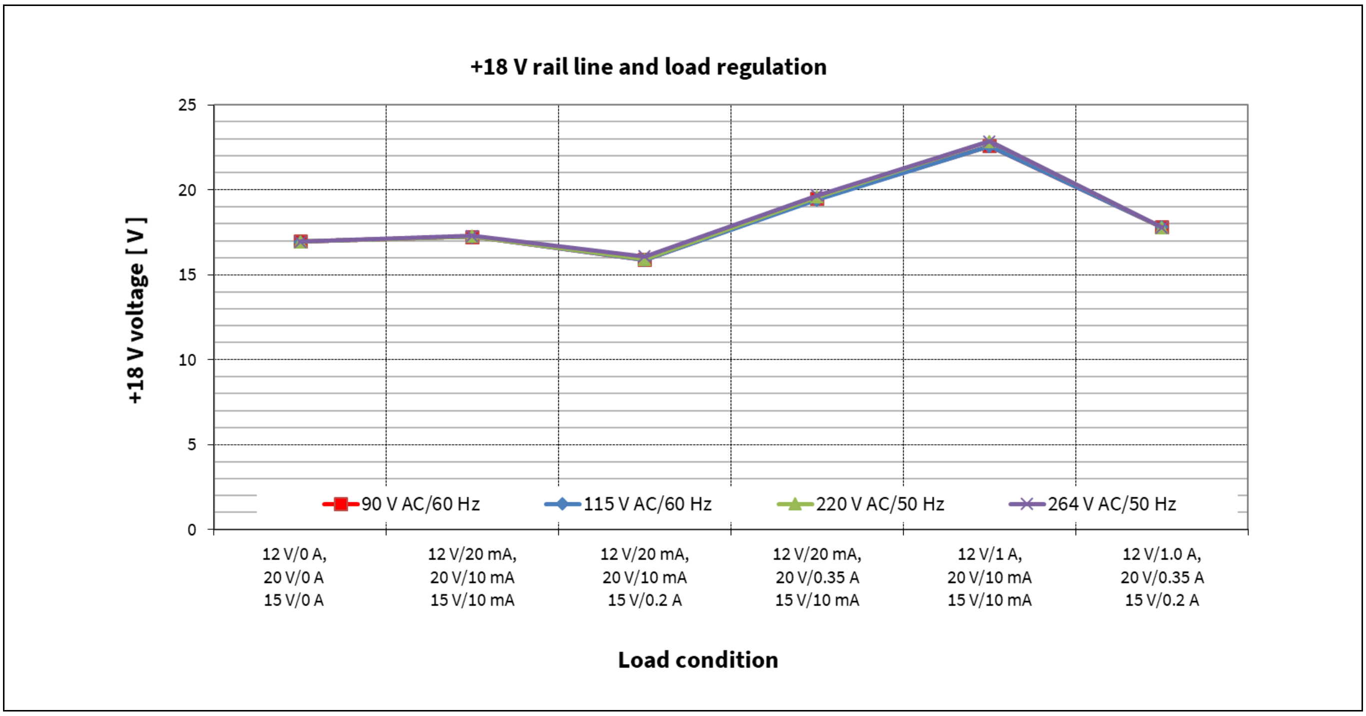


Figure 19 **+18 V rail regulation**

10 Waveforms and oscilloscope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy HDO4034 oscilloscope.

10.1 Start-up at full load

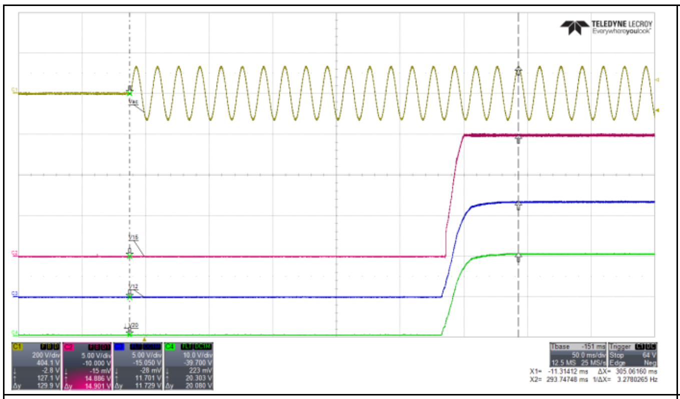
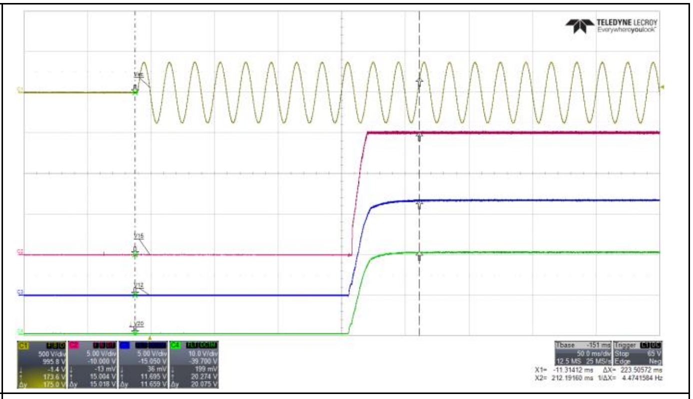
	
C1 (yellow) : AC-line voltage C2 (purple) : +15 V output voltage C3 (blue) : +12 V output voltage C4 (green) : +20 V output voltage	C1 (yellow) : AC-line voltage C2 (purple) : +15 V output voltage C3 (blue) : +12 V output voltage C4 (green) : +20 V output voltage
90 V AC start-up time at full load is less than 305 ms	264 V AC start-up time at full load is less than 230 ms

Figure 20 **Start-up**

10.2 Soft-start at full load

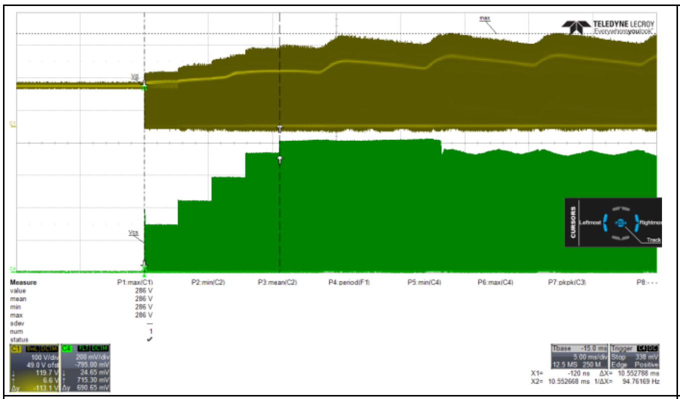
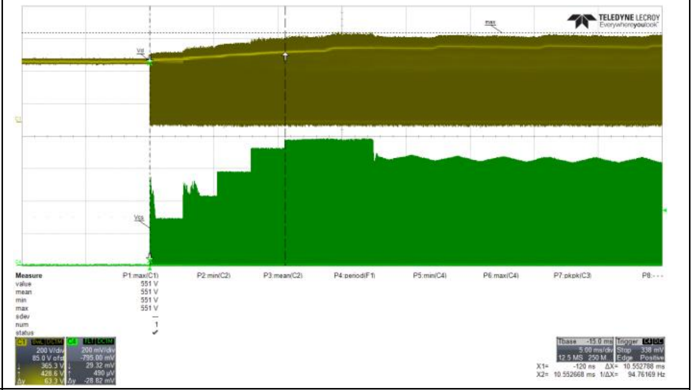
	
C1 (yellow) : Drain voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C4 (green) : CS voltage
90 V AC soft-start at full load within ~11 ms	264 V AC soft-start time at full load within ~11 ms

Figure 21 **Soft-start**

10.3 Drain and CS voltage at full load

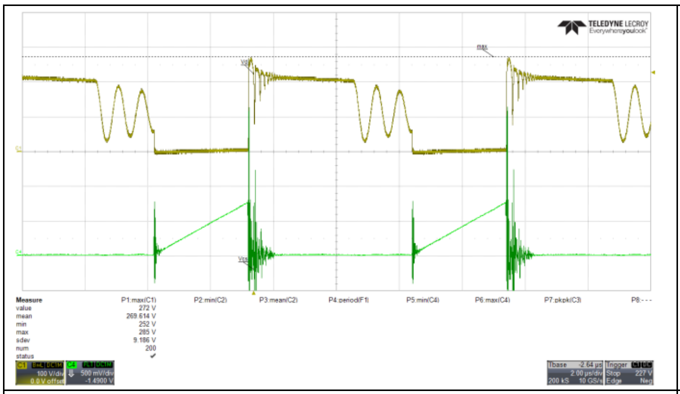
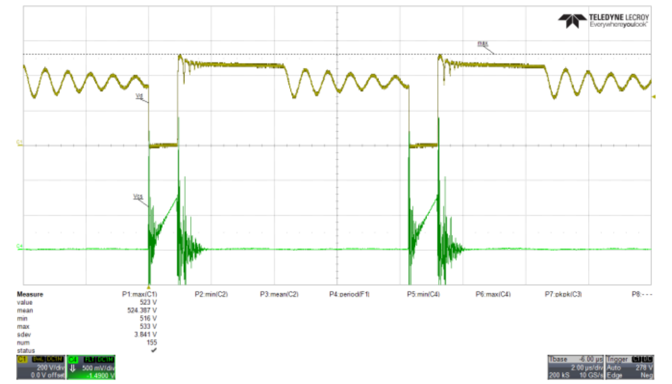
	
C1 (yellow) : Drain voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C4 (green) : CS voltage
90 V AC maximum drain voltage at full load is ~272 V	264 V AC maximum drain voltage at full load is ~530 V

Figure 22 Drain and CS voltage

10.4 Frequency jittering and modulated gate drive at full load

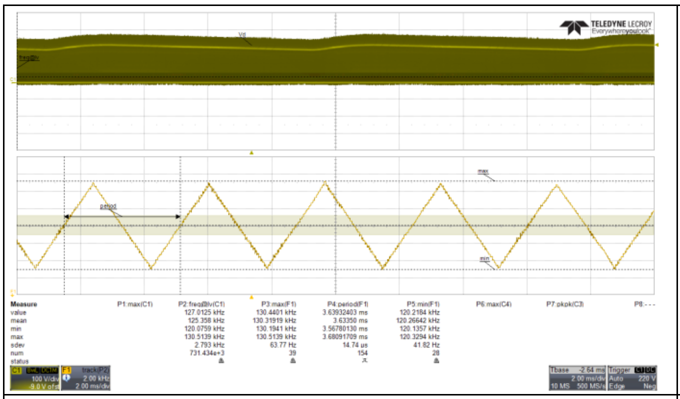
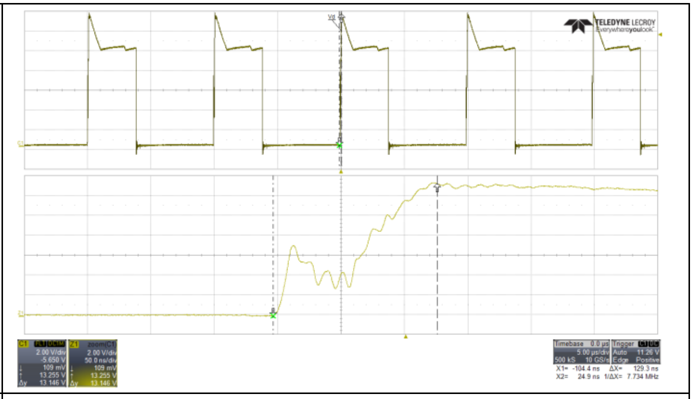
	
C1 (yellow) : Drain voltage F1 (yellow) : Frequency track of drain voltage	C1 (yellow) : Gate voltage
90 V AC frequency jittering at full load is ~120 kHz to ~130 kHz with jitter period of 3.6 ms	90 V AC modulated gate drive at ~120 ns rise time

Figure 23 Frequency jittering and modulated gate drive

10.5 Load transient response (dynamic load from minimum to full load)

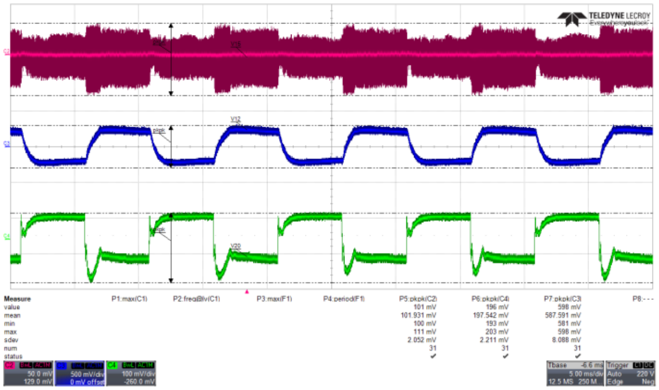
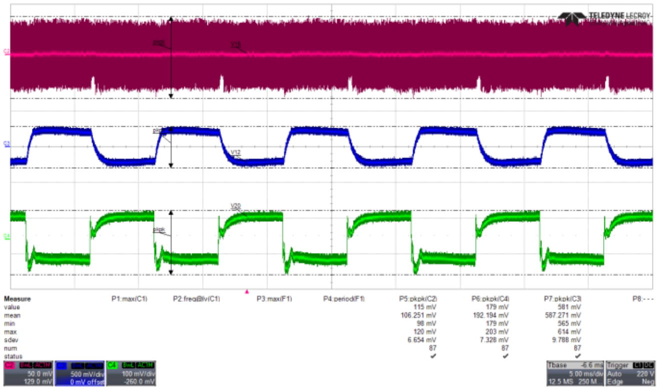
	
C2 (purple) : +15 V output voltage C3 (blue) : +12 V output voltage C4 (green) : +20 V output voltage	C2 (purple) : +15 V output voltage C3 (blue) : +12 V output voltage C4 (green) : +20 V output voltage
90 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~588 mV and +15 V output voltage $V_{ripple\_pk\_pk}$ is ~102 mV and +20 V output voltage $V_{ripple\_pk\_pk}$ is ~198 mV	264 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~587 mV, +15 V output voltage $V_{ripple\_pk\_pk}$ is ~106 mV and +20 V output voltage $V_{ripple\_pk\_pk}$ is ~192 mV

Figure 24 **Load transient response with +12 V output load change from minimum (20 mA) to full load (1 A) at 0.4 A/µs slew rate, 100 Hz. +15 V output load is fixed at 0.2 A and +20 V output load is fixed at 0.35 A. Probe terminals are decoupled with 1 µF electrolytic and 0.1 µF ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz.**

10.6 Output ripple voltage at full load

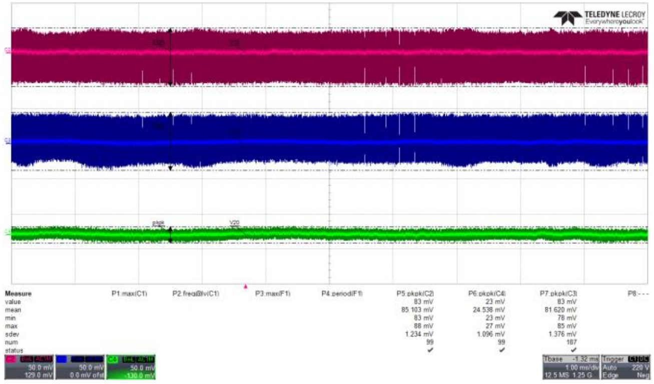
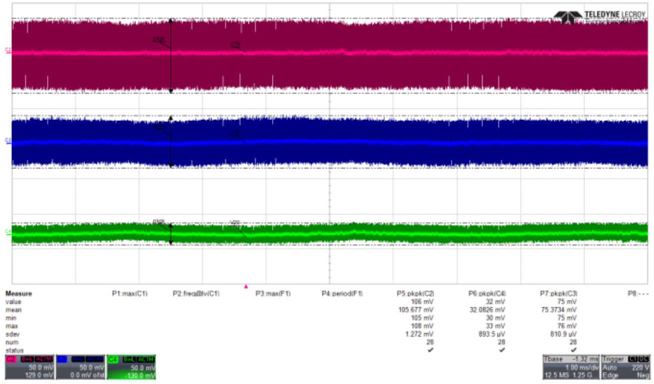
	
C2 (purple) : +15 V output voltage C3 (blue) : +12 V output voltage C4 (green) : +20 V output voltage	C2 (purple) : +15 V output voltage C3 (blue) : +12 V output voltage C4 (green) : +20 V output voltage
90 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~82 mV and +15 V output voltage $V_{ripple\_pk\_pk}$ is ~85 mV and +20 V output voltage $V_{ripple\_pk\_pk}$ is ~24 mV	264 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~75 mV, +15 V output voltage $V_{ripple\_pk\_pk}$ is ~105 mV and +20 V output voltage $V_{ripple\_pk\_pk}$ is ~32 mV

Figure 25 **Output ripple voltage at full load. Probe terminals are decoupled with 1 µF electrolytic and 0.1 µF ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz.**

10.7 Output ripple voltage at ABM (minimum load)

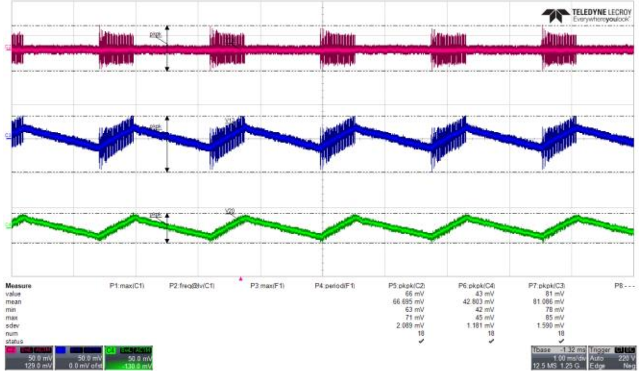
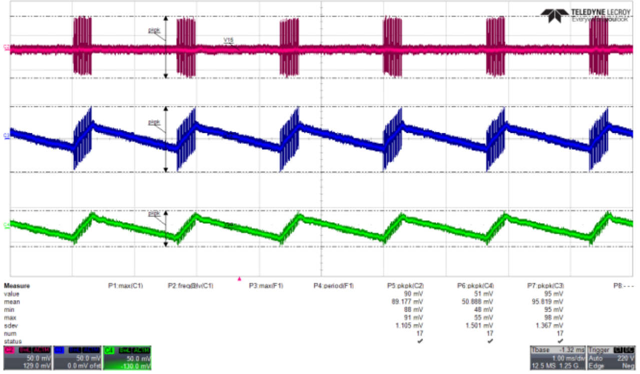
	
C2 (purple) : +15 V output voltage C3 (blue) : +12 V output voltage C4 (green) : +20 V output voltage	C2 (purple) : +15 V output voltage C3 (blue) : +12 V output voltage C4 (green) : +20 V output voltage
90 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~81 mV and +15 V output voltage $V_{ripple\_pk\_pk}$ is ~67 mV and +20 V output voltage $V_{ripple\_pk\_pk}$ is ~43 mV	264 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~95 mV, +15 V output voltage $V_{ripple\_pk\_pk}$ is ~89 mV and +20 V output voltage $V_{ripple\_pk\_pk}$ is ~51 mV

Figure 26 **Output ripple voltage at minimum load. Probe terminals are decoupled with 1 µF electrolytic and 0.1 µF ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz.**

10.8 Entering ABM

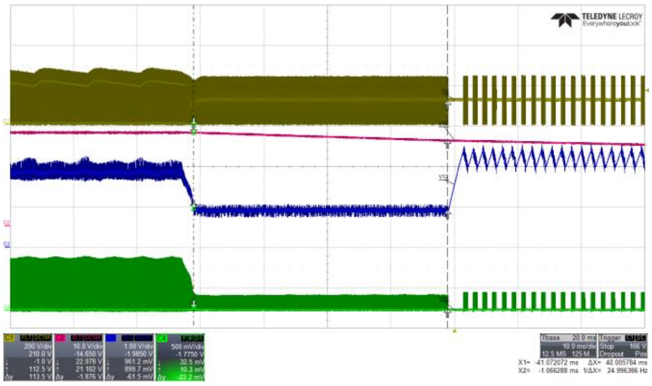
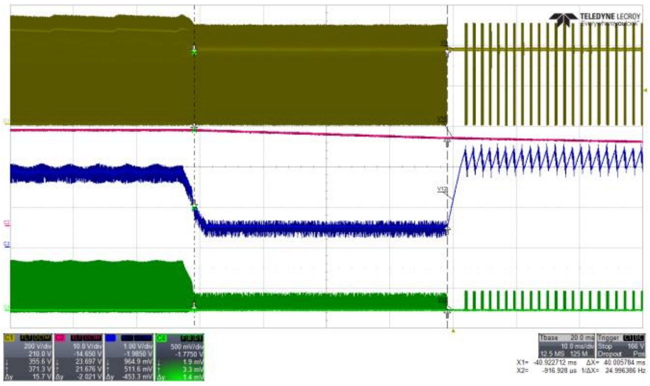
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
90 V AC enters ABM at FB pin voltage less than 0.93 V (V_{FB_EBLP}) for more than 36 ms (t_{FB_BEB})	264 V AC enters ABM at FB pin voltage less than 10.93 V (V_{FB_EBLP}) for more than 36 ms (t_{FB_BEB})

Figure 27 **Entering ABM. +12 V output load from 1 A to 20 mA load. Both +15 V and +20 V outputs have 10 mA fixed load.**

10.9 During ABM

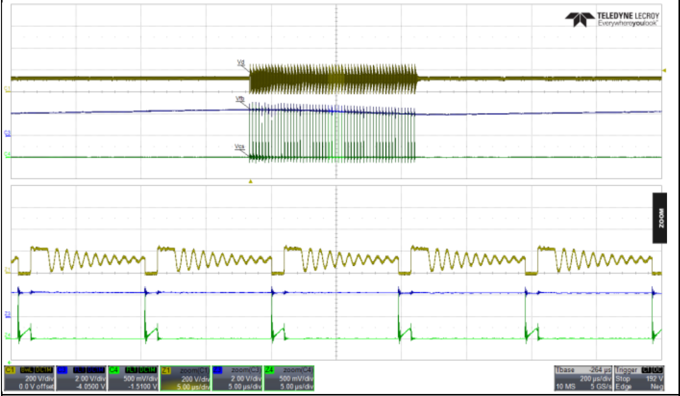
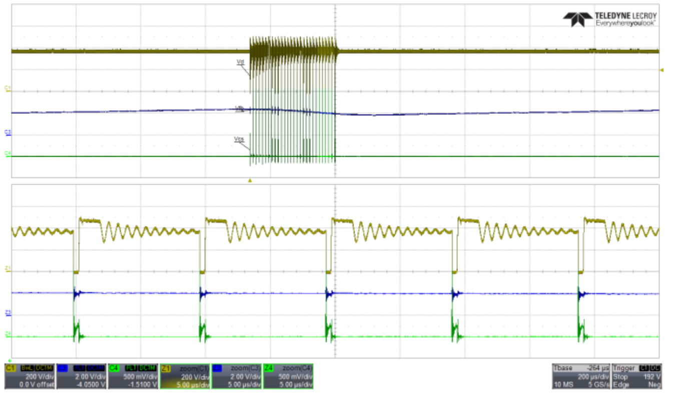
	
C1 (yellow) : Drain voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
90 V AC ABM. Burst-on at FB voltage 2.35 V ($V_{FB\_Bon\_ISO}$) and burst-off at 2 V ($V_{FB\_BOff\_ISO}$). CS voltage at 0.22 V (V_{CS_BLP}). Switching frequency at 103 kHz (f_{OSC4_ABM}).	264 V AC ABM. Burst-on at FB voltage 2.35 V ($V_{FB\_Bon\_ISO}$) and burst-off at 2 V ($V_{FB\_BOff\_ISO}$). CS voltage at 0.22 V (V_{CS_BLP}). Switching frequency at 103 kHz (f_{OSC4_ABM}).

Figure 28 **During ABM. Output at minimum load.**

10.10 Leaving ABM

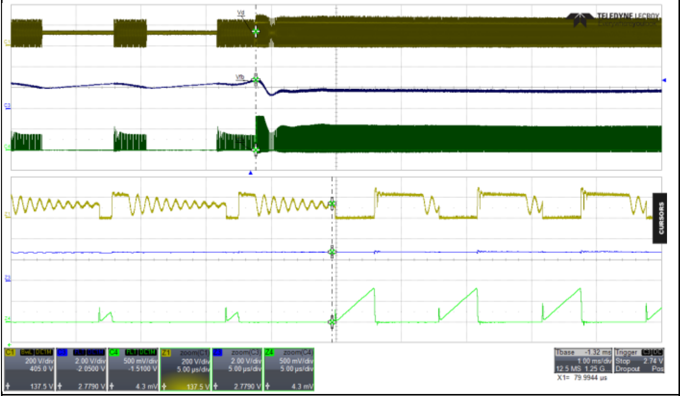
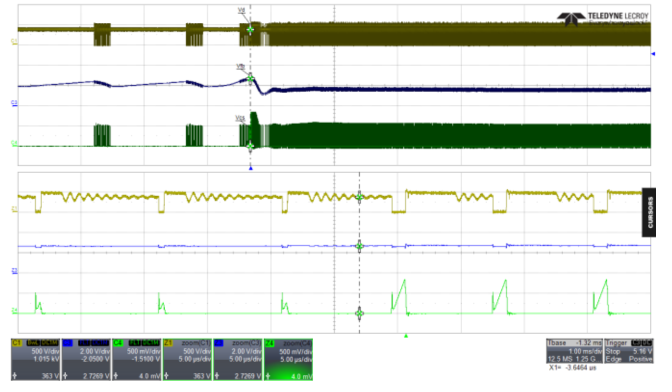
	
C1 (yellow) : Drain voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
90 V AC leaves ABM at FB voltage higher than 2.73 V (V_{FB_LB})	264 V AC leaves ABM at FB voltage higher than 2.73 V (V_{FB_LB})

Figure 29 **Leaving ABM. +12 V output load from 20 mA to 1 A load. Both +15 V and +20 V outputs have 10 mA fixed load.**

10.11 V_{CC} OV/UV protection

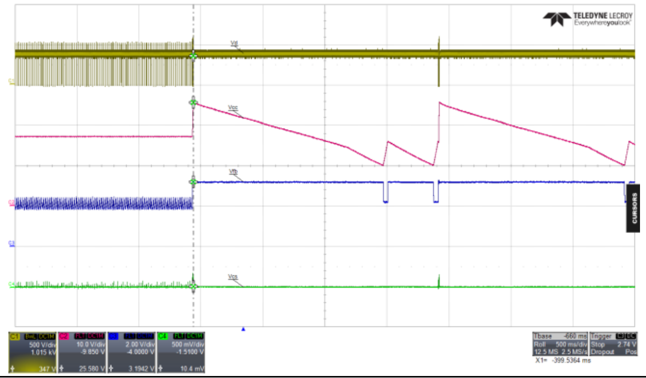
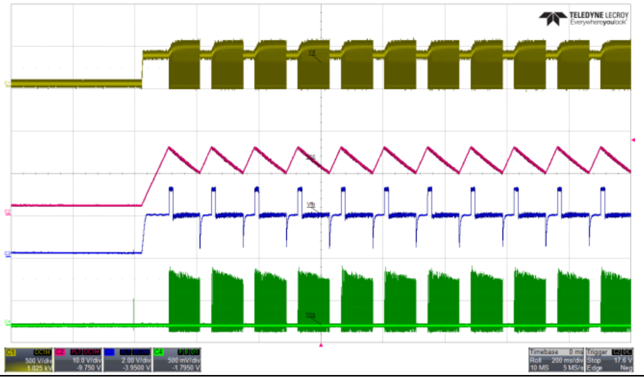
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
264 V AC at no load. Trigger V_{CC} OVP at V_{CC} voltage greater than 25.5 V (V_{VCC_OVP}). Odd-skip auto-restart mode. Short R26.	264 V AC at full load. Trigger V_{CC} UVP at V_{CC} voltage less than 10 V (V_{VCC_OFF}). Auto-restart mode. Open D12A.

Figure 30 V_{CC} OV/UV protection

10.12 Over-load protection

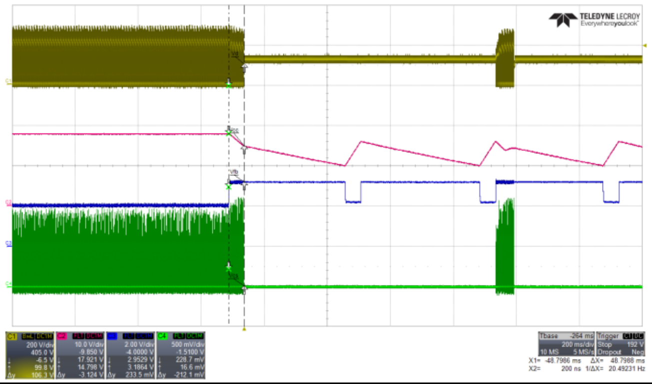
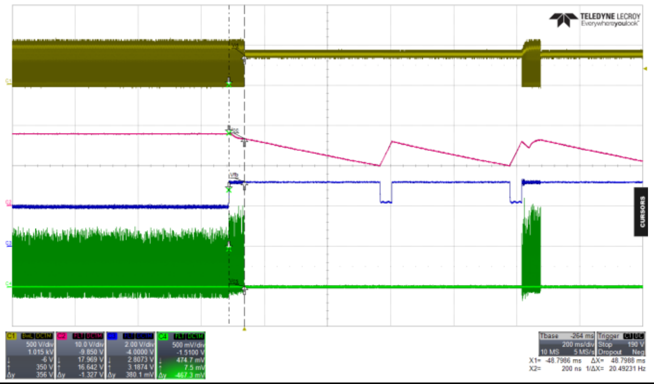
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
90 V AC at full load to over-load. Trigger protection at FB pin voltage greater than 2.73 V (V_{FB_OLP}) for more than 54 ms ($t_{FB\_OLP\_B}$). Odd-skip auto-restart mode.	264 V AC at full load to over-load. Trigger protection at FB pin voltage greater than 2.73 V (V_{FB_OLP}) for more than 54 ms ($t_{FB\_OLP\_B}$). Odd-skip auto-restart mode.

Figure 31 **Over-load protection. Load increased at +12 V output from 1 A to 2 A load to trigger protection. +15 V output has 0.2 A and +20 V output has 0.35 A fixed load.**

10.13 Brown-in and LOVP

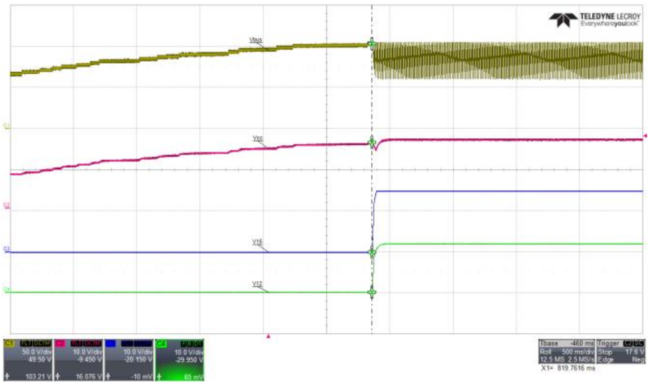
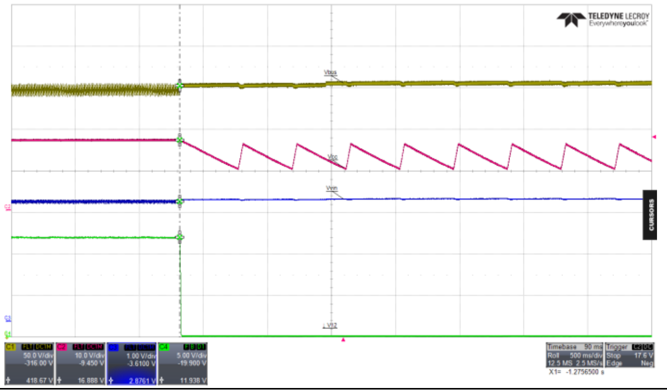
	
C1 (yellow) : Bus voltage C2 (purple) : V_{CC} voltage C3 (blue) : +15 V output voltage C4 (green) : +12 V output voltage	C1 (yellow) : Bus voltage C2 (purple) : V_{CC} voltage C3 (blue) : VIN pin voltage C4 (green) : +12 V output voltage
Turn-on at 103 V bus voltage (74 V AC)	Trigger LOVP at (419 V bus voltage/298 V AC), VIN pin voltage greater than 2.85 V (V_{VIN_LOVP}). Non-switch auto-restart mode.

Figure 32 Brown-in and LOVP

11 Appendix A: Transformer design and spreadsheet [3]

Calculation tool for FF Flyback converter using fifth-generation CoolSET™ (Version 1.0)

Project:	REF_5GR2280AG_22W1
Application:	AUX for commercial air-conditioner unit
CoolSET™:	ICE5GR2280AG
Date:	23 February 2019
Revision:	V 0.0

Notes:

Enter design variables in orange coloured cells

Read design results in green coloured cells

Equation numbers are according to the design guide

Select component values based on standard values available

Voltage/current rating does not include design margin, voltage spikes and transient currents

In “Output regulation”, only fill in either isolated or non-isolated, whichever is applicable

Input, output, CoolSET™ specs

Line input

	Description	Eq. #	Parameter	Unit	Value
Input	Minimum AC input voltage		V_{ACMin}	[V]	90
Input	Maximum AC input voltage		V_{ACMax}	[V]	264
Input	Line frequency		f_{AC}	[Hz]	60
Input	Bus capacitor DC ripple voltage		$V_{DCRipple}$	[V]	36

Output 1 specs

	Description	Eq. #	Parameter	Unit	Value
Input	Output voltage 1		V_{Out1}	[V]	12
Input	Output current 1		I_{Out1}	[A]	1
Input	Forward voltage of output diode 1		V_{FOut1}	[V]	0.6
Input	Output ripple voltage 1		$V_{OutRipple1}$	[V]	0.3
Result	Output power 1	Eq 001	P_{Out1}	[W]	12
Result	Output load weight 1	Eq 004	K_{L1}		0.55

Output 2 specs

	Description	Eq. #	Parameter	Unit	Value
Input	Output voltage 2		V_{Out2}	[V]	20
Input	Output current 2		I_{Out2}	[A]	0.5
Input	Forward voltage of output diode 2		V_{FOut2}	[V]	0.6
Input	Output ripple voltage 2		$V_{OutRipple2}$	[V]	0.2
Result	Output power 2	Eq 002	P_{Out2}	[W]	10
Result	Output load weight 2	Eq 005	K_{L2}		0.45

Auxiliary

	Description	Eq. #	Parameter	Unit	Value
Input	V_{CC} voltage		V_{Vcc}	[V]	18
Input	Forward voltage of V_{CC} diode (D2)		$V_{F\,Vcc}$	[V]	0.6

Power

	Description	Eq. #	Parameter	Unit	Value
Input	Efficiency		η		0.8
Result	Nominal output power	Eq 003	P_{OutNom}	[W]	22.00
Input	Maximum output power for over-load protection		P_{OutMax}	[W]	27
Result	Maximum input power for over-load protection	Eq 006	P_{InMax}	[W]	33.88
Input	Minimum output power		P_{OutMin}	[W]	2.2

Controller/CoolSET™

	Controller/CoolSET™				ICE5GR2280AG
Input	Switching frequency		f_S	[Hz]	125000
Input	Targeted max. drain source voltage		V_{DSMax}	[V]	600
Input	Max. ambient temperature		T_{amax}	[°C]	50

Diode bridge and input capacitor

Diode bridge

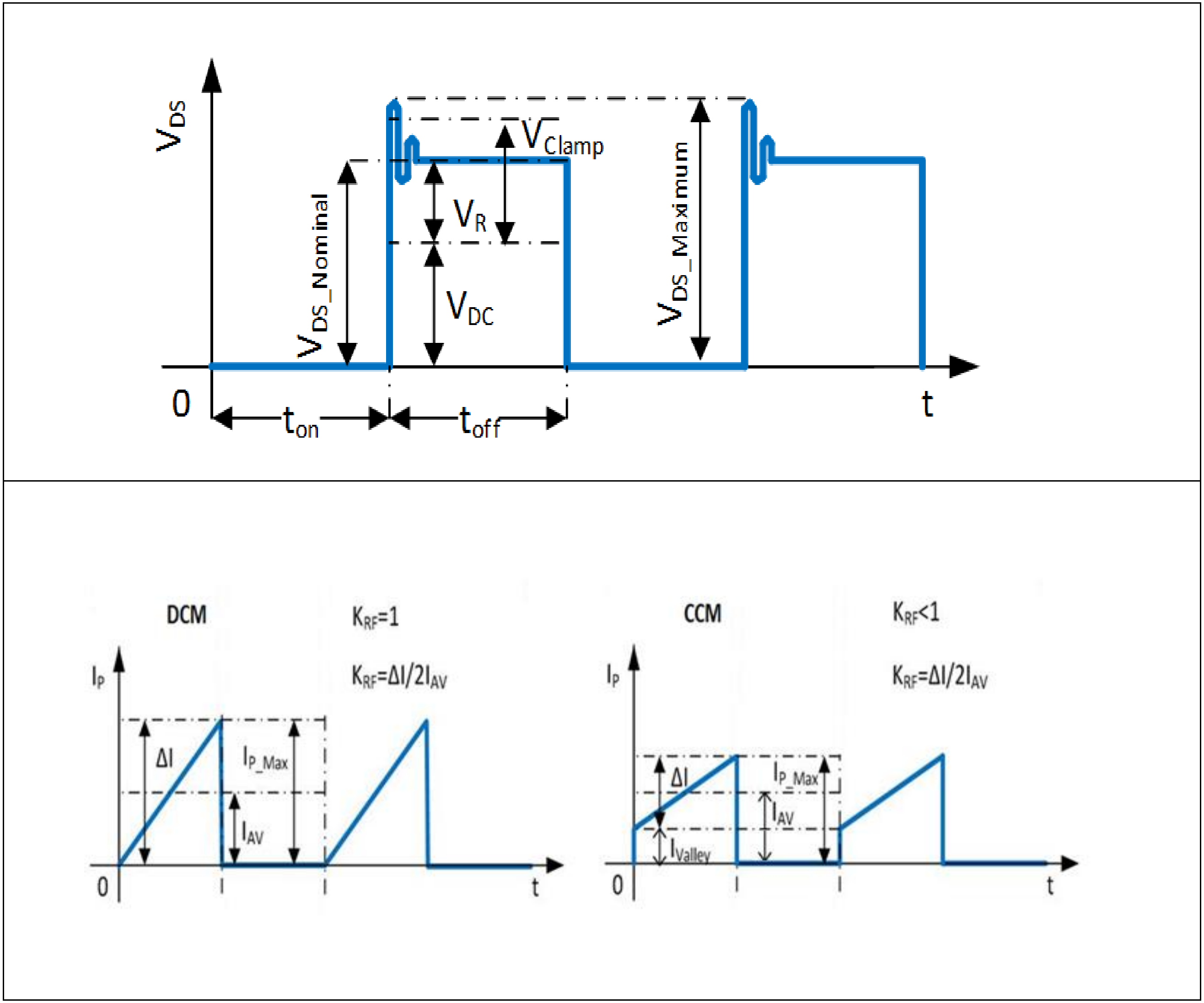
Input	Power factor		cosφ		0.6
Result	Maximum AC input current	Eq 007	I_{ACRMS}	[A]	0.627
Result	Peak voltage at V_{ACMax}	Eq 008	$V_{DCMaxPk}$	[V]	373.35

Input capacitor

Result	Peak voltage at V_{ACMin}	Eq 009	$V_{DCMinPk}$	[V]	127.28
Result	Selected minimum DC input voltage	Eq 010	$V_{DCMinSet}$	[V]	92.68
Result	Discharging time at each half-line cycle	Eq 011	T_D	[ms]	6.33
Result	Required energy at discharging time of input capacitor	Eq 012	W_{In}	[Ws]	0.21
Result	Calculated input capacitor	Eq 013	C_{INCal}	[µF]	56.35
Input	Select input capacitor (C1)		C_{in}	[µF]	56
Result	Calculated minimum DC input voltage	Eq 015	V_{DCMin}	[V]	92.42

Transformer design

Drain voltage and current waveform



Primary inductance and winding currents

Input	Reflection voltage		V_{RSET}	[V]	100.8
Result	Maximum duty cycle	Eq 016	D_{Max}		0.52
Input	Select current ripple factor		K_{RF}		1
Result	Primary inductance	Eq 017	L_P	[H]	2.74E-04
Result	Primary turn-on average current	Eq 018	I_{AV}	[A]	0.70
Result	Primary peak-to-peak current	Eq 019	ΔI	[A]	1.41
Result	Primary peak current	Eq 020	I_{PMax}	[A]	1.41
Result	Primary valley current	Eq 021	I_{Valley}	[A]	0.00
Result	Primary RMS current	Eq 022	I_{PRMS}	[A]	0.586

Select core type

Input	Select core type				1
Result	Core type				EE20/10/6
Result	Core material				TP4A (TDG)
Result	Maximum flux density		B_{Max}	[T]	0.255
Result	Cross-sectional area		A_e	[mm^2]	32
Result	Bobbin width		BW	[mm]	11
Result	Winding cross-section		A_N	[mm^2]	34
Result	Average length of turn		l_N	[mm]	41.2

Winding calculation

Result	Calculated minimum number of primary turns	Eq 023	N_{PCal}	Turns	42.27
Input	Select number of primary turns		N_P	Turns	48
Result	Calculated number of secondary 1 turns	Eq 024	N_{S1Cal}	Turns	6.00
Input	Select number of secondary 1 turns		N_{S1}	Turns	6
Result	Calculated number of secondary 2 turns	Eq 025	N_{S2Cal}	Turns	9.81
Input	Select number of secondary 2 turns		N_{S2}	Turns	10
Result	Calculated number of auxiliary turns	Eq 026	N_{VccCal}	Turns	8.86
Input	Select number of auxiliary turns		N_{Vcc}	Turns	19
Result	Calculated V_{CC} voltage	Eq 027	V_{VccCal}	[V]	18.30

Post calculation

Result	Primary to secondary 1 turns ratio	Eq 028	N_{PS1}		8.00
Result	Primary to secondary 2 turns ratio	Eq 029	N_{PS2}		4.80
Result	Post-calculated reflected voltage	Eq 030	V_{RPost}	[V]	100.80
Result	Post-calculated maximum duty cycle	Eq 031	$D_{MaxPost}$		0.52
Result	Duty cycle prime	Eq 032	D_{Max}'		0.48
Result	Actual flux density	Eq 033	B_{MaxAct}	[T]	0.251
Result	Maximum DC input voltage for CCM operation	Eq 034	$V_{DCmaxCCM}$	[V]	92.42

Transformer winding design

Input	Margin according to safety standard		M	[mm]	0
Input	Copper space factor		f_{Cu}		0.4
Result	Effective bobbin window	Eq 035	BW_E	[mm]	11.0
Result	Effective winding cross-section	Eq 036	A_{Ne}	[mm^2]	34.0
Input	Primary winding area factor		AF_{NP}		0.50
Input	Secondary 1 winding area factor		AF_{NS1}		0.30
Input	Secondary 2 winding area factor		AF_{NS2}		0.15
Input	Auxiliary winding area factor		AF_{NVcc}		0.05

Primary winding

Result	Calculated copper wire cross-sectional area	Eq 037	A_{PCal}	[mm^2]	0.1417
Result	Calculated maximum wire size	Eq 038	AWG_{PCal}		26
Input	Select wire size		AWG_P		26
Input	Select number of parallel wire		nw_P		1
Result	Copper wire diameter	Eq 039	d_P	[mm]	0.41
Result	Copper wire cross-sectional area	Eq 040	A_P	[mm^2]	0.1303
Result	Wire current density	Eq 041	S_P	[A/mm^2]	4.50
Input	Insulation thickness		INS_P	[mm]	0.01
Result	Turns per layer	Eq 042	NL_P	Turns/layer	25
Result	Number of layers	Eq 043	Ln_P	Layers	2

Secondary 1 winding

Result	Calculated copper wire cross-sectional area	Eq 044	A_{NS1Cal}	[mm^2]	0.6800
Result	Calculated maximum wire size	Eq 045	AWG_{S1Cal}		19
Input	Select wire size		AWG_{S1}		31
Input	Select number of parallel wires		nw_{S1}		7
Result	Copper wire diameter	Eq 046	d_{S1}	[mm]	0.2287
Result	Copper wire cross-sectional area	Eq 047	A_{S1}	[mm^2]	0.2874
Result	Peak current	Eq 048	I_{S1Max}	[A]	5.4601
Result	RMS current	Eq 049	I_{S1RMS}	[A]	2.1307
Result	Wire current density	Eq 050	S_{S1}	[A/mm^2]	7.41
Input	Insulation thickness		INS_{S1}	[mm]	0.01
Result	Turns per layer	Eq 051	NL_{S1}	Turns/layer	6
Result	Number of layers	Eq 052	Ln_{S1}	Layers	1

Secondary 2 winding

Result	Calculated copper wire cross-sectional area	Eq 053	A_{NS2Cal}	[mm^2]	0.2040
Result	Calculated maximum wire size	Eq 054	AWG_{S2Cal}		24
Input	Select wire size		AWG_{S2}		31
Input	Select number of parallel wires		nw_{S2}		7
Result	Copper wire diameter	Eq 055	d_{S2}	[mm]	0.2287
Result	Copper wire cross-sectional area	Eq 056	A_{S2}	[mm^2]	0.2874
Result	Peak current	Eq 057	I_{S2Max}	[A]	3.0659
Result	RMS current	Eq 058	I_{S2RMS}	[A]	1.2242
Result	Wire current density	Eq 059	S_{S2}	[A/mm^2]	4.26
Input	Insulation thickness		INS_{S2}	[mm]	0.01
Result	Turns per layer	Eq 060	NL_{S2}	Turns/layer	6
Result	Number of layers	Eq 061	Ln_{S2}	Layers	2

RCD clamper and CS resistor

RCD clamper circuit

Input	Leakage inductance percentage		$L_{LK\%}$	[%]	0.26
Result	Leakage inductance	Eq 062	L_{LK}	[H]	7.11E-06
Result	Clamping voltage	Eq 063	V_{Clamp}	[V]	125.85
Result	Calculated clamping capacitor	Eq 064	$C_{ClampCal}$	[nF]	0.05
Input	Select clamping capacitor value (C2)		C_{clamp}	[nF]	1
Result	Calculated clamping resistor	Eq 065	$R_{clampCal}$	[kΩ]	470
Input	Select clamping resistor value (R4)		R_{clamp}	[kΩ]	470

CS resistor

Input	CS threshold value from datasheet		V_{CS_N}	[V]	0.8
Result	Calculated current sense resistor (R8A, R8B)	Eq 066	R_{sense}	[Ω]	0.57

Output rectifier

Secondary 1 Output rectifier

Result	Diode reverse voltage	Eq 067	$V_{RDiode1}$	[V]	58.67
Result	Diode RMS current		$I_{S\,1RMS}$	[A]	2.45
Input	Max. voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.3
Input	Number of clock periods		n_{cp1}		20
Result	Output capacitor ripple current	Eq 068	$I_{Ripple1}$	[A]	2.23
Result	Calculated minimum output capacitor	Eq 069	$C_{Out1Cal}$	[µF]	533
Input	Select output capacitor value (C152)		C_{Out1}	[µF]	820
Input	ESR (Z_{max}) value from datasheet at 100 kHz		R_{ESR1}	[Ω]	0.041
Input	Number of parallel capacitors		nc_{COut1}		1
Result	Zero frequency of output capacitor	Eq 070	f_{ZCOut1}	[kHz]	4.73
Result	First-stage ripple voltage	Eq 071	$V_{Ripple1}$	[V]	0.251400
Input	Select LC filter inductor value (L151)		L_{out1}	[µH]	4.7
Result	Calculated LC filter capacitor	Eq 072	C_{LCCal1}	[µF]	240.5
Input	Select LC filter capacitor value (C153)		C_{LC1}	[µF]	220
Result	LC filter frequency	Eq 073	f_{LC1}	[kHz]	4.95
Result	Second-stage ripple voltage	Eq 074	$V_{2ndRipple1}$	[mV]	0.55

Secondary 2 Output rectifier

Result	Diode reverse voltage	Eq 075	$V_{RDiode2}$	[V]	97.78
Result	Diode RMS current		I_{S2RMS}	[A]	1.22
Input	Max. voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.365
Input	Number of clock periods		n_{cp2}		20
Result	Output capacitor ripple current	Eq 076	$I_{Ripple2}$	[A]	1.12
Result	Calculated minimum output capacitor	Eq 077	$C_{Out2Cal}$	[µF]	219
Input	Select output capacitor value (C152)		C_{Out2}	[µF]	220
Input	ESR (Z_{max}) value from datasheet at 100 kHz		R_{ESR2}	[Ω]	0.15
Input	Number of parallel capacitors		nc_{COut2}		1
Result	Zero frequency of output capacitor	Eq 078	f_{ZCOut2}	[kHz]	4.82
Result	First-stage ripple voltage	Eq 079	$V_{Ripple2}$	[V]	0.46
Input	Select LC filter inductor value (L151)		L_{out2}	[µH]	4.7
Result	Calculated LC filter capacitor	Eq 080	C_{LCCal2}	[µF]	231.7
Input	Select LC filter capacitor value (C153)		C_{LC2}	[µF]	220
Result	LC filter frequency	Eq 081	f_{LC2}	[kHz]	4.95
Result	Second-stage ripple voltage	Eq 082	$V_{2ndRipple2}$	[mV]	0.72

V_{CC} diode and capacitor

V_{CC} diode and capacitor

Result	Auxiliary diode reverse voltage (D2)	Eq 083	$V_{RDiodeVCC}$	[V]	88.3
Input	Soft-start time from datasheet		t_{ss}	[ms]	12
Input	$I_{VCC,Charge3}$ from datasheet		$I_{VCC\_Charge3}$	[mA]	3
Input	V_{CC} on-threshold		V_{VCC_ON}	[V]	16
Input	V_{CC} off-threshold		V_{VCC_OFF}	[V]	10
Result	Calculated V_{CC} capacitor	Eq 084	C_{VCCCal}	[µF]	6.00
Input	Select V_{CC} capacitor (C3)		C_{VCC}	[µF]	22
Input	V_{CC} short threshold from datasheet		V_{VCC_SCP}	[V]	1.1
Input	$I_{VCC\_Charge1}$ from datasheet		$I_{VCC\_Charge1}$	[mA]	0.2
Result	Start-up time	Eq 085	$t_{StartUp}$	[ms]	230.267

Calculation of losses

Input diode bridge

Input	Diode bridge forward voltage		V_{FBR}	[V]	1
Result	Diode bridge power loss	Eq 086	P_{DIN}	[W]	1.25

Transformer copper

Result	Primary winding copper resistance	Eq 087	R_{PCu}	[mΩ]	261.04
Result	Secondary 1 winding copper resistance	Eq 088	R_{S1Cu}	[mΩ]	14.79
Result	Secondary 2 winding copper resistance	Eq 089	R_{S2Cu}	[mΩ]	24.65
Result	Primary winding copper loss	Eq 090	P_{PCu}	[mW]	89.63
Result	Secondary 1 winding copper loss	Eq 091	P_{S1Cu}	[mW]	88.67
Result	Secondary 2 winding copper loss	Eq 092	P_{S2Cu}	[mW]	36.95
Result	Total transformer copper loss	Eq 093	P_{Cu}	[W]	0.2152

Output rectifier diode

Result	Secondary 1 diode loss	Eq 094	P_{Diode1}	[W]	1.47
Result	Secondary 2 diode loss	Eq 095	P_{Diode2}	[W]	0.73

RCD clamper circuit

Result	RCD clamper loss	Eq 096	$P_{Clamper}$	[W]	0.16

Current sense resistor

Result	CS resistor loss	Eq 097	P_{CS}	[W]	0.20

MOSFET

Input	$R_{DS(on)}$ from datasheet		$R_{DS(on)}$ at T_A = 125°C	[Ω]	4.31
Input	$C_{o(er)}$ from datasheet		$C_{o(er)}$	[pF]	7
Input	External drain-to-source capacitance		C_{DS}	[pF]	0
Result	Switch-on loss at minimum AC input voltage	Eq 098	$P_{SONMinAC}$	[W]	0.0163
Result	Conduction loss at minimum AC input voltage	Eq 099	$P_{condMinAC}$	[W]	1.4799
Result	Total MOSFET loss at minimum AC input voltage	Eq 100	$P_{MOSMinAC}$	[W]	1.4962
Result	Switch-on loss at maximum AC input voltage	Eq 101	$P_{SONMaxAC}$	[W]	0.0984
Result	Conduction loss at maximum AC input voltage	Eq 102	$P_{condMaxAC}$	[W]	0.3663
Result	Total MOSFET loss at maximum AC input voltage	Eq 103	$P_{MOSMaxAC}$	[W]	0.4647
Result	Total MOSFET loss (from minimum or maximum AC)		P_{MOS}	[W]	1.4962

Controller

Input	Controller current consumption		I_{VCC_Normal}	[mA]	0.9
Result	Controller loss	Eq 104	P_{Ctrl}	[W]	0.0165

Efficiency after losses

Result	Total power loss	Eq 105	P_{Losses}	[W]	5.54
Result	Post calculated efficiency	Eq 106	η_{Post}	%	83.03 percent

CoolSET™/MOSFET temperature

CoolSET™/MOSFET temperature

Input	Enter thermal resistance junction-ambient (include copper pour)		R_{thJA_As}	[°K/W]	50.0
Result	Temperature rise	Eq 107	ΔT	[°K]	74.8
Result	Junction temperature at T_{amax}	Eq 108	Tjmax	°C	124.8

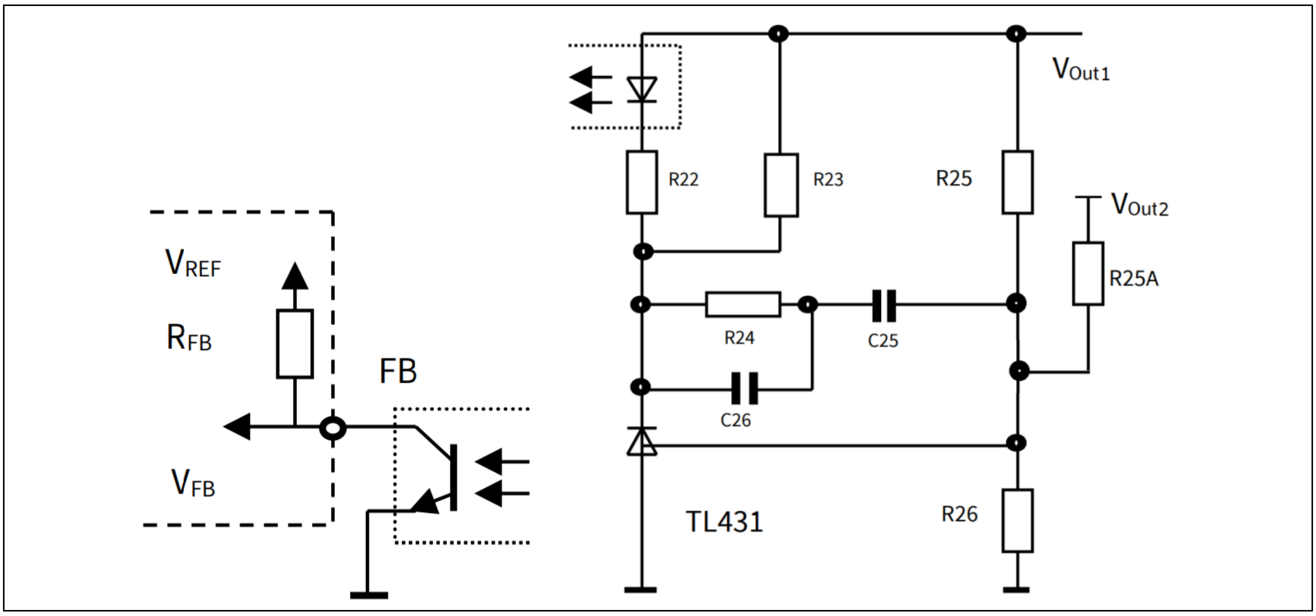
Line OVP

Line OVP

Input	Select AC input LOVP		V_{OVP_AC}	[V AC]	300
Input	High-side DC input voltage divider/resistor (R3A, R3B, R3C)		R_{I1}	[MΩ]	16
Input	Controller LOVP threshold		V_{VIN_LOVP}	[V]	2.85
Result	Low-side DC input voltage divider/resistor	Eq 109	R_{I2Cal}	[kΩ]	108.88
Input	Select low-side DC input voltage divider/resistor (R7)		R_{I2}	[kΩ]	110
Result	Post-calculated LOVP	Eq 110	V_{OVP_ACPost}	[V AC]	296.98

Output regulation (isolated using TL431 and optocoupler)

Isolated feedback circuit



Output regulation

Input	TL431 reference voltage		V_{REF_TL}	[V]	2.5
Input	Weighted regulation factor of V_{Out1}		W_1		0.6
Input	Current for voltage divider/resistor R26		I_{R26}	[mA]	1
result	Calculated voltage divider/resistor	Eq 111	$R26_{Cal}$	[kΩ]	2.5
Input	Select voltage divider/resistor value		R26	[kΩ]	2.5
result	Calculated voltage divider/resistor	Eq 112	$R25_{Cal}$	[kΩ]	15.83
Input	Select voltage divider/resistor value		R25	[kΩ]	15
result	Calculated voltage divider/resistor	Eq 113	$R25A_{Cal}$	[kΩ]	47.73
Input	Select voltage divider/resistor value		R25A	[kΩ]	47

Optocoupler and TL431 bias

Input	Current Transfer Ratio (CTR)		G_C	[Percent]	100 percent
Input	Optocoupler diode forward voltage		V_{FOpto}	[V]	1.25
Input	Maximum current for optocoupler diode		I_{Fmax}	[mA]	10
Input	Minimum current for TL431		I_{KAmin}	[mA]	1
Result	Calculated minimum optocoupler bias resistance	Eq. 114	$R22_{Cal}$	[kΩ]	0.825
Input	Select optocoupler bias resistor		R22	[kΩ]	0.82
Input	FB pull-up reference voltage V_{REF} from datasheet		V_{REF}	[V]	3.3
Input	V_{FB_OLP} from datasheet		V_{FB_OLP}	[V]	2.75
Input	R_{FB} from datasheet		R_{FB}	[kΩ]	15
Result	Calculated maximum TL431 bias resistance	Eq. 115	$R23_{Cal}$	[kΩ]	1.28
Input	Selected TL431 bias resistor		R23	[kΩ]	1.2

Regulation loop

Result	FB transfer characteristic	Eq. 116	K_{FB}		18.29
Result	Gain of FB transfer characteristic	Eq. 117	G_{FB}	[db]	25.25
Result	Voltage divider transfer characteristic	Eq. 118	K_{VD}		0.208333
Result	Gain of voltage divider transfer characteristic	Eq. 119	G_{VD}	[db]	-13.62
Result	Resistance at maximum load pole	Eq. 120	R_{LH}	[Ω]	5.31
Result	Resistance at minimum load pole	Eq. 121	R_{LL}	[Ω]	65.45
Result	Poles of power stage at maximum load pole	Eq. 122	f_{OH}	[Hz]	73.05
Result	Poles of power stage at minimum load pole	Eq. 123	f_{OL}	[Hz]	5.93
Result	Zero frequency of the compensation network	Eq. 124	f_{OM}	[Hz]	20.81

Input	Zero dB crossover frequency		fg	[kHz]	3
Input	PWM-OP gain from datasheet		A_V		2.03
Result	Transient impedance	Eq. 117	Z_{PWM}	[V/A]	1.4
Result	Power stage at crossover frequency	Eq. 118	$\lvert F_{PWR}(fg)\rvert$		0.144
Result	Gain of power stage at crossover frequency	Eq. 119	$G_{PWR}(fg)$	[db]	-16.84
Result	Gain of the regulation loop at fg	Eq. 120	Gs(ω)	[db]	-5.218
Result	Separated components of the regulator	Eq. 121	Gr(ω)	[db]	5.218
Result	Calculated resistance value of compensation network	Eq. 122	$R24_{Cal}$	[kΩ]	3.91
Input	Select resistor value of compensation network		R24	[kΩ]	20
Result	Calculated capacitance value of compensation network	Eq. 123	$C26_{Cal}$	[nF]	2.653
Input	Select capacitor value of compensation network		C26	[nF]	1
Result	Calculated capacitance value of compensation network	Eq. 124	$C25_{Cal}$	[nF]	381.31
Input	Select capacitor value of compensation network		C25	[nF]	330

Output regulation (non-isolated)

Final design

Electrical

Minimum AC voltage			[V]	90
Maximum AC voltage			[V]	264
Maximum input current			[A]	0.38
Minimum DC voltage			[V]	92
Maximum DC voltage			[V]	373
Maximum output power			[W]	27.1
Output voltage 1			[V]	12.0
Output ripple voltage 1			[mV]	0.4
Output voltage 1			[V]	20.0
Output ripple voltage 1			[mV]	0.7
Transformer peak current			[A]	1.41
Maximum duty cycle				0.52
Reflected voltage			[V]	101
Copper losses			[W]	0.22
MOSFET losses			[W]	1.50
Sum losses			[W]	5.54
Efficiency			[Percent]	83.03 percent

Transformer

Core type				EE20/10/6
Core material				TP4A(TDG)
Effective core area			[mm^2]	32
Maximum flux density			[mT]	251
Inductance			[µH]	274
Margin			[mm]	0
Primary turns			Turns	48
Primary copper wire size			AWG	26
Number of primary copper wires in parallel				1
Primary layers			Layer	2
Secondary 1 turns (N_{S1})			Turns	6
Secondary 1 copper wire size			AWG	31
Number of secondary 1 copper wires in parallel				7
Secondary 1 layers			Layer	1
Secondary 2 turns (N_{S2})			Turns	10
Secondary 2 copper wire size			AWG	31
Number of secondary 2 copper wires in parallel				7
Secondary 2 layers			Layer	2
Auxiliary turns			Turns	9
Leakage inductance			[µH]	0.7

Components

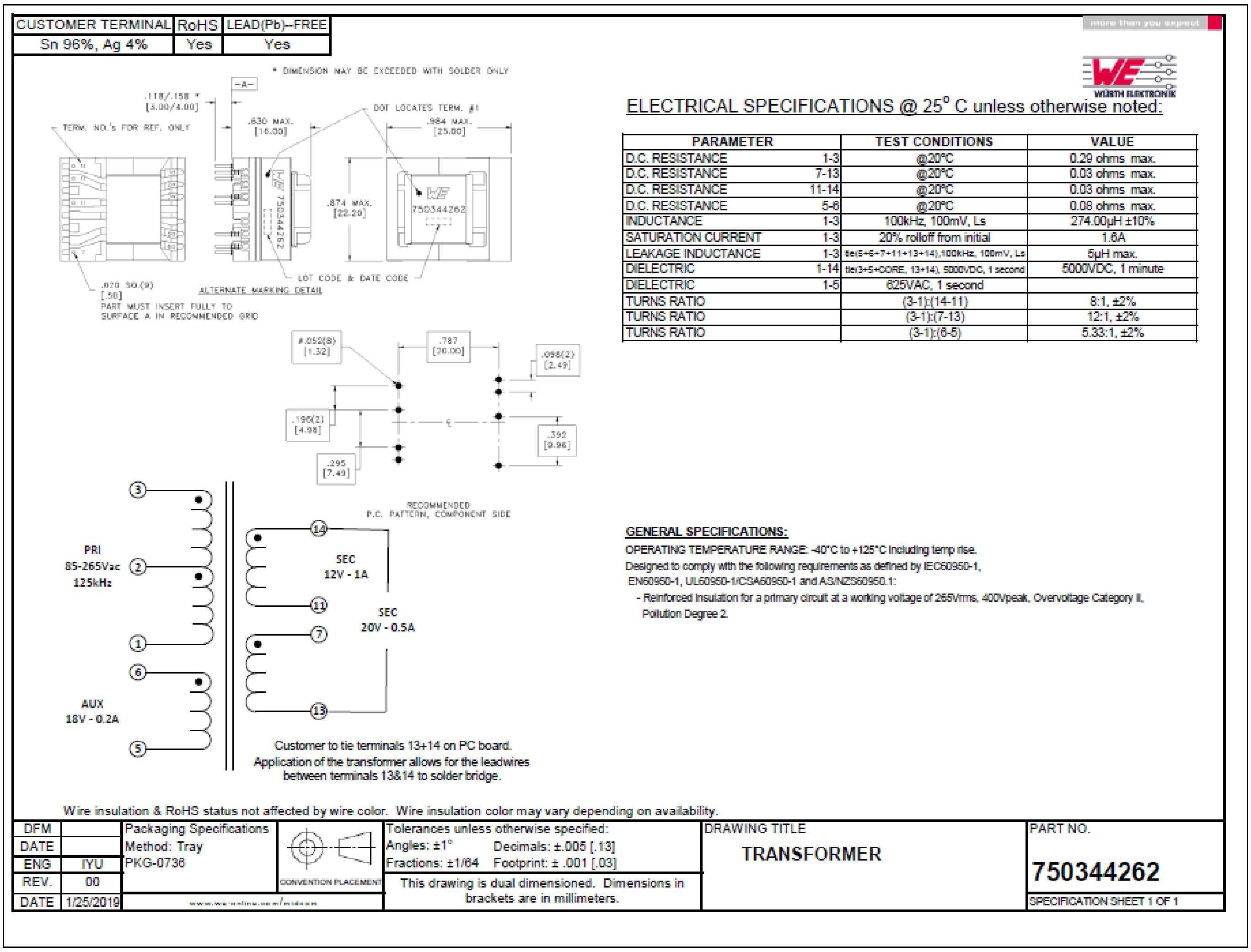
Input capacitor (C1)			[µF]	56.0
Secondary 1 output capacitor (C152)			[µF]	820.0

Secondary 1 output capacitor in parallel				1.0
Secondary 1 LC filter inductor (L151)			[µH]	4.7
Secondary 1 LC filter capacitor (C153)			[µF]	220.0
Secondary 2 output capacitor (C102)			[µF]	220.0
Secondary 2 output capacitor in parallel				1.0
Secondary 2 LC filter inductor (L101)			[µH]	4.7
Secondary 2 LC filter capacitor (C103)			[µF]	220.0
V_{CC} capacitor (C3)			[µF]	22.0
Sense resistor (R8A, R8B)			[Ω]	0.57
Clamping resistor (R4)			[kΩ]	470.0
Clamping capacitor (C2)			[nF]	1
High-side DC input voltage divider/resistor (R3A, R3B, R3C)			[MΩ]	16
Low-side DC input voltage divider/resistor (R7)			[kΩ]	110

Regulation components (isolated using TL431 and optocoupler)

Voltage divider		R26	[kΩ]	2.5
Voltage divider (V_{out1} sense)		R25	[kΩ]	15.0
Voltage divider (V_{out2} sense)		R25A	[kΩ]	47.0
Optocoupler bias resistor		R22	[kΩ]	0.82
TL431 bias resistor		R23	[kΩ]	1.2
Compensation network resistor		R24	[kΩ]	20.0
Compensation network capacitor		C26	[nF]	1.00
Compensation network capacitor		C25	[nF]	330.0

12 Appendix B: WE transformer specification



CUSTOMER TERMINAL	RoHS	LEAD(Pb)--FREE
Sn 96%, Ag 4%	Yes	Yes

Customer to tie terminals 13+14 on PC board.
Application of the transformer allows for the leadwires between terminals 13&14 to solder bridge.

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1-3	@20°C	0.29 ohms max.
D.C. RESISTANCE	7-13	@20°C	0.03 ohms max.
D.C. RESISTANCE	11-14	@20°C	0.03 ohms max.
D.C. RESISTANCE	5-6	@20°C	0.08 ohms max.
INDUCTANCE	1-3	100kHz, 100mV, Ls	274.00µH ±10%
SATURATION CURRENT	1-3	20% rolloff from initial	1.6A
LEAKAGE INDUCTANCE	1-3	tie(5+6+7+11+13+14),100kHz, 100mV, Ls	5µH max.
DIELECTRIC	1-14	tie(3+5+CORE, 13+14), 5000VDC, 1 second	5000VDC, 1 minute
DIELECTRIC	1-5	625VAC, 1 second	
TURNS RATIO		(3-1):(14-11)	8:1, ±2%
TURNS RATIO		(3-1):(7-13)	12:1, ±2%
TURNS RATIO		(3-1):(6-5)	5.33:1, ±2%

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C Including temp rise.

Designed to comply with the following requirements as defined by IEC60950-1, EN60950-1, UL60950-1/CSA60950-1 and AS/NZS60950.1:

- Reinforced Insulation for a primary circuit at a working voltage of 265Vrms, 400Vpeak, Overvoltage Category II, Pollution Degree 2.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

DFM		Packaging Specifications Method: Tray PKG-0736	CONVENTION PLACEMENT	Tolerances unless otherwise specified: Angles: ±1° Decimals: ±.005 [.13] Fractions: ±1/64 Footprint: ± .001 [.03]	DRAWING TITLE TRANSFORMER
DATE					
ENG	IYU				
REV.	00			This drawing is dual dimensioned. Dimensions in brackets are in millimeters.	PART NO. 750344262
DATE	1/25/2019	www.we-online.com/midcom			SPECIFICATION SHEET 1 OF 1

Figure 33 WE transformer specification

13 References

[1] ICE5GR2280AG datasheet, Infineon Technologies AG

[2] 5th-Generation Fixed-Frequency Design Guide

[3] CalculationTool_ICE5xSAG_ICE5xRxxxxAG

Revision history

Document version	Date of release	Description of changes
V 1.0	26 March 2019	First release

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Edition 2019-03-26

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
AN_1902_PL83_1903_022928

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