MTU

Memory Test Unit

AURIX™ TC3xx Microcontroller Training
V1.0 2020-06

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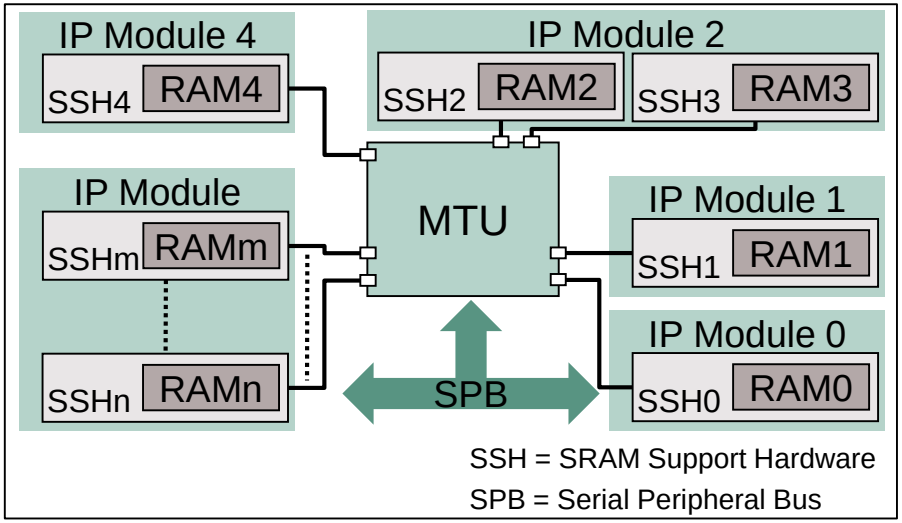
MTU
Memory Test Unit



Highlights

- The Memory Test Unit (MTU) controls and monitors the test, initialization and data integrity checking functions of the various internal memories in the AURIX™ TC3xx devices.

Key Features

- Memory Initialization
- Memory Built-In-Self-Test (MBIST)
- Unified interface to internal SRAM Support Hardware (SSH)

Customer Benefits

- Fills the memories with a pre-defined data value for initialization
- Verification of integrity of the internal SRAMs realized in hardware
- SSH provides a direct access to the memories, without CPU overload

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MTU
Memory Initialization

- Each SRAM in the system can be individually initialized via the MTU
- The MTU offers two initialization options:
  - Clear an SRAM by writing “0” to all memory locations
    - User only needs to set one bit in a register to have a cleared SRAM
    - Everything else is done in hardware
    - CPU is not used to access the SRAM
  - Fill up a SRAM with a defined pattern chosen by the user
    - User needs to provide the pattern to be written in the SRAM and start the write operation
    - CPU is not used to access the SRAM
- The MTU protects the security sensitive memories against unintended initialization

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MTU
Memory Built-In-Self-Test (MBIST)

- The MTU enables the user to perform various Memory Built-in Self Tests (MBIST) on the memory and the test results are signaled via an interrupt
- The MTU MBIST relies on an Error Correction Code which has the following characteristics:
  - Single Bit Error Correction
  - Double Bit Error Detection
- The MTU also sends alarm notification to Safety Management Unit (SMU):
  - The MTU sends SRAM specific alarms to the SMU
    - Correctable Error alarm
    - Uncorrectable Critical Error alarm
    - Miscellaneous Error alarm

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MTU
Unified interface to internal SRAM Support Hardware

- Each SRAM has some digital logic surrounding it, known as SRAM Support Hardware (SSH)
- The SSH controls the Error Detection & Correction and the Memory Built-In-Self-Test (MBIST) of internal memories
- There are multiple SSH instances, each controlling one or more different internal memories:
  - The MTU provides a unified register interface to control the operation of each SSH instance
  - MTU can control directly the SSH instances for various test types on each SRAM block
  - The SSH provides direct access to the memories, without involving the CPU
  - Even small memories that are not directly accessible via the CPU can be tested via SSH

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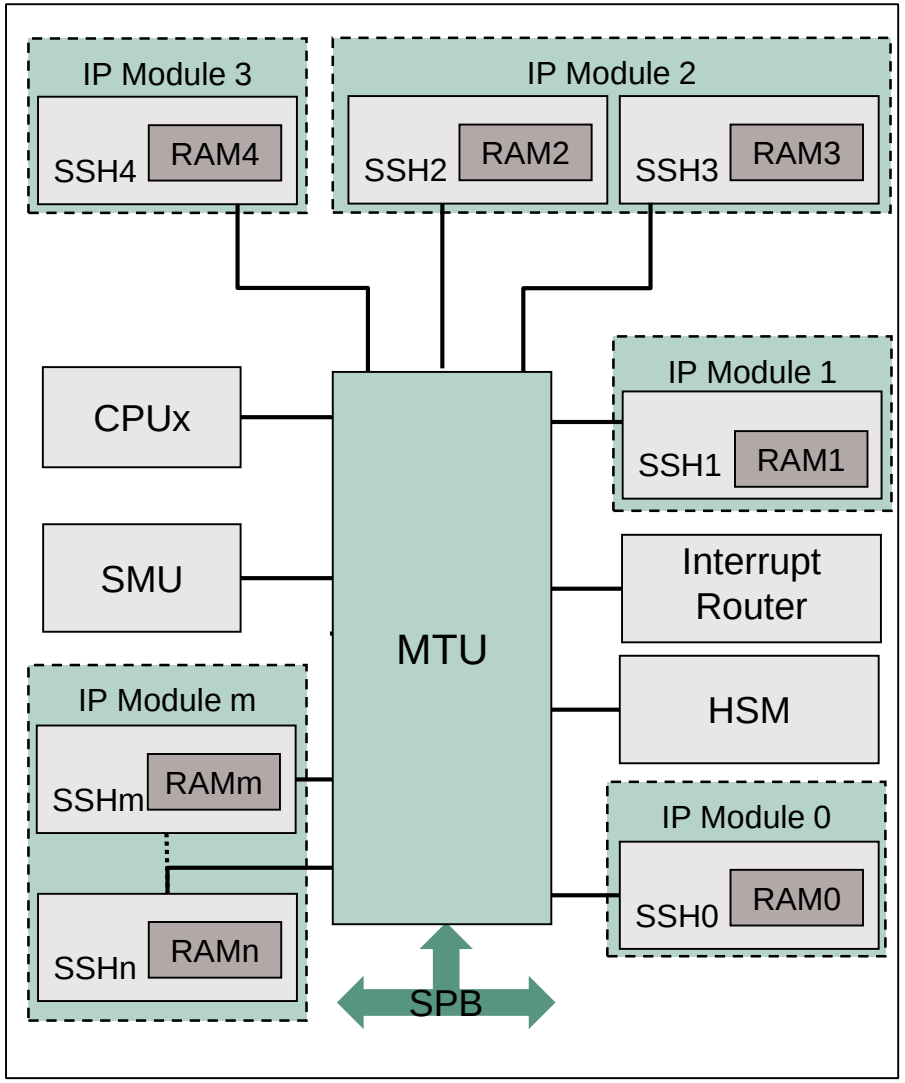
MTU
System Integration

- The MTU is a unified interface for the control of MBIST, ECC and memory initialization
- Different IP modules in the system (E.g. CPU, LMU, CAN etc.) may have one or more than one SRAM inside them
- Surrounding every SRAM is its own SRAM Support Hardware (SSH) wrapper
- The MTU also ensure the protection of security sensitive memories against unintended initialization that might lock the device



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Email: erratum@infineon.com

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