

CONVCTRL

Converter Control Block

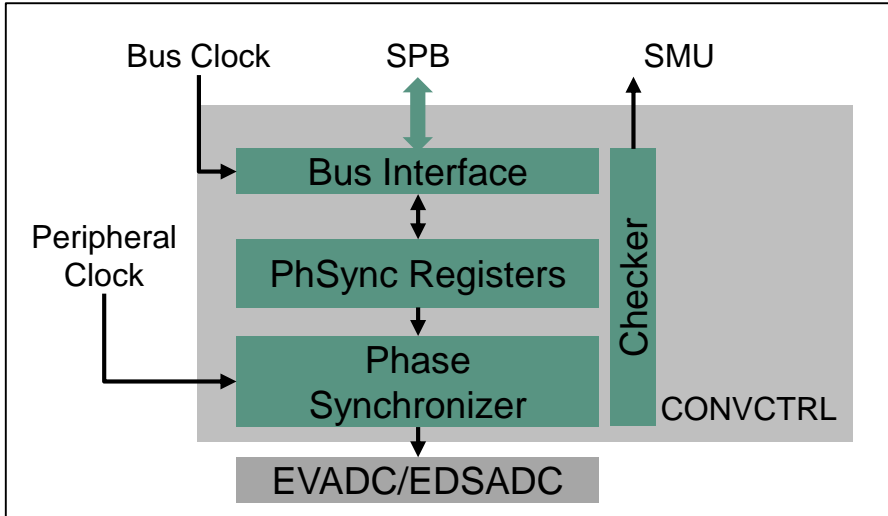
AURIX™ TC3xx Microcontroller Training
V1.0 2020-09



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CONVCTRL

Converter Control Block



Highlights

- > The converter control block is used for the common control functions of all converters implemented in AURIX™ TC3xx

Key Features

Phase Synchronizer

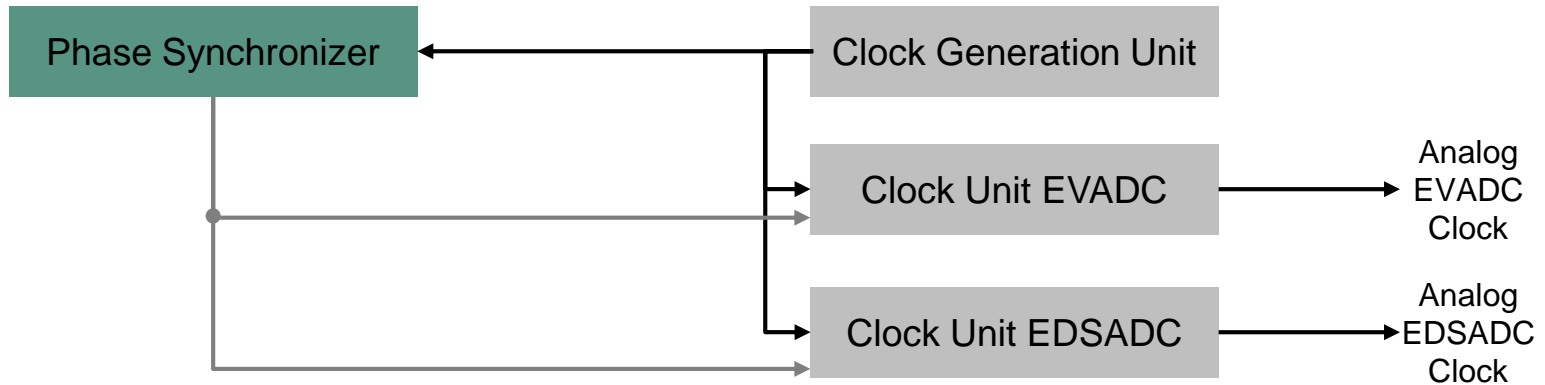
Safety measures

Customer Benefits

- > Provides a specific clock enable signal to synchronize the operations of all analog blocks within EVADC and EDSADC
- > Both the Phase Synchronizer and the converters are supervised in order to ensure the correct operation

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Phase Synchronizer

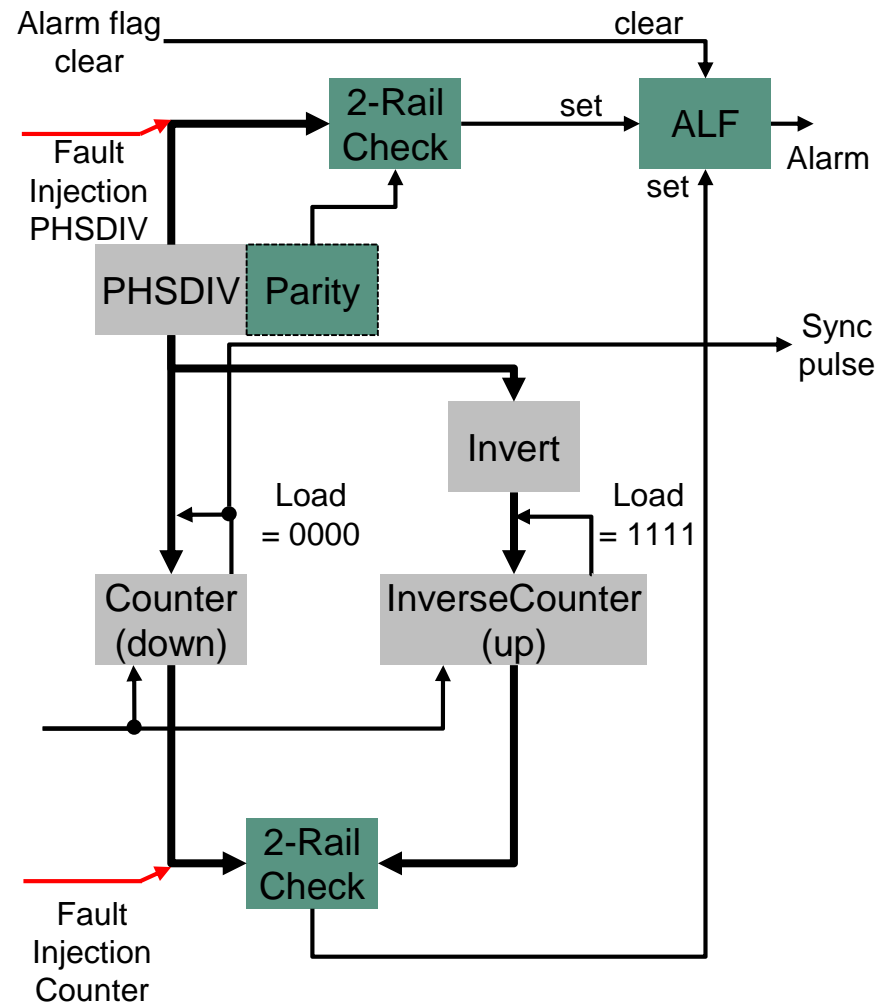


- › These analog blocks use the voltage references and synchronizing their clock edges avoid any performance loss due to the mutual cross-coupling via the reference lines
- › The CONVCTRL ensures that all switching activities connected to the analog blocks occur at the same clock edge, therefore the ringing that occurs on the reference lines does not disturb the operation of another analog block
- › The Phase Synchronizer broadcasts its clock enable signal, while each connected module locally generates its own analog clock signal based on the Phase Synchronizer signal. With this approach, no additional clock balancing is required

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Safety measures

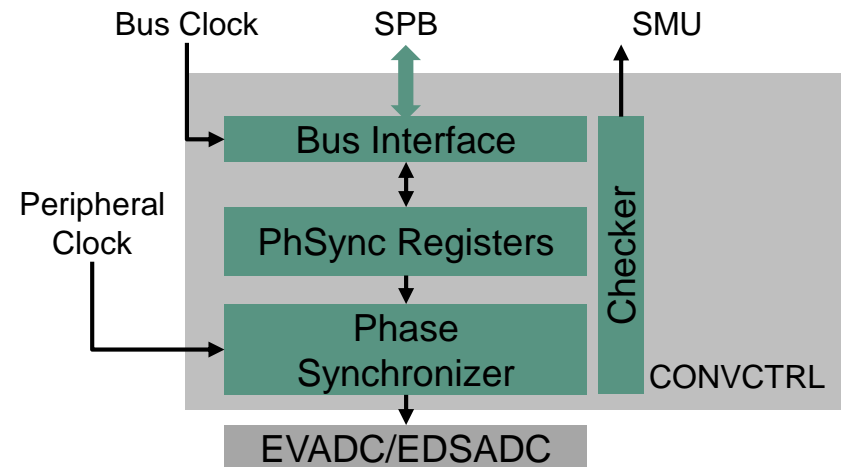
- › CONVCTRL comprises the following safety measures:
 - **Parity-Protection of the Prescaler Value:** the additional parity bit helps to detect a corrupted prescaler value which might lead to the wrong synchronization frequency of the converters
 - **Run-Time Supervision of the Counter:** two counter are working in parallel and their states are constantly compared
- › In case of a failure in any of the above cases, an alarm is triggered
- › Additionally, the software can deliberately inject a fault condition into both mechanisms in order to test the supervision measures



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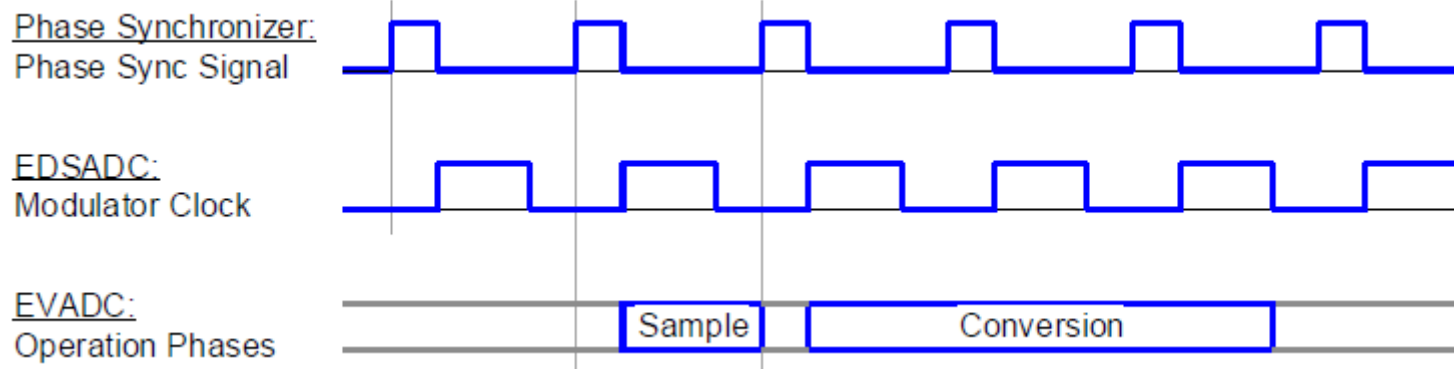
System Integration

- › The CONVCTRL receives the peripheral clock and the bus clock from the Clocking system
- › After synchronization, both EVADC and EDSADC are generating their internal clocks based on CONVCTRL trigger
- › Additionally, CONVCTRL is connected to the Safety Management Unit (SMU), where all the alarms are signalled
- › As a response to the alarm different reactions can be configured, for example a module reset or an interrupt



Application example

Inter-module Synchronization



Overview

- > The converters can be synchronized in order to eliminate the interference of concurrently operating ADC channels
- > The EDSADC uses the signal directly to generate its modulator signal, while EVADC is using it to start a conversion

Advantages

- > Each converter can reach its optimum performance
- > Easy configuration for the synchronization of all converters

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