MTU
Memory Test Unit

AURIX™ TC2xx Microcontroller Training
V1.0 2019-03

MTU
Memory Test Unit

MC = Memory Controller
SPB = Serial Peripheral Bus
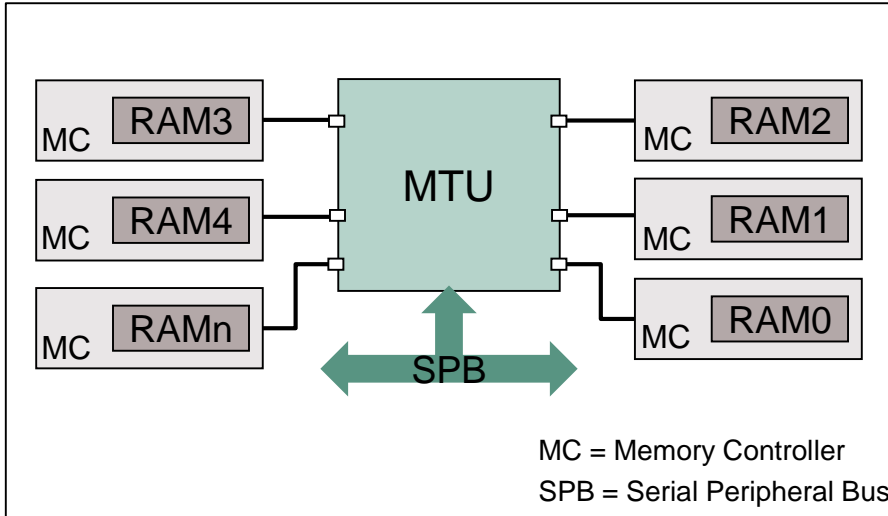
Highlights

› The Memory Test Unit (MTU) integrates a unified interface for the control of Error Correction (ECC), Built-in-Self-Test (BIST) and redundancy features on the internal SRAMs within the AURIX™ family of microcontrollers.

Key Features

Memory Initialization

Memory Built-In-Self-Test (MBIST)

Customer Benefits

› Fill the memories with a pre-defined data value for initialization

› Verification of integrity of the internal SRAMs realized in hardware

MTU
Memory Initialization

› Each SRAM in the system can be individually initialized via the MTU

› The MTU offers two initialization options:

– Clear a SRAM by writing "0" to all memory locations

– User only needs to set one bit in a register to have a cleared SRAM

– Rest is done in HW

– CPU not used to access the SRAM

– Fill up a SRAM with a defined pattern chosen by the user

– User needs to provide the pattern to be written in the SRAM and start the write operation
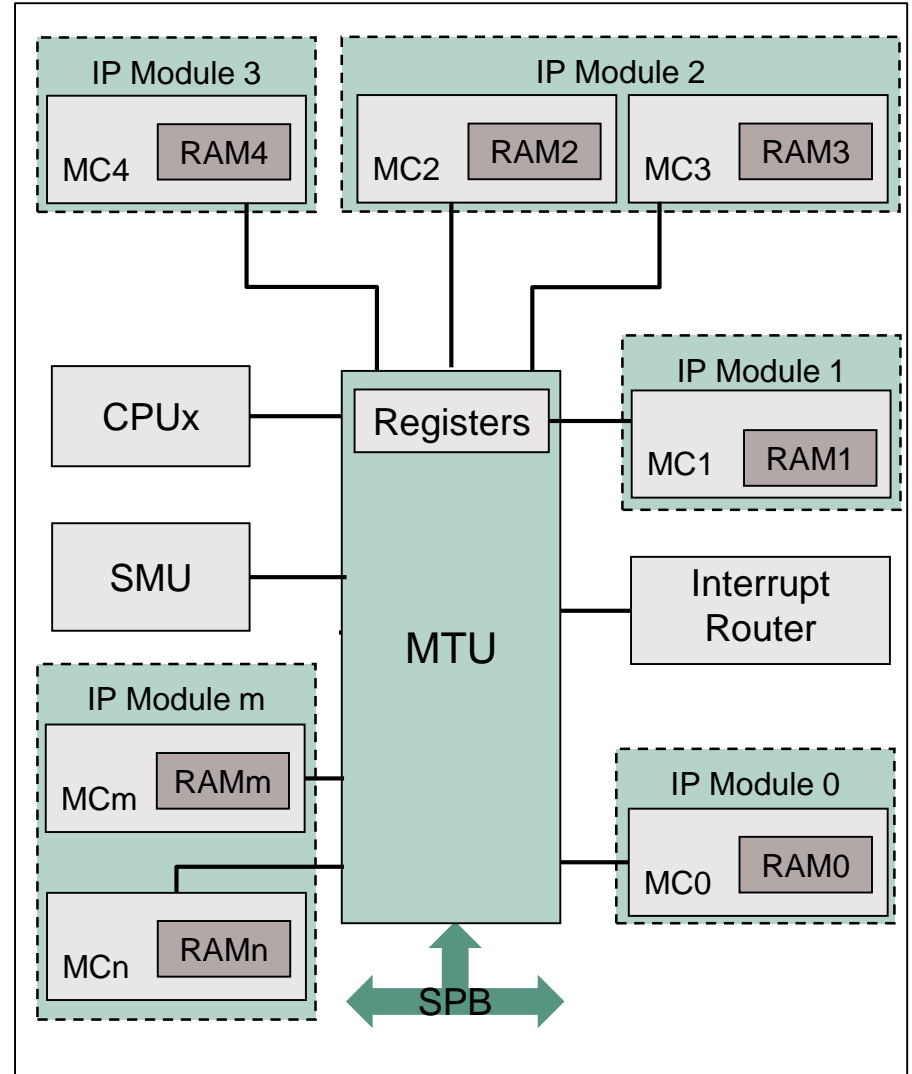
– CPU not used to access the SRAM

MTU
Memory Built-In-Self-Test (MBIST)

› The MTU enables the user to perform various Memory Built-in Self Tests (MBIST) on the memory and obtains the test results

› The MTU MBIST relies on an Error Correction Code which has the following characteristics:

   – Single Bit Error Correction

   – Double Bit Error Detection

› The MTU also sends alarm notification to Safety Management Unit (SMU):

   – The MTU sends SRAM specific alarms to the SMU

   – Correctable Error alarm

   – Uncorrectable Error alarm

   – Address Error

   – Error Buffer Overflow

MTU
System Integration

› The MTU is a unified interface for the control of MBIST, ECC and memory initialization

› Different IP modules in the system (E.g. CPU, LMU, CAN etc.) may have one or more than one SRAM inside them

› Surrounding every SRAM is its own SRAM Memory Controller (MC) wrapper, with its own registers and MBIST logic.

› The advantage of using the MTU is that it provides direct access to the memories without using the CPU

› Even small memories that are not directly accessible via the CPU can be tested using MBIST

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