HybridPACK™ Automotive Power Modules

Explanation of Technical Information

About this document

This application note supports automotive power electronics engineers in understanding datasheet parameters.

Scope and purpose

This document helps to understand datasheet parameters of automotive power modules and its device characteristics. It explains the interaction between the parameters and the influence of boundary conditions. Automotive typical specifications like parameters needed for direct fluid cooled power modules are also addressed in this application note.

Intended audience

Power electronics engineers. Engineers responsible for automotive power modules.

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1 Introduction

The nomenclature of the Infineon power modules datasheets is mainly based on the IEC 60747-15 standard for IGBTs [1], IEC 60747-2 standard for rectifier diodes [2] and IEC 60747-9 standard for isolated power semiconductor devices [3]. The power electronics engineers can on the one hand compare devices from different vendors, while on the other hand they can figure out the limits of the devices based on these datasheet parameters.

This document helps to understand the datasheet parameters and device characteristics. It explains the interaction between the parameters and the influence of boundary conditions. Datasheet values that refer to dynamical characterization tests (e.g. switching losses), are related to a specific test setup with defined stray inductance, gate resistor, driver type, etc. .These system parameters can deviate from a final user application, which is explained in this application note.

The attached diagrams, tables and explanations are referring to datasheet templates, used by automotive IGBT modules released in year 2017 or later. Older datasheet templates may have a different appearance but the technical meaning is still the same if not noted specially and thus this application note can also be applied to older product datasheets.

For the latest version of the automotive HybridPACK™ datasheets please refer to our webpage www.infineon.com/hybridpack.

1.1 Status of datasheets

Depending on the status of the product development, the relating technical information contains:

- Target data (Revisions V1.x)
- Preliminary data (Revisions V2.x)
- Final data (Revisions V3.x)

V1.x Target data describes the design goal of the future product. The technical data may change during the development phase without any notice.

V2.x Preliminary data is based on components produced from series tools. The manufacturing is close to production, but partly in development. Mechanical, thermal and electrical data can change slightly during the further development process. Qualification is still ongoing and final results are pending.

V3.x Final data is based on final components. Manufacturing is done under series conditions considering productive tooling for mass production. Mechanical, thermal and electrical data are fixed and can be changed only under the valid terms of the corresponding PCN (Product Change Notification) process. Reliability and lifetime is approved and released. Only final power module datasheets describe the properties of a released product.

2 IGBT, Inverter Maximum Rated Values

2 IGBT,Inverter

2.1 Maximum Rated Values

Parameter	Conditions	Symbol	Value	Unit
Collector-emitter voltage	T_{vj} = 25°C	V_{CES}		V
Implemented collector current		I_{CN}		A
Continuous DC collector current	T_F = °C, $T_{vj\,max}$ = °C	$I_{C\,nom}$		A
Repetitive peak collector current	t_P = 1 ms	I_{CRM}		A
Total power dissipation	T_F = °C, $T_{vj\,max}$ = °C	P_{tot}		W
Gate-emitter peak voltage		V_{GES}		V

Figure 1 Overview maximum rated values (template).

2.1 Collector-emitter voltage (V_{CES})

The permissible peak collector-emitter voltage is specified typically at a junction temperature of 25°C. The allowed collector emitter voltage decreases by about 0.6V/K (i.e. ≈40V lower for -40°C compared to the 25°C value) for IGBT3/Emcon3 650V technologies. A maximum allowed collector-emitter voltage over different junction temperatures can be typically obtained in the characteristics diagrams section of the datasheet.

The allowed leakage currents at the peak collector emitter voltage (i.e. the collector-emitter cut-off current I_{ces}) is defined in the characteristic values. When maximum V_{CES} is applied, the leakage current will be lower than the characteristic I_{CESmax}. Applying a collector-emitter voltage higher than specified V_{CES} may lead to an increased I_{CES} and can cause breakdown failure. Therefore, it is very important that under all conditions the maximum allowed collector-emitter voltage is not exceeded at any time.

2.2 Implemented collector current (I_{CN})

An implemented collector current is not defined in the IEC 60747 standards [1][2][3] and has without defined temperatures no technical meaning in terms of a current capability or possible inverter output power. Due to this fact, this current value should never be used to benchmark power modules, especially not over different manufacturers. Nevertheless, this value is used by almost all semiconductor companies for a rough classification of the potential power class of the power module and is also used for the type designation of the power modules. For some latest power module developments, which are qualified based on the standard AGQ 324 from the ZVEI organization [4] (e.g. HybridPACK™ Drive product family), the I_{CN} current value plays an important role. It is clearly defined, that power cycling tests have to be performed at different ΔT[1] in order to provide a power cycling robustness curve. At least one test (i.e. typically the test with highest ΔT) has to be performed minimally at 85% of the I_{CN} value. This requirement ensures that the implemented collector current is application relevant. Nevertheless, a wide range of currents can be defined on the same part and thus the I_{CN} rating is still not useable for benchmarking power modules.

A module with FS820 type designation (I_{CN} = 820A), which is qualified based on the AQG 324 standard, has to be tested at least with 697 A_{dc} during the IGBT power cycling test with highest ΔT. At Infineon the I_{CN} value is furthermore used to derive the repetitive collector current I_{CRM} (see later sections for explanations).

[1] ΔT at power cycling test is the temperature delta between the maximum and minimum junction temperature during an alternating load current cycle.

2.3 Continuous DC collector current (I_{Cnom})

In contrast to the implemented collector current the continuous DC collector current I_{Cnom} is specified with temperature values and is calculated from the thermal characteristics and the output characteristics:

$$I_{Cnom} = \frac{T_{vjop\,max} - T_F}{R_{thJF\,IGBT\,max} \cdot V_{CEsat\,max}(I_C, T_{vj})} \quad (2.1)$$

The datasheet specifies this current value at a typical application cooling fluid temperature and the maximum junction temperature. Furthermore, the maximum thermal resistance at the defined conditions and the worst case conduction conditions are applied to derive the continuous DC collector current.

Before benchmarking different power modules it is necessary to check if the same parameters are applied to derive the I_{Cnom} value. In almost all cases different typical cooling conditions are assumed. But sometimes Rth and V_{CEsat} typical values are applied rather than maximum values. Different cooling flow rates (and/or pressure drop) in the system reduce or increase R_{thJF} values. Only with equal boundary conditions the equal and comparable I_{Cnom} values will be calculated.

The power module continuous DC collector current can be applied for long operating times (minutes, hours) if not otherwise noted in the maximum allowed terminal currents.
Please note that current ratings without defined temperature conditions have no technical meaning at all.

2.4 Repetitive peak collector current (I_{CRM})

The repetitive peak collector current is in theory derived from the feasible power dissipation and the thermal impedance Z_{th}. However, this theoretical value does not take into account any limitations of bond wires, chip reverse bias safe operating area (RBSOA), etc.
Therefore, the datasheet value is quite low compared to a theoretical calculated value from Z_{th} values and the chip output characteristics, but it specifies a safe switching operation considering all practical limitations of the power module. Each Infineon automotive power module is tested in a RBSOA test (IGBT turn-off test) minimally at the specified I_{CRM} value and minimally at the specified dv/dt given in the turn-off energy loss per pulse section (see 3.2.2).

2.5 Total power dissipation (P_{tot})

This parameter describes the maximum feasible power dissipation per IGBT switch, which is in general calculated with:

$$P_{tot} = \frac{\Delta T}{R_{thmax}} \quad (2.2)$$

The ΔT and R_{thmax} are defined depending on the product. For power modules with a PinFin baseplate (i.e. direct cooling fluid structure) the total power dissipation as a function of the cooling fluid temperature is calculated with:

$$P_{tot}(T_F) = \frac{T_{vjopmax} - T_F}{R_{thJFmax}} \quad (2.3)$$

The total power dissipation as a function of the case temperature for power modules with a flat base plate or without baseplate is calculated with:

$$P_{tot}(T_C) = \frac{T_{vjopmax} - T_C}{R_{thJCmax}} \quad (2.4)$$

The feasible power dissipation of the diode chips can be calculated respectively.

For comparisons between products with PinFin (fluid temperature) and flat or no baseplate (case temperature) it is important to take into account also the system Rth. Products with PinFin cooling structure includes the entire thermal stack and thus specify the P_{tot} directly in dependence of the cooling fluid temperature. No additional terms have to be added.
When P_{tot} is defined with regards of the case temperature, it is obvious that not the entire thermal stack is considered. The customer specific R_{thCH} and R_{thHF} has to be added in the calculation (CH Case to Heatsink; HF Heasink to Fluid) as the layers show also a ΔT. But these values are system parameters (outside of the power module) and thus cannot be specified in the power module datasheet. Sometimes typical values are specified, which give a rough indication for typical assemblies.
More information about Tj, Tvj, etc nomenclature can be found under [8].

2.6 Gate-emitter peakvoltage (V_{GES})

This parameter specifies the maximum voltage allowed for the gate-emitter voltage. The corresponding leakage current under this condition is specified in the characteristics values table (see I_{GES}).

3 IGBT, Inverter Characteristic Values

The IGBT characteristic in the Infineon power module datasheets is organized in the following blocks: static characteristics, dynamic – switching characteristic, short circuit characteristic and its thermal characteristics as shown in Figure 2.

2.2 Characteristic Values

			min.	typ.	max.	
Collector-emitter saturation voltage	I_C = A, V_{GE} = 15 V; T_{vj} = 25°C I_C = A, V_{GE} = 15 V; T_{vj} = 150°C I_C = A, V_{GE} = 15 V; T_{vj} = 175°C I_C = A, V_{GE} = 15 V; T_{vj} = 25°C I_C = A, V_{GE} = 15 V; T_{vj} = 175°C	$V_{CE\,sat}$				V
Gate threshold voltage	I_C = mA, V_{CE} = V_{GE}; T_{vj} = 25°C T_{vj} = 175°C	V_{GEth}				V
Gate charge	V_{GE} = -8 V ... 15 V, V_{CE} = 400V	Q_G				µC
Internal gate resistor	T_{vj} = 25°C	R_{Gint}				Ω
Input capacitance	f = 1 MHz, V_{CE} = 50 V, V_{GE} = 0 V; T_{vj} = 25°C	C_{ies}				nF
Output capacitance	f = 1 MHz, V_{CE} = 50 V, V_{GE} = 0 V; T_{vj} = 25°C	C_{oes}				nF
Reverse transfer capacitance	f = 1 MHz, V_{CE} = 50 V, V_{GE} = 0 V; T_{vj} = 25°C	C_{res}				nF
Collector-emitter cut-off current	V_{CE} = V, V_{GE} = 0 V; T_{vj} = 25°C V_{CE} = V, V_{GE} = 0 V; T_{vj} = 175°C	I_{CES}				mA
Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V; T_{vj} = 25°C	I_{GES}				nA
Turn-on delay time, inductive load	I_C = A, V_{CE} = V; T_{vj} = 25°C V_{GE} = -8 V / +15 V; T_{vj} = 150°C R_{Gon} = Ω; T_{vj} = 175°C	$t_{d\,on}$				µs
Rise time, inductive load	I_C = A, V_{CE} = V; T_{vj} = 25°C V_{GE} = -8 V / +15 V; T_{vj} = 150°C R_{Gon} = Ω; T_{vj} = 175°C	t_r				µs
Turn-off delay time, inductive load	I_C = A, V_{CE} = V; T_{vj} = 25°C V_{GE} = -8 V / +15 V; T_{vj} = 125°C R_{Goff} = Ω; T_{vj} = 175°C	$t_{d\,off}$				µs
Fall time, inductive load	I_C = A, V_{CE} = V; T_{vj} = 25°C V_{GE} = -8 V / +15 V; T_{vj} = 150°C R_{Goff} = Ω; T_{vj} = 175°C	t_f				µs
Turn-on energy loss per pulse	I_C = A, V_{CE} = V, L_S = nH; T_{vj} = 25°C V_{GE} = -8 V / +15 V; T_{vj} = 150°C R_{Gon} = Ω; T_{vj} = 175°C di/dt (T_{vj} 25°C) = A/µs di/dt (T_{vj} 150°C) = A/µs	E_{on}				mJ
Turn-off energy loss per pulse	I_C = A, V_{CE} = V, L_S = nH; T_{vj} = 25°C V_{GE} = -8 V / +15 V; T_{vj} = 150°C R_{Goff} = Ω; T_{vj} = 175°C dv/dt (T_{vj} 25°C) = V/µs dv/dt (T_{vj} 150°C) = V/µs	E_{off}				mJ
SC data	$V_{GE} \leq$ 15 V, V_{CC} = V; $t_P \leq$ µs, T_{vj} = 25°C $V_{CEmax} = V_{CES} - L_{sCE} \cdot di/dt$; $t_P \leq$ µs, T_{vj} = 175°C	I_{SC}				A
Thermal resistance, junction to cooling fluid	per IGBT; $\Delta V/\Delta t$ = 10 dm³/min, T_F = °C	R_{thJF}				K/W
Temperature under switching conditions	t_{op} continuous for 10s within a period of 30s, occurence maximum times over lifetime	$T_{vj\,op}$	-40 150		150 175	°C

Static Characteristic

Dynamic Characteristic

Short Circuit Characteristic

Thermal Characteristic

Figure 2 IGBT characteristic values (template).

3.1 Static Characteristics

3.1.1 Collector-emitter saturation voltage (V_{CEsat})

The collector-emitter saturation voltage (V_{CEsat}) is one of the most used benchmarking value of an IGBT product and depends on the applied current (I_C), gate voltage (V_{GE}), junction temperature (T_{vj}) as well as the implemented chip size and its chip technology.

Power module datasheets specifies in general the chip values for (V_{CEsat}) as this is the most relevant parameter for calculating chip power losses and temperatures via the chip thermal resistance (R_{th}).
When the voltage drop is measured over the power tabs it is normal that higher values than the chip only values are obtained, because the voltage drop of the package resistance ($R_{CC'EE'}$) is included in the measurement.

Most product datasheets with EDT2 IGBTs notes two different operating points for V_{CEsat}. This simplifies the data extraction for linearized simulation models, which use V_{ce0} (i.e. voltage drop across the pn-junction) and R_{ce} (i.e. resistive part of the device) as a behavioral model. When only a single operating point is specified in the numeric table of the datasheet the corresponding values can also be obtained from the diagram section under the IGBT

output characteristics. In the following section these two V_{CEsat} operation points are noted as "_low" and "_high". With the two operating points (I_{C_low}, V_{CEsat_low} & I_{C_high}, V_{CEsat_high}) the linearized model can be simply calculated with:

$$R_{CE} = \frac{V_{CEsat\_high} - V_{CEsat\_low}}{I_{C\_high} - I_{C\_low}} \quad (3.1)$$

$$V_{CE0} = V_{CEsat\_low} - \left(R_{CE} * I_{C\_low}\right) \quad (3.2)$$

The following table and calculation provide an example:

Parameter	Conditions	Value
IGBT V_{CEsat}	I_C = **450A (I_{C_low})** T_{vj} = 25°C	**V_{CEsat_low} = 1.10V**
IGBT V_{CEsat}	I_C = **820A (I_{C_high})** T_{vj} = 25°C	**V_{CEsat_high} = 1.35V**
IGBT V_{CEsat}	I_C = **450A (I_{C_low})** T_{vj} = 175°C	**V_{CEsat_low} = 1.15V**
IGBT V_{CEsat}	I_C = **820A (I_{C_high})** T_{vj} = 175°C	**V_{CEsat_high} = 1.55V**

$$R_{ce\_25°C} = \frac{1.35V - 1.10V}{820A - 450A} \approx 0.68m\Omega \; ; \quad V_{CE0\_25°C} = 1.10V - (0.68m\Omega * 450A) \approx 0.79V$$

$$R_{ce\_175°C} = \frac{1.55V - 1.15V}{820A - 450A} \approx 1.08m\Omega \; ; \quad V_{CE0\_175°C} = 1.15V - (1.08m\Omega * 450A) \approx 0.66V$$

3.1.2 Gate threshold voltage (V_{GEth}), transfer and short circuit characteristic

The gate-emitter threshold voltage specifies when the IGBT starts to conduct. The collector current has low absolute values at this condition. As all modern IGBTs are designed for switching operation (not for linear mode, where IGBT is desaturated) it is important that the gate driver circuit ensure during the turn-off phase a gate-emitter voltage, which is lower than the specified V_{GEth} value. Otherwise the switches will overheat in a thermal runaway event and may lead finally to module damage.
Please note that the V_{GEth} value is not the Miller plateau level during the dynamic turn-on and off switching events (see Figure 4 for a deeper understanding). This Miller plateau level can be obtained from the transfer characteristics diagrams. Depending on the gate current (I_g) during the Miller plateau level (V_{pl}) and IGBT internal gate resistance (R_{gint}) the externally measured Miller plateau can be expected at the following level: $V_{pl,extern} = V_{pl} - (I_g \cdot R_{gint})$.

The V_{GEth} can be seen as the quasi-starting point of the transfer characteristic. The short circuit current is in this meaning the end-point of the transfer characteristic as it defines the transfer current at typical V_{GE} = 15V. Knowing this information the transfer characteristic diagram can be extrapolated as shown in the example of Figure 3

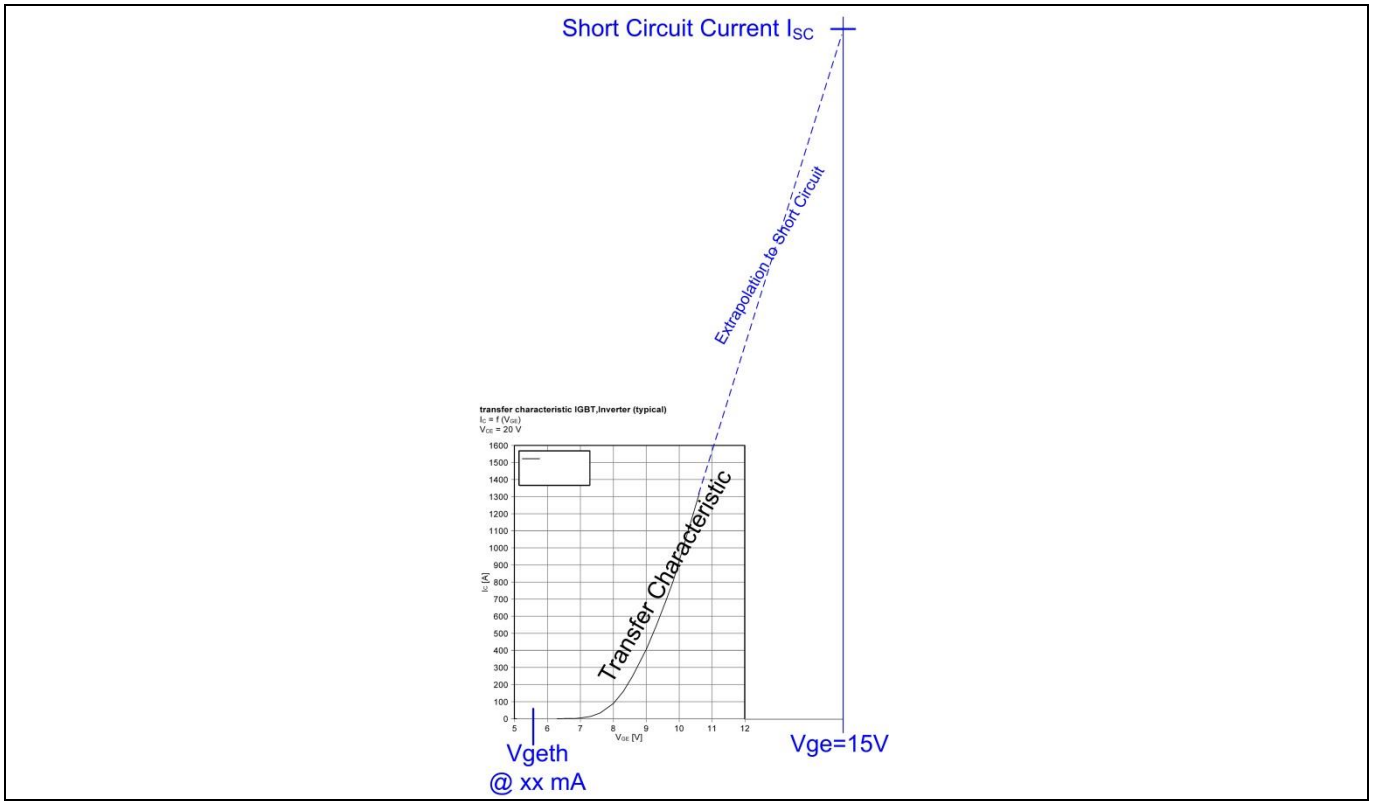

Figure 3 Gate threshold, transfer characteristic and short circuit.

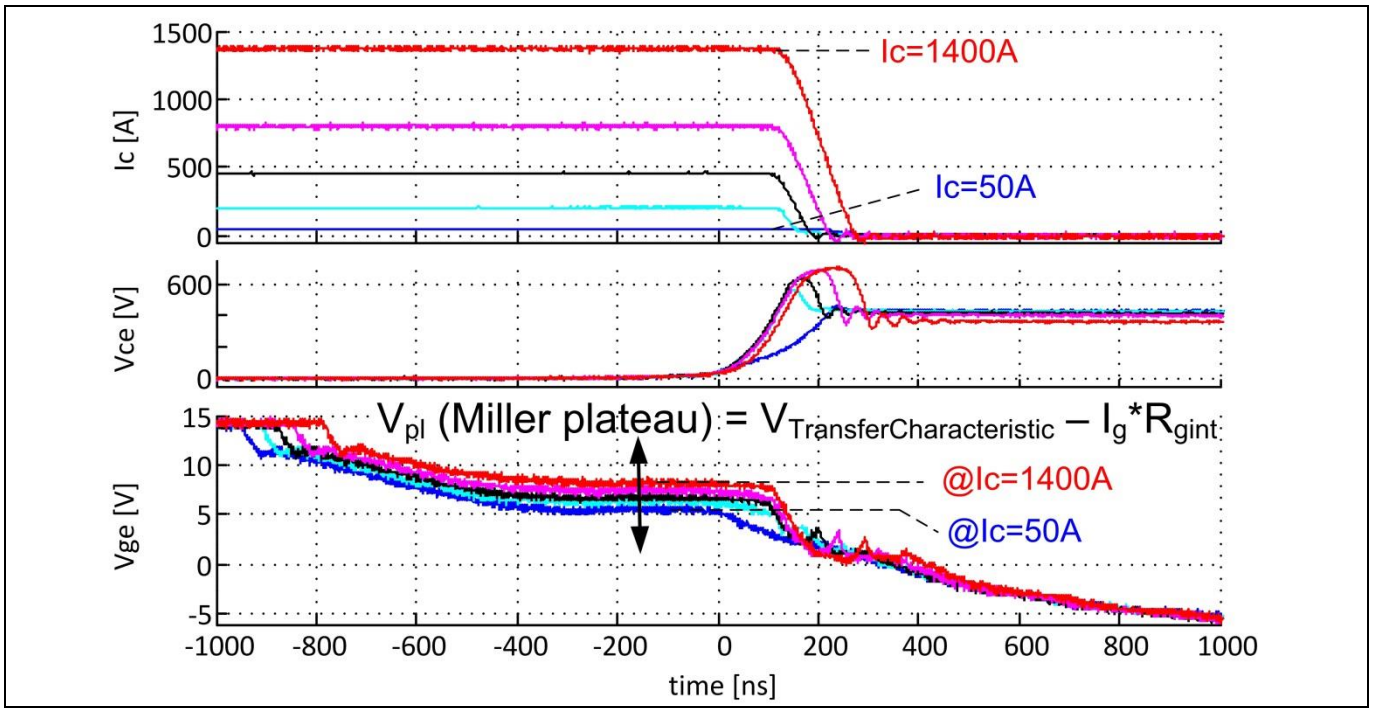

Figure 4 Dynamic turn-off switching event at different currents. The Miller plateau level (V_{pl}) depends on the transfer characteristic, the gate current and internal gate resistance.

Figure 4 show a measured IGBT turn-off event at different current levels (in this example 50..1400A). The Miller plateau level rises depending on the transfer characteristics. With very simplified consideration (i.e. zero gate current or zero internal gate resistance): the Miller plateau would be at the V_{geth} level when switching only some milliamperes. The plateau will follow exactly the transfer characteristic for higher currents.

When the current is further increased (e.g. a short circuit condition) the plateau will reach the V_{ge_on} value (in the example V_{ge}=15V). The IGBT cannot create enough charge carriers to support a low on-resistance and it will desaturate. In desaturated mode the V_{ce} voltage rises up to the working voltage.

3.1.3 Gate charge (Q_G)

The value of the gate charge is useful in order to design the gate driving circuit. The average output power required from the gate driving circuit can be calculated with data of the gate charge, gate drive voltages and switching frequency:

$$P_{Gdr} = Q_G \cdot \left(V_{GE(on)} - V_{GE(off)}\right) \cdot f_{sw} \quad (3.3)$$

Q_G itself is also depending on the gate driving voltages. When Q_G of different products have to be compared it is important to compare the Q_G values at the same $V_{GE(on)}$ and $V_{GE(off)}$ values. In the power module datasheets with EDT2 IGBT chipset a gate charge characteristic over different gate drive voltages can be obtained in the characteristic diagrams section and Q_G for different gate drive voltages can be derived as shown in the following examples:

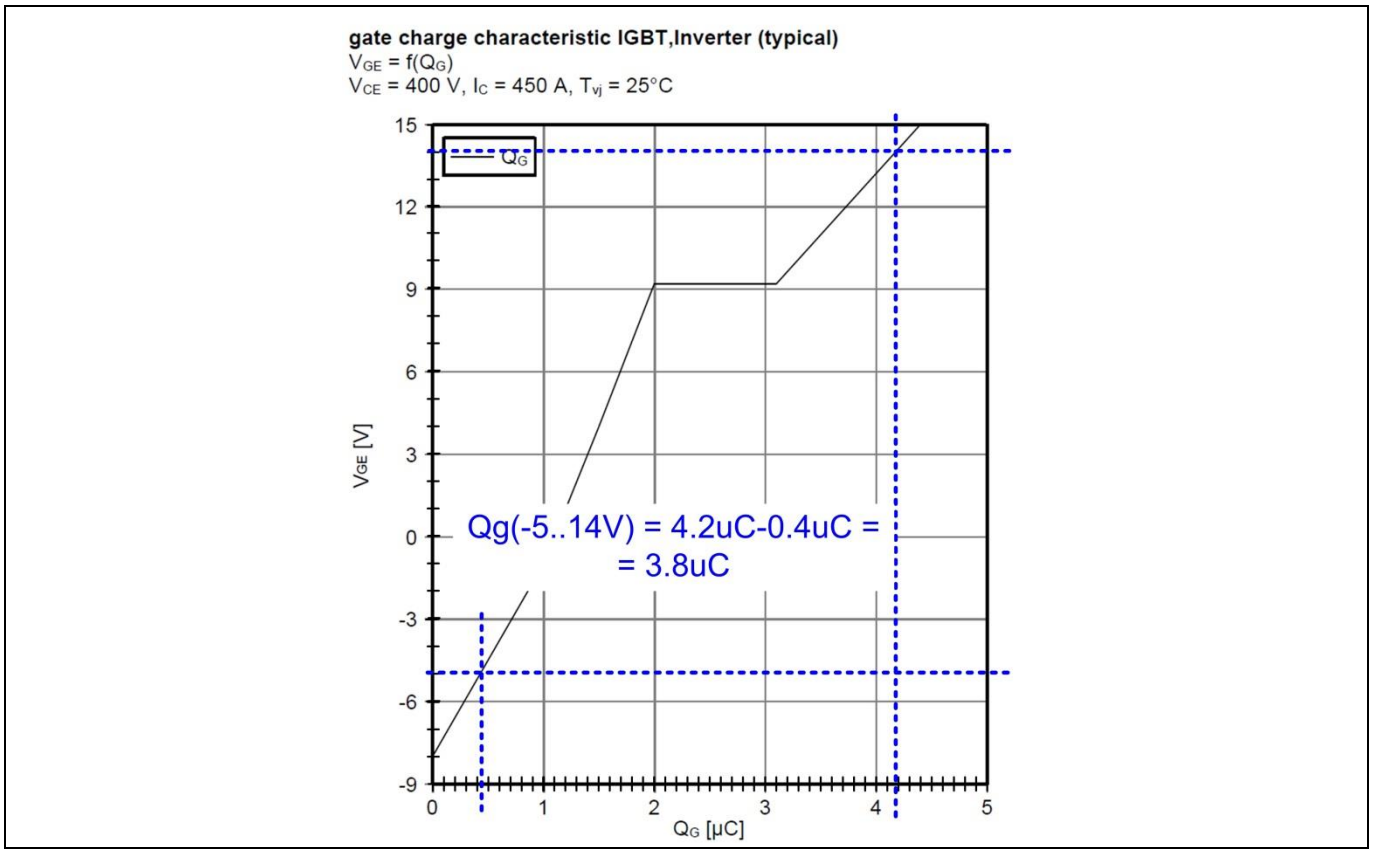

Figure 5 Example of Q_G for a different gate drive voltage based on the gate charge characteristics diagram.

3.1.4 Internal gate resistor (R_{Gint})

The value of the internal gate resistor give a useful information for calculating a theoretical gate drive peak current in the system:

$$I_{Gdr,peak} = \frac{V_{GE(on)} - V_{GE(off)}}{R_{Gext} + R_{Gint}} \quad (3.4)$$

In practice, this peak current will not be reached, because it is limited by stray inductances and non-ideal switching transitions of a real gate driving circuit.
Please also note that in case paralleled IGBTs are used inside of the power module, the datasheet value of the internal gate resistor has to be understood as the equivalent resistor of the total switch configuration. Knowing the number of chips (n) used in parallel it is possible to calculate the chip internal resistance with:

$$R_{Gint} = \frac{R_{Gchip}}{n} \quad (3.5)$$

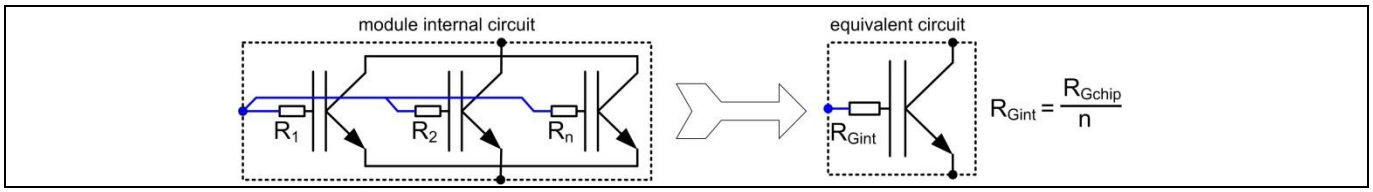

Figure 6 Example with n IGBT chips per switch paralleled in the module and the equivalent circuit with module R_{Gint}.

IGBT modules without an internal gate resistance (typically smaller IGBT sizes with lower 100A current rating) the R_{Gint} is specified with 0Ω. When such a configuration has to be paralleled it is mandatory to use a gate resistor for every individual IGBT chip in order to ensure a good dynamic current sharing during switching events and for avoiding oscillations in the system. Figure 7 shows such an application with externally paralleled IGBTs exemplarily. Please note that modules with an auxiliary/signal emitter pin may require additional individual resistances in the emitter connection for paralleling in order to avoid balancing currents in the signal emitter path.

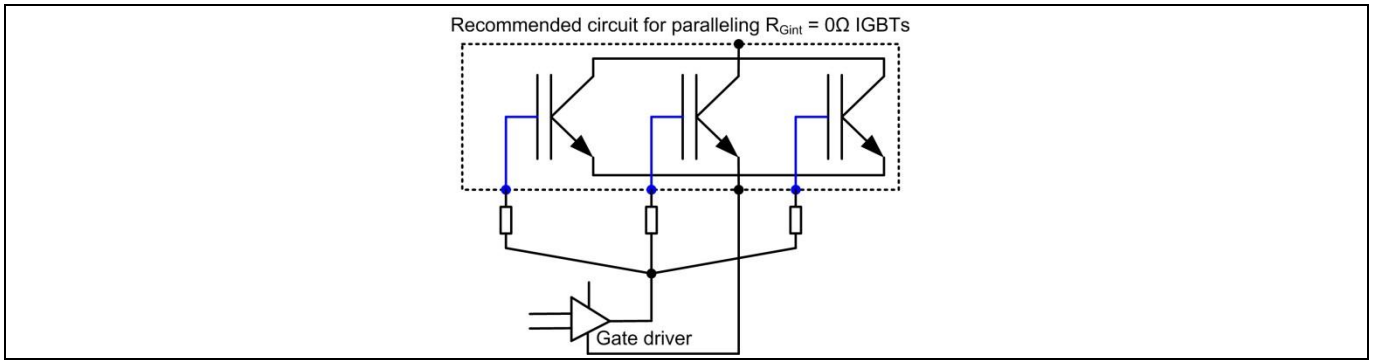

Figure 7 Example where IGBT chips without internal gate resistances are connected externally to a paralleled switch.

3.1.5 Parasitic capacitances (C_{ies}, C_{res}, C_{oes})

3.1.5.1 Circuit for measuring parasitic capacitances

According to IEC 60747 [1][2][3], the parasitic capacitances has to be measured in a single switch configuration (includes the antiparallel diodes for power module datasheets) and in steady state off condition (low amount of charge carriers in the channel and pn-junction).

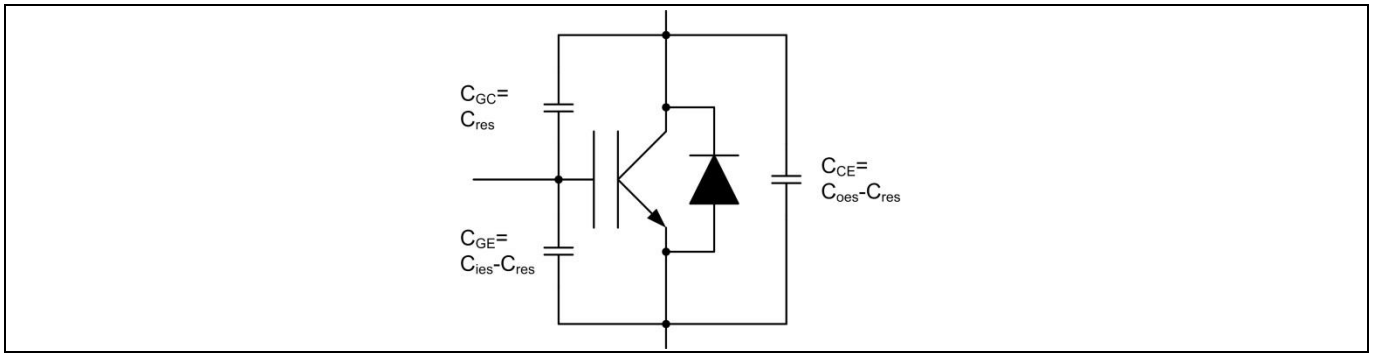

Figure 8 Parasitic capacitances of the single switch (IGBT + Diode).

Due to the measurement method, these values should not be used to simulate oscillation or EMI behavior as the real device condition with switching events and thus charge carriers in the device (i.e. tail and reverse recovery current) may lead to a very different behavior.
Nevertheless, the capacitance values characterized according to the standard can give a rough indication for susceptibility for parasitic turn-on events and are due to the standardized measurement method comparable with other devices and also from other manufacturers.
The parasitic capacitances furthermore strongly depend on the operating point of the IGBT (i.e. voltage dependent) which is also noted in the characteristic diagrams (capacity characteristic IGBT, Inverter(typical). In order to measure these capacitances at biased gate or collector-emitter voltages, following measurement circuits have to be applied:

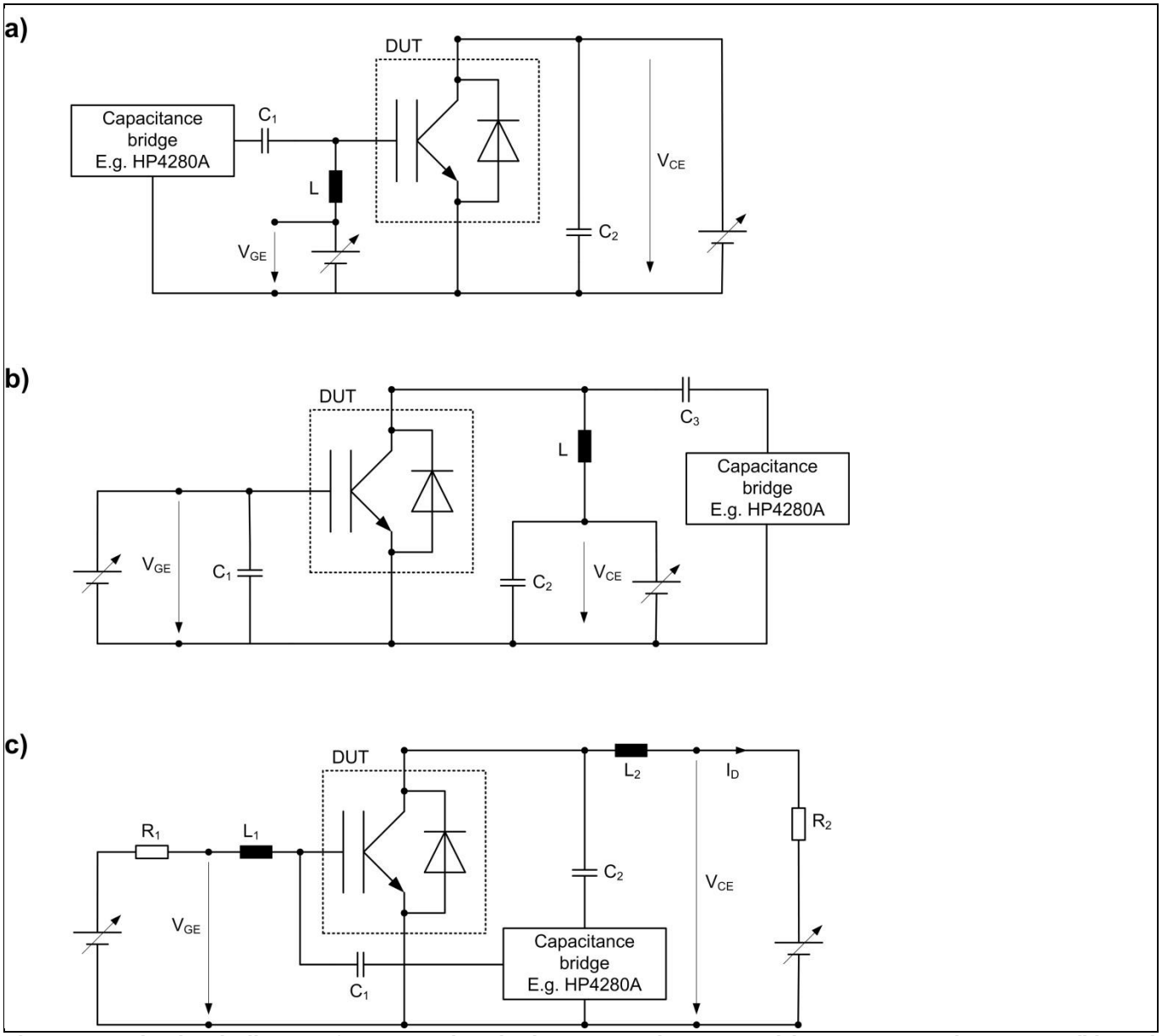

Figure 9 Basic circuit diagram for measuring the input capacitance C_{ies} (a), output capacitance C_{oes} (b), and reverse transfer capacitance C_{res} (c).

Input capacitance C_{ies} (Figure 9a):
The input capacitance C_{ies} is measured at a biased collector-emitter voltage. The values of the DC voltage across the gate-emitter and collector-emitter connections are specified with the test frequency. The capacitors C1 and C2 must form an adequate bypass at the test frequency. The inductors decouples the DC supply.

Output capacitance C_{oes} (Figure 9b):
The output capacitance C_{oes} is measured at biased collector-emitter voltages. The values of the DC voltage across the gate-emitter and collector-emitter connections are specified with the test frequency. The capacitors C_1, C_2 and C_3 must form an adequate bypass at the test frequency. The inductor L decouples the DC supply.

Reverse transfer capacitance C_{res} (Figure 9c):
The reverse transfer capacitance C_{res} is measured at a biased collector-emitter voltage. The values of the DC voltage across the gate-emitter and collector-emitter connections are specified with the test frequency. The capacitors C_1 and C_2 must form an adequate bypass at the test frequency. The inductors decouples the DC supply.

3.2 Switching Characteristics

The dynamic IGBT characteristic (i.e. switching characteristic of the device under test) depends on the device itself but it is also strongly dependent on the setup and its dynamic behavior. Due to the physical nature of all real parts, this dynamic behavior is always non-linear and especially at modern fast switching devices, the results can be strongly influenced by the surrounding environment. Therefore, basic information about the setup and the applied switching speed is noted in the datasheets.

Please be aware that using the same gate resistors in a final application is not the necessary and sufficient condition in order to achieve the same switching performance. The real switching speed is defined by dv/dt, di/dt values and is explained in the subsequent sections.

3.2.1 Turn-on delay time ($t_{d\,on}$), Rise time (t_r), Turn-on energy loss per pulse (E_{on})

The turn-on switching performance is characterized in a double pulse test bench with an inductive load. An example is shown in Figure 10a where the low side IGBT is the device under test. The Figure 10b show idealized the switching waveforms and Figure 10c in detail the definition of the datasheet values.

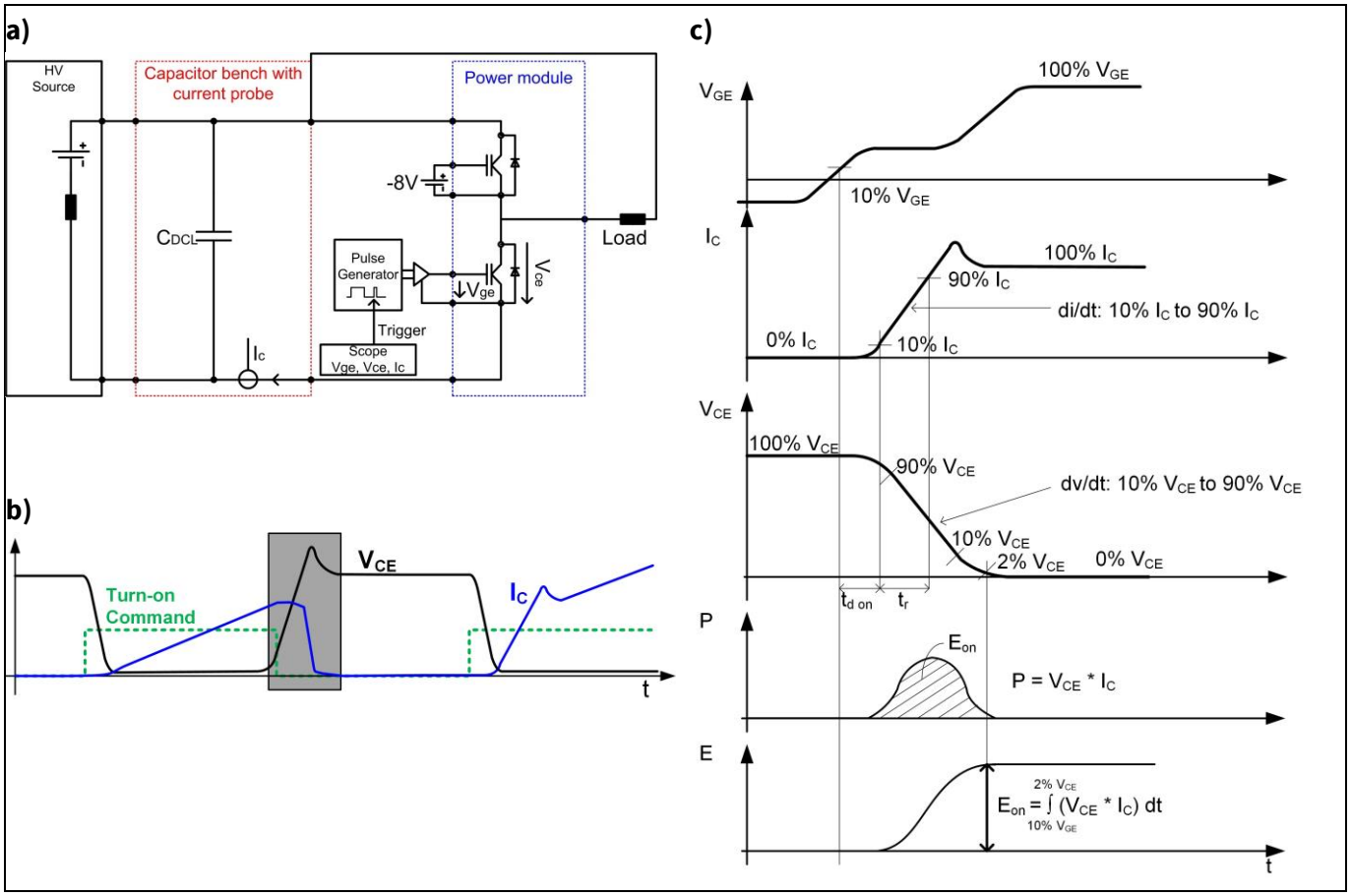

Figure 10 Test bench example for low side IGBT turn-on (a) corresponding waveform during double pulse testing (b) and nomenclature for datasheet values (c)[1].

The turn-on delay time defines the charging speed of the IGBT gate. This value depend on the characteristic of the IGBT gate driver and the gate charge characteristic of the module.

[1] the nomenclature is implemented for automotive IGBT power modules datasheets released in calendar year 2017 and later. Older Datasheets uses di/dt tangent between 50% Ic to Ic + 50% (Icmax - Ic) as well as an Eon integration from 10% Ic to 2% Vce.

Higher measured t_{don} time indicate that the project specific gate driver is charging the gate slower than the reference driver used for the datasheet characterization. When t_{don} time is much lower than expected the gate resistor has to be chosen higher (see also Figure 11 as an example).
It has to be noted that adjusting the gate resistor for same t_{don} time is still not the sufficient and necessary condition in order to get the same switching speed as non-linear behavior in gate drivers can lead to same t_{don} time but may still lead to different gate current during the switching event and finally to different switching energies.

The di/dt during the turn-on event defines the real switching speed of the IGBT (this value is noted for 150°C and also for 25°C room temperature in order to simplify investigations on the switching performance in a final application). At same stray inductance (L_s is the stray inductance in the test bench not in the module L_{sCE}!), the specified E_{on} switching losses will be achieved (see also Figure 11 as an example).

Please note that high bandwidth current probes with minimum delay are mandatory for measuring energy losses (e.g. Pearson current monitors). Parasitic capacitances in the load increase the turn-on switching losses.

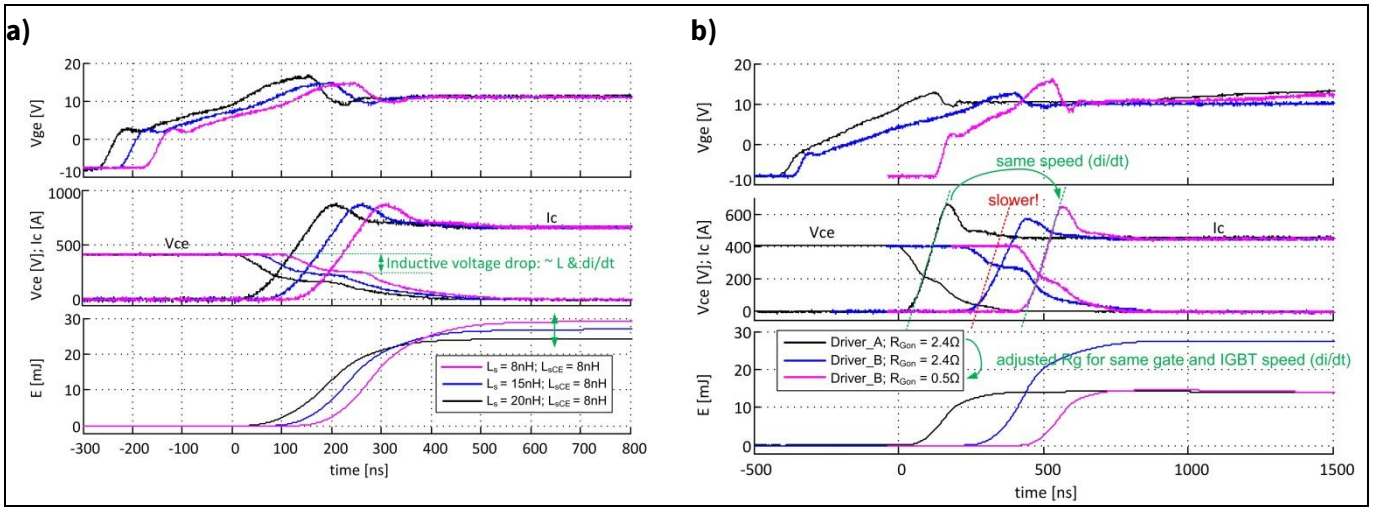

Figure 11 Turn-on with same module, driver and operating point but different setup stray inductance Ls (a). Same module, operating point, Ls but different gate driver circuits and Rg (b).

The Figure 11a shows a real switching example of the same module, same gate driver, same operating point but different stray inductances in the test setup varying from L_s = 8nH to 20nH. It can be seen that the initial V_{ce} drop, which is caused by di/dt as well as module and test bench stray inductance, influences the turn-on energy.
Lower system stray inductance leads to an increased turn-on loss because the effective voltage during the switching event is higher. With a higher total stray inductance the device is operated towards a soft turn-on transition with resulting low turn-on energies.

The Figure 11b shows an example of the same module, same operating point but different gate drivers were applied. The black and the blue waveform are with same gate resistors but leading finally to a total different behavior. The root cause is a different dynamic behavior of these two gate driver types.

The gate driver type B was used in combination with a different (lower) Rg and finally the module switches at the same turn-on speed and thus also at the same switching energies which can be seen in the comparison of black and magenta waveform in the Figure 11b.

3.2.2 Turn-off delay time ($t_{d\,off}$), Fall time (t_f), Turn-off energy loss per pulse (E_{off})

The turn-off switching performance is characterized similar to the turn-on event. The test-circuit principle is shown in Figure 12a. The low side IGBT is the device under test in this example. The Figure 8b shows idealized the switching waveforms and 8c in detail the definition of the datasheet values.

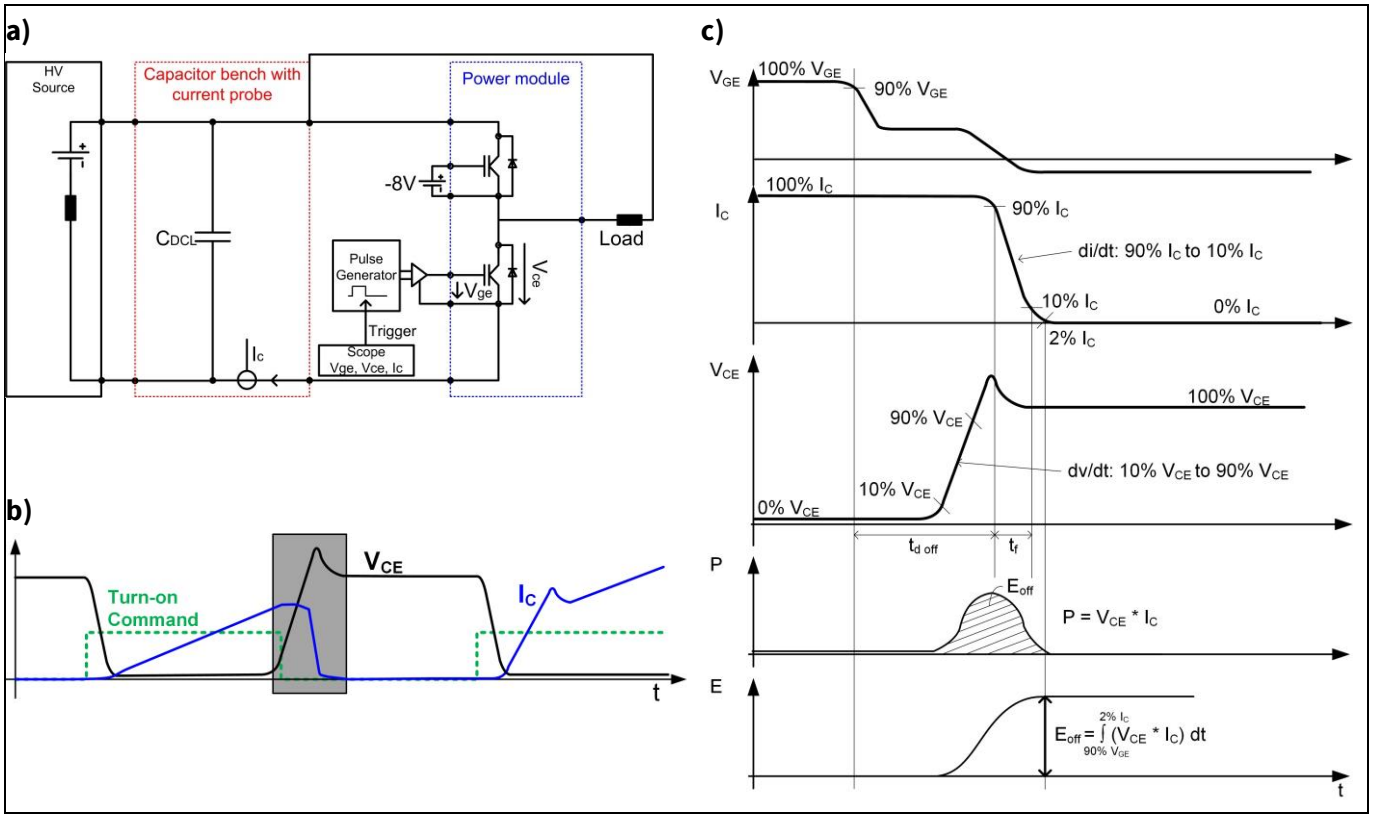

Figure 12 Test bench example for low side IGBT turn-off (a), corresponding waveform during double pulse testing (b), and nomenclature for datasheet values (c)[1].

The turn-off delay time defines the charging speed of the IGBT gate during the turn-off event (see also subsection 3.2.1 for discussion of different turn-off delay times).

The dv/dt and di/dt during the turn-off event defines the real switching speed of the IGBT (the dv/dt value is noted for 150°C and also for 25°C room temperature in order to simplify investigations on the switching performance in a final application). At equal setup stray inductance L_s (L_s is the stray inductance of the test bench not in the module L_{sCE}!) the specified E_{off} switching losses will be achieved.

Please note that high bandwidth current probes with minimum delay are mandatory for measuring energy losses (e.g. Pearson current monitors). Higher system stray inductance lead to increased turn-off losses and higher voltage overshoot. Parasitic capacitances in the load may affect the switching waveforms and lead to distortions of the di/dt, fall times. It has to be also noted that slightly modified turn-off losses can be observed when capacitive loads are switched.

[1] the nomenclature is implemented for automotive IGBT power modules datasheets released in calendar year 2017 and later. Older Datasheets uses an Eoff integration from 10% Vce to 2% Ic.

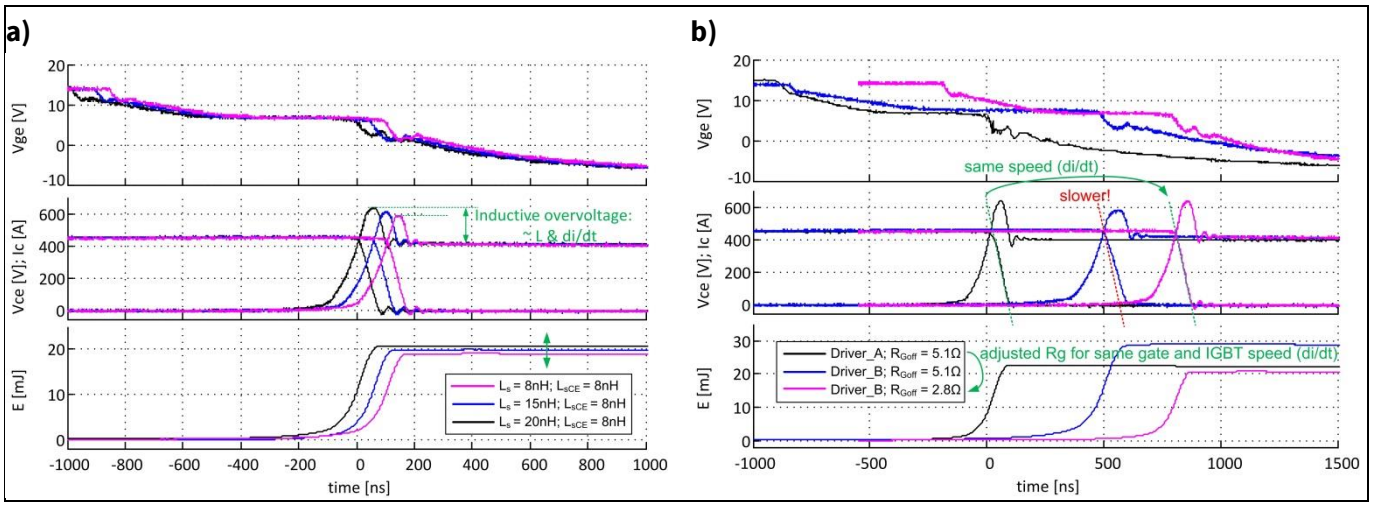

Figure 13 Turn-off with same module, driver and operating point but different setup stray inductance Ls (a). Same module, operating point, Ls but different gate driver circuits and Rg (b).

The Figure 13a shows a real switching of one module, same gate driver, same operating point but different stray inductances in the test setup varying from L_s = 8nH to 20nH. The surge voltage at the turn-off, which is caused by di/dt as well as module and test bench stray inductance (and also forward recovery of the diode), is affected by varying the stray inductances in the three different tests. Lower system stray inductance causes lower voltage overshoot and thus the IGBT can be utilized at higher working voltages at full switching speed. As noted widely in literature a low system stray inductance also supports low turn-off switching energy.

The Figure 13b shows an example of the same module, same operating point but different gate drivers were applied. The black and the blue waveform are with same gate resistances but leading finally to a total different behavior. The reason is a very different dynamic behavior of these two gate driver types. Nevertheless, the gate driver type B was finally applied with a different (lower) Rg and finally the module switches again at the same turn-off speed and thus also at the same switching energies.

3.3 Short Circuit Characteristics (I_{sc})

The short circuit characteristic strongly depends on application specific parameters like temperature, stray inductances, gate driving circuits and the resistance of the short circuit path. For device characterization, a test setup as shown in Figure 14a is used. One IGBT is short-circuited, while the other IGBT is driven with a single pulse (in this drawn example the low side IGBT). The corresponding voltage and current waveforms are illustrated in Figure 14b with corresponding nomenclature. The current in the conducting IGBT increases rapidly with a current slope that is depending on parasitic inductances and the DC-Link voltage. Due to desaturation of the IGBT, the current is only limited by the IGBT itself and the collector-emitter voltage remains on the high level. The chip temperature increases during this short circuit (far beyond the normal maximum allowed T_{vjop}) due to high currents and thus high energy dissipation. Because of the increasing chip temperature, the current decreases slightly while operating in short circuit condition. Within a defined short-circuit-withstand time t_P the IGBT has to be switched off to avoid a device failure.
Please note that the common failure mode is a thermal runaway, which means that the IGBT destruction may appear several milliseconds after it was turned-off in case the specification is exceeded. Please also note that the IGBT is heated in such a short circuit condition far above the allowed maximum operating junction temperature. It is mandatory to ensure a sufficient wait time after such an event (for cooling down the device to temperature lower than the maximum allowed temperature). A safe wait time for cooling after a short circuit is about 1 second.

It has to be mentioned that most application relevant short circuits (short in motor winding, wrong control pattern,…) may lead to different waveforms with less energy dissipation in the IGBTs. When the IGBT is not driven in full desaturation mode (full voltage and short circuit current) the heat dissipation is much lower and thus the wait time after such an event can be chosen much shorter compared to the worst case consideration of the product datasheet.

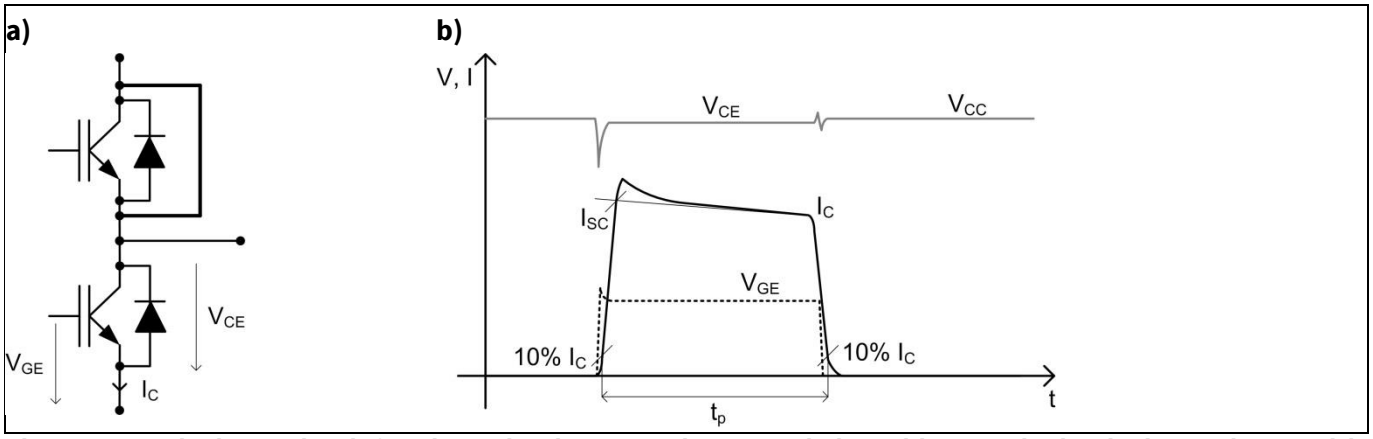

Figure 14 Typical test circuit for short circuit test. In the example low side IGBT is the device under test (a). Measurement description for datasheet values with idealized short circuit waveform (b).

A short circuit according to the definition in the datasheet is a special operation where the inverter system is already in a failure mode. It is assumed that such events are not switched more than 1000 times over lifetime.

3.4 Thermal Characteristics (R_{thJF}, Z_{thJF})

Most of the high power automotive IGBT modules are direct fluid cooled (e.g. via PinFin baseplate). This allows specifying the thermal resistance from junction to cooling fluid under consideration of a reference cooler shape. For power modules without direct fluid cooling (indirect cooled) a major part of the thermal resistance is defined by the customer specific thermal stack and thus it is important to merge the cooler stack model with the module thermal stack. More information for indirect cooled modules can be found in the application note [7].

Directly fluid cooled modules are characterized with a reference cooling circuit as noted in the datasheet. The temperature of the cooling fluid (T_F) is measured at the cooler inlet side (see Figure 15a). The device under test (in this example the three high-side IGBTs in the center which form one switch) is powered and thus generating heat. The junction temperature is measured indirectly via the pn-junction voltage drop (i.e. T_{vj}). Knowing the dissipated power (P) the thermal resistance of this switch is defined by:

$$R_{thJF} = \frac{T_{vj} - T_{Finlet}}{P} \quad (3.6)$$

Please note that the defined Rth nomenclature according to AQG 324 [4] with $R_{thJF} = \frac{T_{vj} - \left(\frac{T_{Finlet} + T_{Foutlet}}{2}\right)}{P}$ leads to reduced ΔT and thus better (i.e. lower) Rth values compared to using only inlet temperatures. Experience has shown that typical inverter projects specify the fluid temperatures of the cooler inlet only and thus the nomenclature of the IFX datasheets can be used much easier in practice.

The definition of the parameters are also exemplarily shown in Figure 15. In this example the IGBT power module consist of three IGBT chips in parallel per switch, which can be seen by the three hot areas in the IR-thermal picture. The T_{vj} is the temperature of the switch, which can be obtained by an indirect measurement via the pn-junction voltage drop.

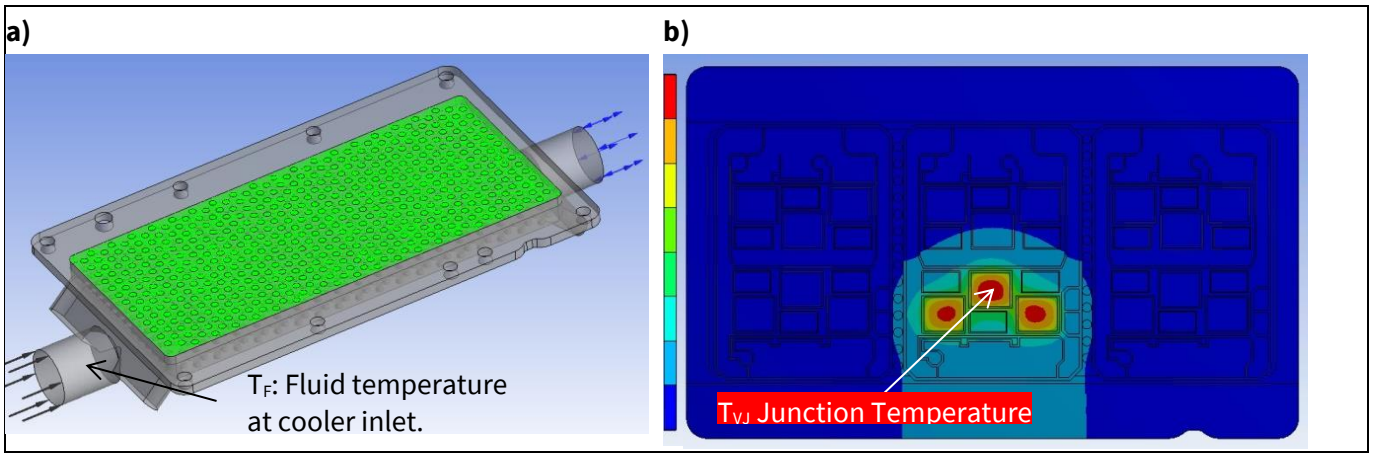

Figure 15 Definition of the datasheet thermal values. The cooling fluid temperature T_F is defined at cooler inlet (a). The T_{vj} of a switch is obtained indirect via pn-junction voltage drop measurement. Illustration of a thermal IR-picture during single switch IGBT power (b).

The transient thermal impedance is specified with Foster-Model as shown in Figure 16. The resistances and capacitances do not represent physical layers of the thermal stack. The parameters of a Foster model are curve fitted from measured and/or simulated thermal characteristics, where the capacitances can be calculated with:

$$c_i = \frac{r_i}{\tau_i} \quad (3.7)$$

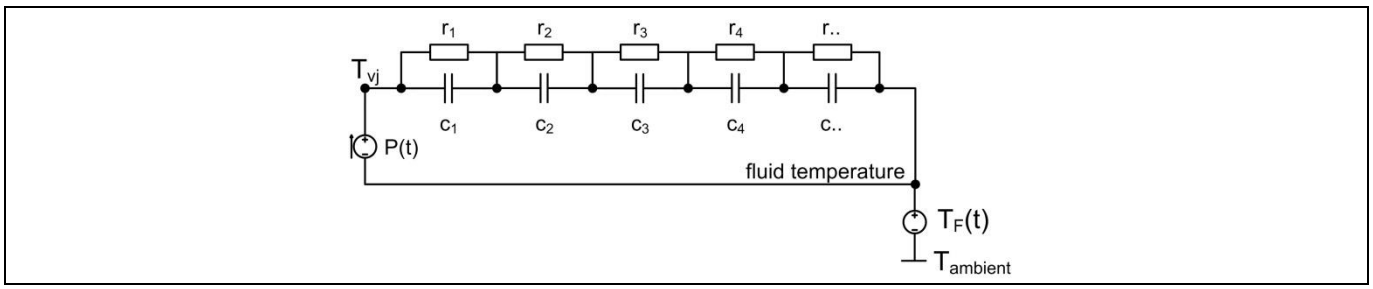

Figure 16 Thermal equivalent model (Foster model).

The parameters of the typical 3rd to 5th order Foster Models are noted in the product datasheets within the diagram section of the transient thermal impedances.

The transient thermal characteristics can be easily calculated at a specific time point with equation:

$$Z_{thJF}(t) = \sum_{i=1}^{n} r_i \cdot \left(1 - e^{-\frac{t}{\tau_i}}\right) \quad (3.8)$$

Having a power dissipation profile of the IGBT switch, the junction temperature can be calculated in dependence of the cooling fluid temperature and the transient thermal impedance:

$$T_{vj}(t) = P(t) \cdot Z_{thJF}(t) + T_F(t) \quad (3.9)$$

The dependence of the cooling fluid flow rate on the thermal impedance is also shown in the diagram section. With this information, it is also possible to estimate the transient thermal impedance as a function of the cooling fluid flow rate (ΔV/Δt).

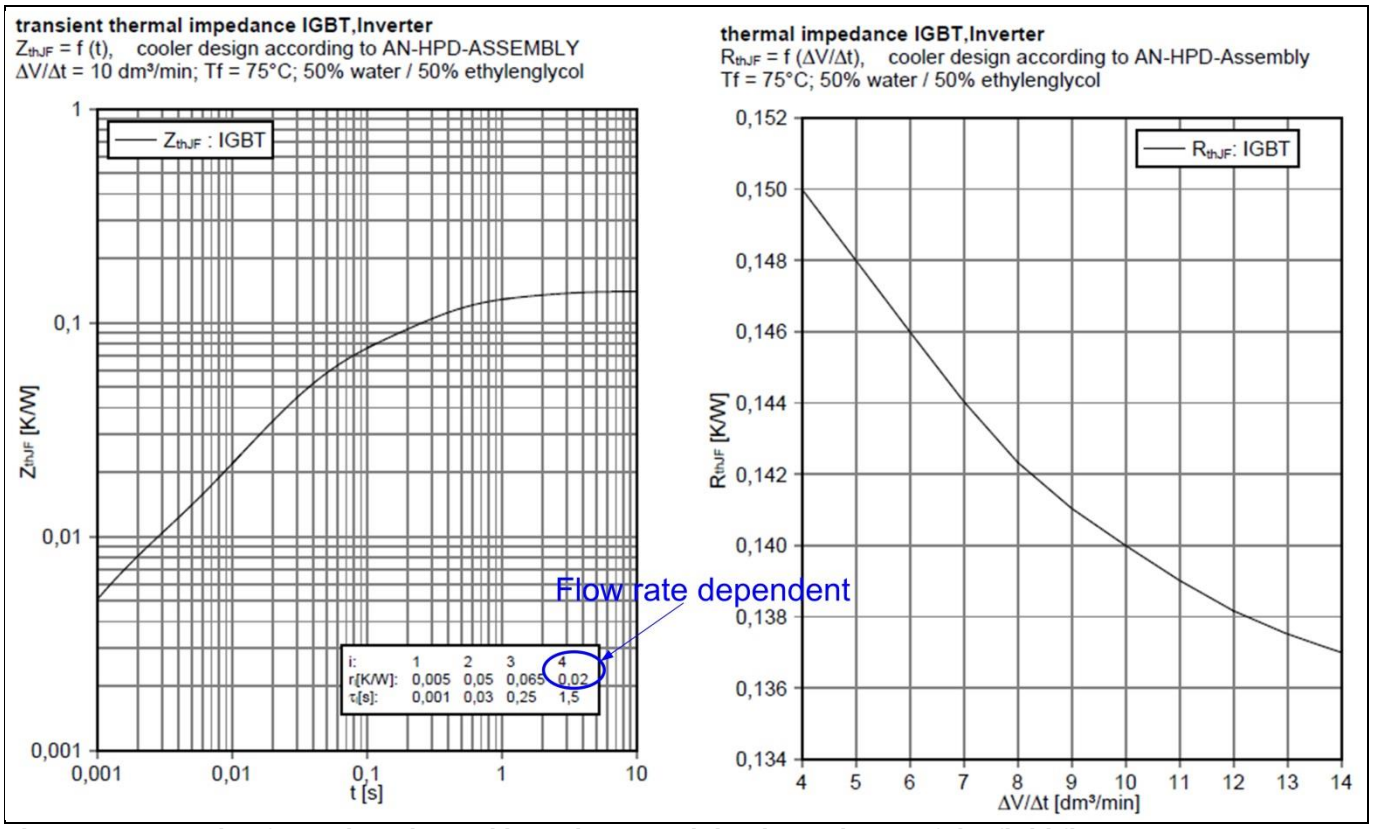

Figure 17 Example of transient thermal impedance and the dependence of the fluid flow rate.

The cooling fluid flow rate has nearly no impact on short times but mainly influences the thermal resistance of the longest time constant. The resistance can thus be estimated as a function of the flow rate with:

$$r_n(\Delta V/\Delta t) \approx R_{thJF}(\Delta V/\Delta t) - \sum_{i=1}^{n-1} r_i \quad (3.10)$$

With the equations above it is possible to build a thermal model parametrized for different cooling fluid flow rates. Figure 18 shows an example how these two datasheet plots can be used to derive the flow rate dependency. Figure 18a and b show the typical datasheet plots. In Figure 18b the simple calculation for the resistance with the highest time constant is exemplarily noted (r_4 in this example). Keeping the r_1 to r_3 constant while using the flow rate dependent r_4 in Figure 18c shows the transient thermal behavior at different cooling conditions.

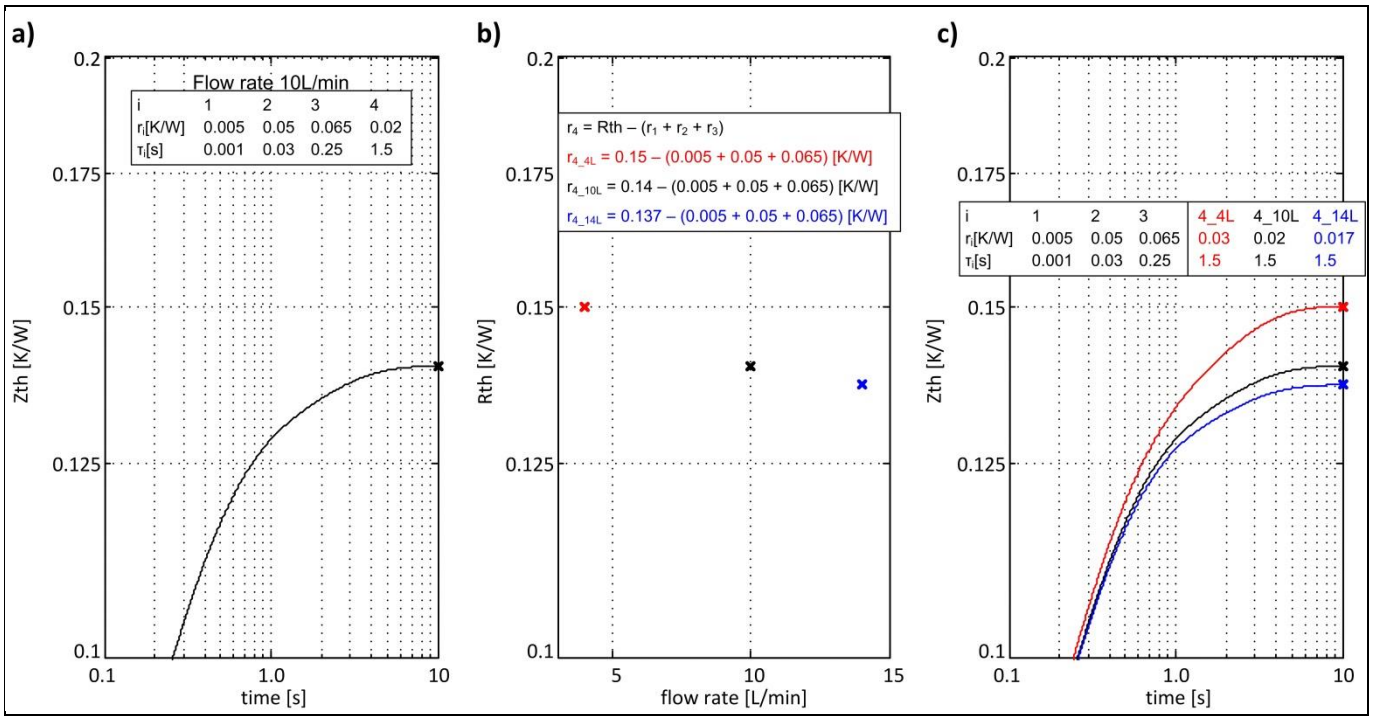

Figure 18 Example of transient thermal impedance at nominal cooling flow rate (a). The steady state thermal resistance at different cooling flow rates (b). Plotted transient thermal impedance with r_n scaled depending on flow rate (c).

The module dissipated power is stored as heat energy in the cooling fluid. Consequently, the lateral heating of the cooling fluid can be calculated in general as a function of the thermal heat capacitance of the cooling fluid and the flow rate:

$$\Delta T_{fluid} = \frac{P_{loss}}{v \cdot c \cdot d} \quad (3.11)$$

For typical 50% water/50% ethylenglycol fluid data based on [10], the lateral heating of the cooling fluid can be estimated with:

$$\Delta T_{fluid} \approx \frac{P_{loss}[W]}{\frac{v[L/min]}{60} \cdot 3370 \left[\frac{\frac{J}{kg}}{K}\right] \cdot \frac{1.06kg}{L}} \quad (3.12)$$

3.5 Temperature under switching conditions ($T_{vj\,op}$)

The $T_{vj\,op}$ specifies the allowed temperature of the chipset under normal switching operation.

Some products of the HybridPACK™ module family, like the HybridPACK™ Drive, specify a short-time extended operation temperature above the continuous rating. This rating is useful for occasionally events like severe motor hill hold conditions under high cooling temperature (or high load currents with low cooling flow rate). Such occasionally extreme events are typically not considered in driving cycles / mission profiles but are defined as worst case operating points in the inverter specification. In order to support best the inverter dimensioning the short-time extended operation temperature area is defined with an occurrence maximum of x times over lifetime. This means that the power module robustness is designed to withstand the normal $T_{vj\,op}$ over the entire

application lifetime and in addition x events are allowed exceeding the continuous operation area for a specified time.

4 Diode, Inverter Maximum Rated Values

3 Diode, Inverter

3.1 Maximum Rated Values

Parameter	Conditions	Symbol	Value	Unit
Repetitive peak reverse voltage	T_{vj} = 25°C	V_{RRM}		V
Implemented forward current		I_{FN}		A
Continuous DC forward current		I_F		A
Repetitive peak forward current	t_P = 1 ms	I_{FRM}		A
I^2t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = °C	I^2t		A^2s

Figure 19 Diode maximum rated values (template).

4.1 Repetitive peak reverse voltage (V_{RRM})

Module configurations designed for switching inductive loads have freewheeling diodes. They have to block same voltage as the IGBTs and thus the repetitive peak reverse voltage (V_{RRM}) is the same as the allowed collector-emitter voltage (V_{CES}). Due to the fixed antiparallel implementation in the module configuration, they are also tested at the same test steps. Unless otherwise noted, the allowed collector-emitter voltage chart over temperature can be also applied to the diode and the diode V_{RRM} is equal to IGBT V_{CES} rating.

4.2 Implemented forward current (I_{FN})

Similar as for the IGBT, this value without temperature conditions has no technical meaning and is used only for the type designation of the power module (i.e. for the product name).

4.3 Continuous DC forward current (I_F)

The continuous DC forward current of the diode can be calculated similar to the IGBTs:

$$I_F = \frac{T_{vjop\,max} - T_F}{R_{thJF\ Diode\ max} \cdot V_{F\,max}(I_F, T_{vj})} \quad (4.1)$$

In most cases, the continuous DC forward current is rated equal to the IGBT, which simply mean that the diode size matches the IGBT size for target applications.

4.4 Repetitive peak forward current (I_{FRM})

The repetitive peak forward current is in theory derived from the feasible power dissipation and the thermal impedance Z_{th}, but would then neglect other failure mechanism like bond wires, overvoltage, etc.
The datasheet value specifies this repetitive forward current considering all practical limitations of the power module. Up to I_{FRM} a switching operation of the diode is allowed. Each Infineon automotive power module is tested in a diode SOA test (Diode turn-off test) minimum at the specified I_{FRM} value using its complementary IGBT in the half-bridge as commutation switch.

4.5 I^2t - value (I^2t)

The I^2t value specifies the surge current capability of the diode for non-switching application. This diode rating is quite similar to IGBT short circuit ratings. Figure 20 show a test bench example. A half-sine pulse current source is connected to the inverter phase node. The Inverter DC+ and DC- terminals are shorted in this test (i.e. equivalent to a capacitor with infinite capacitance value). The high-side or low-side diodes are stressed depending on the current flow direction of the current source (example show high-side diode conduction).
The half-sine current pulse is injected with single pulse sequence. The diode is in a non-switching operation. The diode will be heated during this pulse event beyond its allowed maximum operating junction temperature, which is similar to IGBT short circuit condition. After each current pulse, a cool down (wait time) is mandatory in order to ensure that the diode is again within the allowed junction temperature range before continuing the switching operation. The recommended wait time is about 1 second.

The peak current value within the half-sine pulse current can be calculated with:

$$I^2t = \int_0^{10ms} I^2(t) \cdot t \, dt = \frac{1}{2} \cdot {I_{FSM}}^2 \cdot 10ms \quad (4.2)$$

$$I_{FSM} = \sqrt{\frac{2 \cdot I^2t}{10ms}} \quad (4.3)$$

For shorter times higher peak currents are possible (up to the rated short circuit current of the module I_{SC}). For longer times the current decreases till the continuous current rating of the diode is achieved.

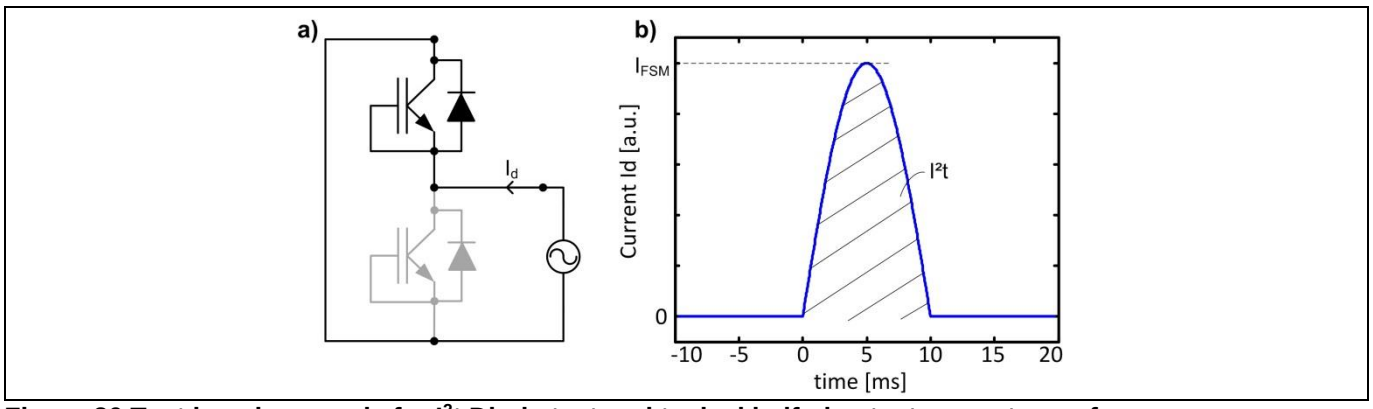

Figure 20 Test bench example for I^2t Diode test and typical half-sine test current waveform.

5 Diode, Inverter Characteristic Values

3.2 Characteristic Values

			min.	typ.	max.	
Forward voltage	I_F = A, V_{GE} = 0 V I_F = A, V_{GE} = 0 V I_F = A, V_{GE} = 0 V I_F = A, V_{GE} = 0 V I_F = A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 150°C T_{vj} = 175°C T_{vj} = 25°C T_{vj} = 175°C	V_F				V
Peak reverse recovery current	I_F = A, - di_F/dt = A/µs (T_{vj} = 150°C) V_R = V V_{GE} = -8 V	T_{vj} = 25°C T_{vj} = 150°C T_{vj} = 175°C	I_{RM}				A
Recovered charge	I_F = A, - di_F/dt = A/µs (T_{vj} = 150°C) V_R = V V_{GE} = -8 V	T_{vj} = 25°C T_{vj} = 150°C T_{vj} = 175°C	Q_r				µC
Reverse recovery energy	I_F = A, - di_F/dt = A/µs (T_{vj} = 150°C) V_R = V V_{GE} = -8 V	T_{vj} = 25°C T_{vj} = 150°C T_{vj} = 175°C	E_{rec}				mJ
Thermal resistance, junction to cooling fluid	per diode; $\Delta V/\Delta t$ = 10 dm³/min, T_F = °C		R_{thJF}				K/W
Temperature under switching conditions	t_{op} continuous for 10s within a period of 30s, occurence maximum times over lifetime		$T_{vj\,op}$	-40 150		150 175	°C

Figure 21 Diode characteristic values.

5.1 Forward Voltage (V_F)

The diode forward voltage characteristic (V_F) depends on the applied current (I_F), junction temperature (T_{vj}) as well as the implemented chip size and its chip technology.

Power module datasheets specifies in general the chip values for (V_F) as this is the most relevant parameter for calculating chip power losses and temperatures via the chip thermal resistance (Rth).
When the voltage drop is measured over the power tabs it is normal that higher values than the chip only values are obtained because the voltage drop of the package resistance ($R_{CC'EE'}$) is included in the measurement.

Most product datasheets with EDT2 IGBTs notes two different operating points for V_F. This simplifies the data extraction for linearized simulation models, which uses V_{f0} (i.e. voltage drop across the pn-junction) and R_d (i.e. resistance part of the device) as a behavioral model. When only a single operating point is specified in the numeric table of the datasheet, the corresponding values can also be obtained in the diagram section under the Diode forward characterisitcs. In following these two V_F operation points are noted as "_low" and "_high". With the two operating points (I_{F_low}, V_{F_low} & I_{F_high}, V_{F_high}) the linearized model can be simply calculated with:

$$R_d = \frac{V_{F\_high} - V_{F\_low}}{I_{F\_high} - I_{F\_low}} \quad (5.1)$$

$$V_{f0} = V_{F\_low} - \left(r_d * I_{F\_low}\right) \quad (5.2)$$

Diode, Inverter Characteristic Values

The following table and calculation provides an example:

Parameter	Conditions	Value
Diode V_F	I_F = **450A (I_{F_low})** T_{vj} = 25°C	**V_{F_low} = 1.40V**
Diode V_F	I_F = **820A (I_{F_high})** T_{vj} = 25°C	**V_{F_high} = 1.65V**
Diode V_F	I_F = **450A (I_{F_low})** T_{vj} = 175°C	**V_{F_low} = 1.2V**
Diode V_F	I_F = **820A (I_{F_high})** T_{vj} = 175°C	**V_{F_high} = 1.55V**

$$R_{d\_25°C} = \frac{1.65V - 1.40V}{820A - 450A} \approx 0.68m\Omega \;; \quad V_{f0\_25°C} = 1.40V - (0.68m\Omega * 450A) \approx 1.1V$$

$$R_{d\_175°C} = \frac{1.55V - 1.2V}{820A - 450A} \approx 0.95m\Omega \;; \quad V_{f0\_175°C} = 1.2V - (0.95m\Omega * 450A) \approx 0.77V$$

5.2 Diode switching characteristics, turn-off (I_{RM}, Q_{RM}, E_{rec})

The dynamic diode characteristic (i.e. switching characteristic of the device under test) depends on the device itself, the complementary switch (i.e. the IGBT in the module) and thus it is also strongly dependent on the setup. The complementary part (i.e. the high-side IGBT for the low-side diode and the low-side IGBT for the high-side diode) is defined by the product itself and the internal IGBTs are used as test-switches. This is different to stand-alone diodes, which are characterized by means of external reference switches.
In a power module configuration with antiparallel diodes the IGBTs are commutating the diodes. Please note that the considerations of IGBT switching speed (see section 3.2) can be transferred also to the diode switching speed (i.e. IGBT turn-on speed ≈ Diode turn-off speed).

In general: Slower IGBT turn-on leads to slower diode turn-off speed ($-di_F/dt$) resulting in lower reverse recovery peak (I_{RM}), lower reverse recovery charge (Q_{RM}) and also lower reverse recovery energy (E_{rec}).

The diode turn-off switching performance is characterized in a double pulse test bench with an inductive load. Figure 22a shows an example a low-side diode under test. The high-side IGBT is the test switch. The Figure 22b show idealized the switching waveforms and Figure 22c in detail the definition of the datasheet values.

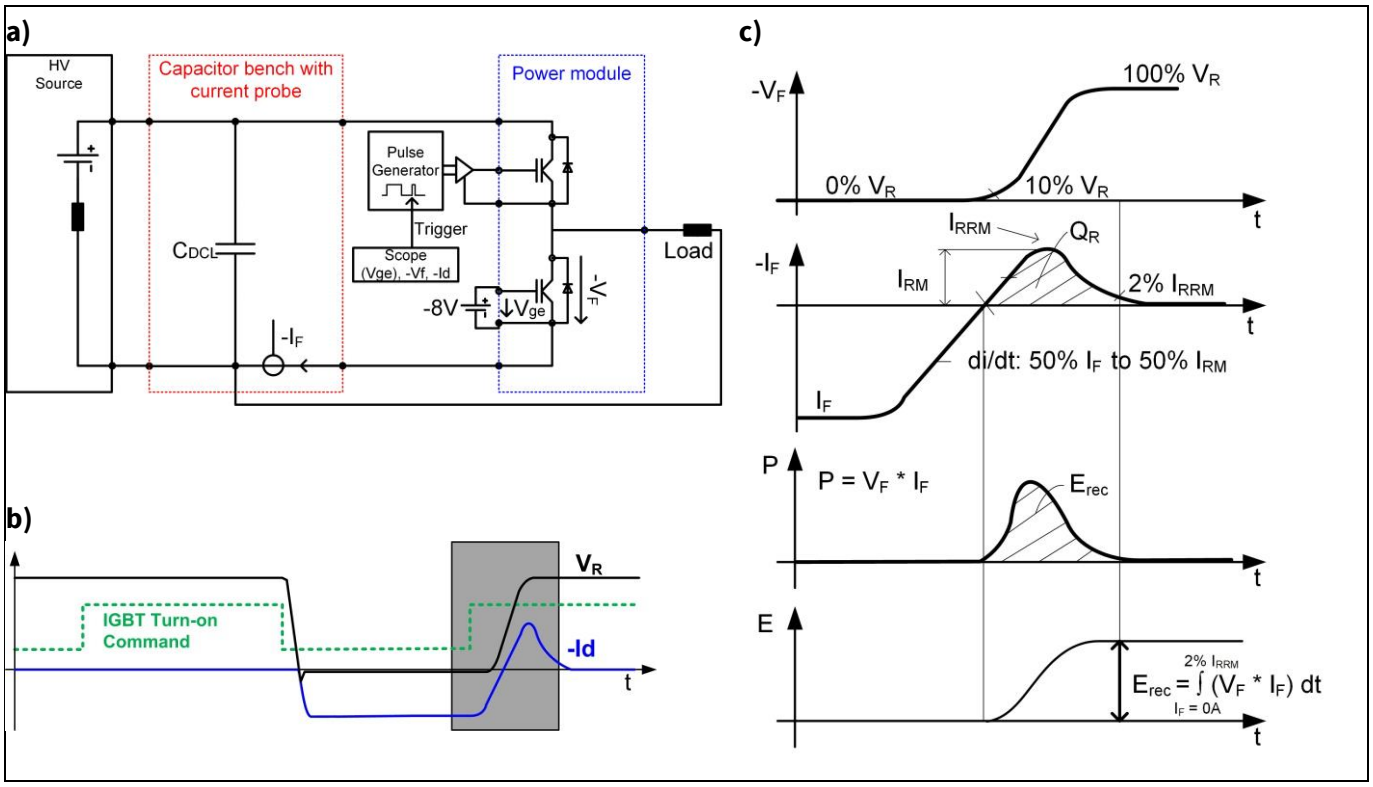

Figure 22 Test bench example for low side Diode turn-off (a) corresponding waveform during double pulse testing (b) and nomenclature for datasheet values (c)[1].

Please note that high bandwidth current probes with minimum delay are mandatory for measuring energy losses (e.g. Pearson current monitors). Lower system stray inductance typically lead to reduced diode turn-off losses. Parasitic capacitances in the load decrease the diode turn-off switching losses.

The influence of different gate driver types and setup stay inductances on the switching characteristic is explained in section 3.2.1 more detailed.

[1] the nomenclature is implemented for automotive IGBT power modules datasheets released in calendar year 2017 and later. Older Datasheets uses an Erec integration from 10% Vr to 2% Irm.

5.3 Thermal resistance (R_{thJF}, Z_{thJF})

The thermal resistance and transient thermal characteristics of the diode is rated in the same way as the IGBT. The only difference is that the power is dissipated by the diode and the temperature difference is defined by the diode junction temperature to the cooling fluid temperature at the cooler inlet. Please refer to section 3.4 for more detailed information.

5.4 Temperature under switching conditions ($T_{vj\,op}$)

The allowed $T_{vj\,op}$ for the diode is specified same way as for the IGBT. Please see section 3.5 for more information.

6 NTC-thermistor

The NTC-thermistor (negative temperature coefficient resistor) is placed on the substrate top side close to the chipset and can be used for temperature monitoring. A common approach is to estimate roughly the chip temperature in steady state from the NTC temperature response, which can be used for basic fault detection algorithms. As an example, the temperature delta between different NTCs in the power module or an unexpected high rising temperature slope of the NTC can indicate an unexpected drop of the cooling fluid flow rate or a missing cooling fluid. It has to be noted that the NTC temperature response is not adequate for measuring fast variation of the chip temperature e.g. in short circuit conditions. Nevertheless, power modules with baseplates have a quite high thermal mass sufficient to store the chip dissipated power in the baseplate heat capacitance for a short time of operation (up to several seconds). The NTC circuit and basic fault detection algorithms have enough time to react on severe fault conditions like a missing cooling fluid.

6.1 NTC resistance and power dissipation (R_{25}, $\Delta R/R$, P_{25})

The resistance of the NTC-thermistor R_{NTC} depend on its temperature T_{NTC} and can be approximated with:

$$R_{\mathrm{NTC}}[\Omega] = \mathrm{R}_{25} \cdot exp^{B\cdot\left(\frac{1}{273.15K+T_{NTC}[°C]}-\frac{1}{298.15K}\right)} \quad (6.1)$$

The resistance at room temperature (R_{25}) and the B values are specified in the datasheet. The equation can be solved to the temperature as follows:

$$T_{NTC}[°C] = \frac{1}{\frac{log\left(\frac{R_{NTC}}{R_{25}}\right)}{B}+\frac{1}{298.15K}} - 273.15K \quad (6.2)$$

The maximum relative deviation of the resistance is defined at a temperature of 100°C (see $\Delta R/R$ value in the datasheet). In order to avoid self-heating of the NTC, the power dissipation has to be limited. The power dissipation, which heat up the NTC of 1 K is specified in the datasheet (see P_{25}). With this value the maximum allowed current through the NTC can be calculated with:

$$I_{NTC\ max} = \sqrt{P_{25}/R_{NTC}} \quad (6.3)$$

6.2 B-value ($B_{25/50}$, $B_{25/80}$, $B_{25/100}$)

The B value is required to solve the equations for NTC resistance and temperature calculations. The B-value itself depends on the considered temperature range. Typically, a range of 25 to 100 degree Celsius is of interest and thus $B_{25/100}$ has to be used. In case a lower temperature range is in focus, the B-values $B_{25/80}$ (for 25 to 80°C) or $B_{25/50}$ (for 25 to 50°C) can be used, which leads to more accurate calculation based on this curve fitting.
The typical characteristics (not the curve fitted values) over temperature can be found in the diagram sections of the datasheet.

7 Datasheet parameters Module

5 Module

Parameter	Conditions	Symbol	Value			Unit
			min.	typ.	max.	
Isolation test voltage	RMS, f = Hz, t = sec	V_{ISOL}				kV
Material of module baseplate						
Internal isolation	basic insulation (class 1, IEC 61140)					
Creepage distance	terminal to heatsink terminal to terminal	d_{Creep}				mm
Clearance	terminal to heatsink terminal to terminal	d_{Clear}				mm
Comperative tracking index		CTI				
Pressure drop in cooling circuit	$\Delta V/\Delta t$ = 10.0 dm³/min; T_F = 75°C	Δp				mbar
Maximum pressure in cooling circuit	$T_{baseplate}$ < °C $T_{baseplate}$ > °C (relative pressure)	p				bar
Stray inductance module		L_{sCE}				nH
Module lead resistance, terminals - chip	T_F = 25 °C, per switch	$R_{CC'+EE'}$				mΩ
Storage temperature		T_{stg}				°C
Mounting torque for modul mounting	Screw M baseplate to heatsink Screw EJOT Delta PCB to frame	M				Nm
Weight		G				g

Figure 23 Module characteristic values (template).

7.1 Insulation test voltage (V_{ISOL})

The insulation of all terminals (connected together) to the baseplate is designed to achieve the basic isolation according to IEC 61140 [5]. The test voltage can be applied with a DC (i.e. f = 0 Hz) or with an AC source of f = 50..60 Hz. Important is that the same peak voltage for DC or AC measurement method is applied:

$$V_{ISOL\_DC} = V_{ISOL\_AC} \cdot \sqrt{2} \quad (7.1)$$

Furthermore, the test voltage can be applied in a 60 seconds or in 1 second routine test with the following dependency (see e.g. UL 1557 [6] for reduction of routine test times):

$$V_{ISOL\_1s} = V_{ISOL\_60s} \cdot 120\% \quad (7.2)$$

The rated test voltage in the datasheet is tested before and after reliability tests of the power module and is furthermore part of failure criteria of such stress tests.

The insulation between NTC and other connectors is tested at the same conditions if not otherwise noted. In case of failures (e.g. the gate driving circuit) a conducting path can be formed by moving bond wires that change their position during the failure event or by a plasma path forming as a consequence of arcing during failure. Therefore, additional isolating barriers externally on the gate driver board is recommended for the NTC measurement.

7.2 Clearance, Creepage distance (d_{Creep}, d_{Clear}) and tracking (CTI)

In automotive high voltage systems it is important not to have a breakdown, arcing and/or too high leakage currents between two conductive parts with different voltage potential. The isolation test voltage already described the characteristics between the low voltage and the high voltage part. But it is also mandatory to specify in general the distances between to conductive parts with different voltage potential and the material properties of the insulating part on component level.

The clearance distance (d_{Clear}) specifies the shortest distance in air between two conductive parts of different voltage potential >60V. This value includes high voltage signal & load terminals to the baseplate distance and on the high voltage side parts with different voltage like collector to emitter path.

The creepage distance (d_{Creep}) specifies the shortest tracking path between two conductive parts of different voltage potential >60V. Similar to clearance distance this includes high voltage terminals to the baseplate and high voltage to high voltage paths.

The comparative tracking index is a performance value of insulating materials under test conditions defined in the IEC 60112. It gives a quantitative comparison of isolation materials. The higher the number the better the insulation characteristics whereby low CTI values can be compensated by larger creepage distances (see also IEC60664-1 for more information).

7.3 Pressure drop and maximum pressure (Δp, p)

The characteristic pressure drop (Δp) in the cooling circuit of direct fluid cooled modules is an important parameter for the design of the cooling system especially for the cooling pump. This pressure drop is given for typical cooling conditions and the reference cooler shape, which is specified in the assembly/mounting instructions of the corresponding product family.
The specified maximum pressure in a cooling circuit (p) must never been exceeded, even for test procedures! Exceeding the maximum pressure may bend the baseplate and the risk is a leakage of the cooling circuit and/or damage of the insulation parts.
All pressure values are specified as relative values to atmospheric pressure.

7.4 Module stray inductance (L_{sCE})

Stray inductances lead to transient voltages during the switching events and limit due to the surge voltage in the turn-off events the useable working voltages for a given switching speed. The transient voltage due to stray inductances can be calculated in general with:

$$\Delta V = L \cdot \frac{di}{dt} \quad (7.3)$$

It has to be noted that also stray inductances in the system (capacitor, busbar, etc.) contribute to these transient voltages besides the stand-alone module stray inductance (L_{sCE}). As a result, the entire system stray inductances have to be low enough in order not to exceed the maximum allowed collector-emitter voltage during the turn-off transitions.

A simplified equivalent circuit of the module stray inductances is shown in Figure 24. The stray inductance of the module is the sum of stray inductances of one phase-leg between the power terminals:

$$L_{sCE} = L_{11} + L_{12} + L_{13} + L_{14} \quad (7.4)$$

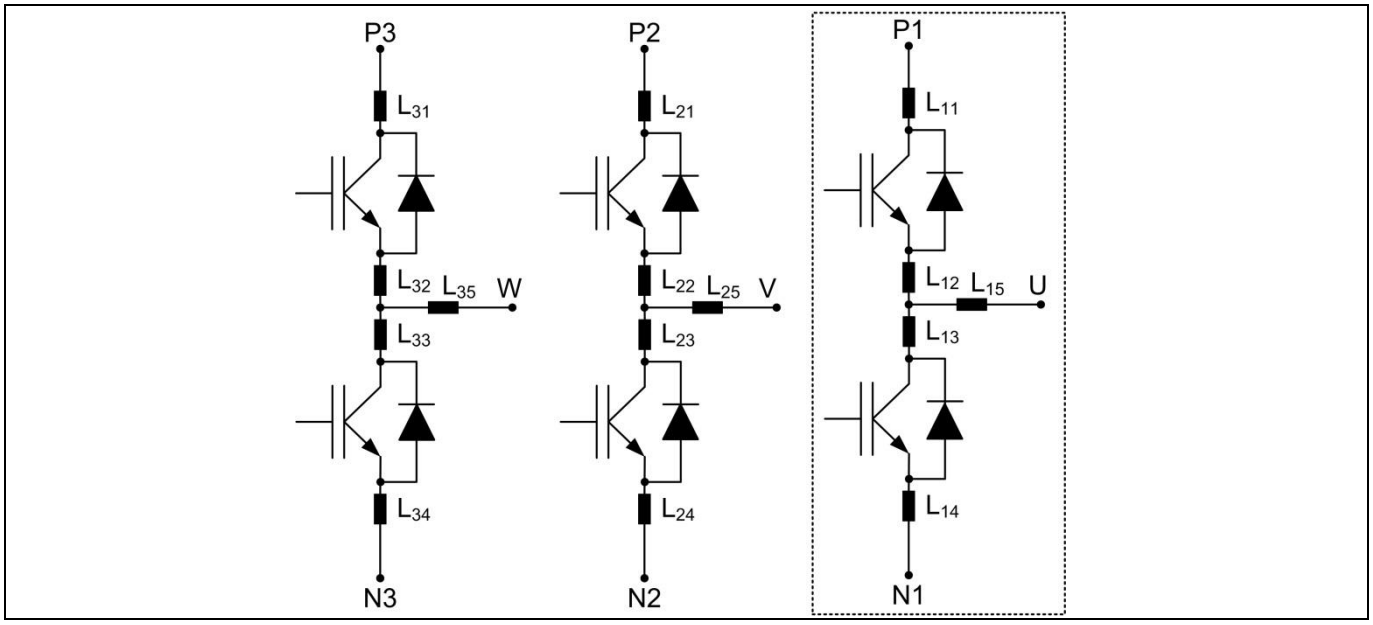

Figure 24 Equivalent stray inductance circuit of a six-pack module with 6xDC terminal. Module stray inductances are drawn simplified.

In case the power module is not symmetric (especially for two terminal DC connection B6-bridge modules), the stray inductance of each phase-leg is measured and the maximum value is noted in datasheet.

The module stray inductances L_{sCE} can be measured with an external auxiliary switch according to Figure 25. The auxiliary switch performs a double pulse and the diodes in the module provides the freewheeling path. At the second turn-on the module stray inductance causes a ΔV_{CE} depending on the stray inductance and the di/dt commutation speed. In practice, it can be seen that this measurement is not simple as it is very sensitive on voltage resolution and current probe bandwidth. Experience has shown that low commutation speed and lower working voltages provides a better signal quality and makes it easier to identify the module stray inductance.

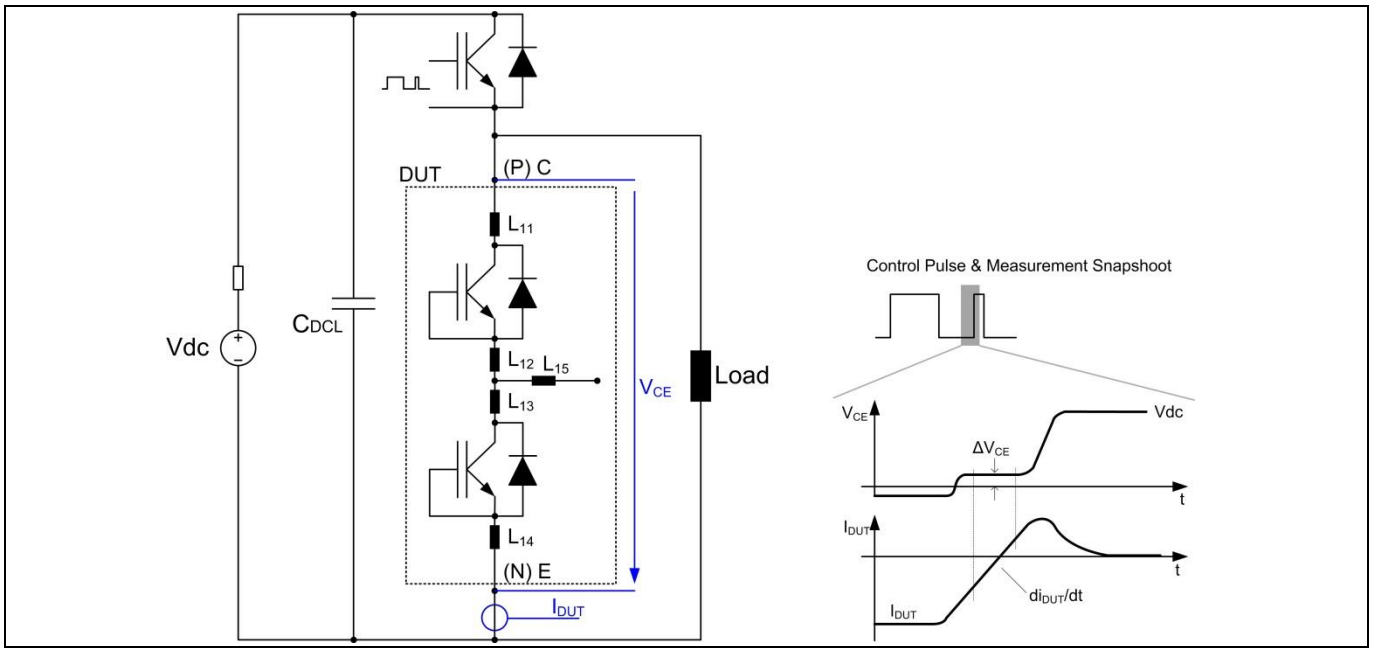

Figure 25 Typical setup for measurement of IGBT module stray inductance L_{sCE} with schematic voltage/current waveforms.

7.5 Module lead resistance, terminals - chip ($R_{CC'+EE'}$)

The lead resistance of the module is a further contributor to voltage drop and thus power losses. The specified value in the datasheet characterizes the lead resistance between the power terminals of one switch. According to the equivalent circuit shown in Figure 26, the module lead resistance is defined as:

$$R_{CC'+EE'} = R_{C'C''} + R_{CC''} + R_{EE''} + R_{E''E'} \quad (7.5)$$

The Figure 26 show the lead resistance of both, a high side and a low side switch. For the datasheet value the mean value of both is specified at room temperature. For aluminium bond wired power modules with DCB subtrates, the conducting paths contributing to the lead resistance are of aluminium and copper materials. These have a linear temperature coefficient of $\alpha_{AL} \approx 4.3 \cdot 10^{-3} \frac{1}{K}$ and $\alpha_{CU} \approx 3.9 \cdot 10^{-3} \frac{1}{K}$. For a simple approximation, the following dependency can be applied:

$$R_{CC'+EE'}(T) = R_{CC'+EE'}(25°C) \cdot \left[1 + 4.0 \cdot 10^{-3} \frac{1}{K}(T - 25°C)\right] \quad (7.6)$$

Which lead to 40% higher resistance at 125°C compared to the 25°C value.

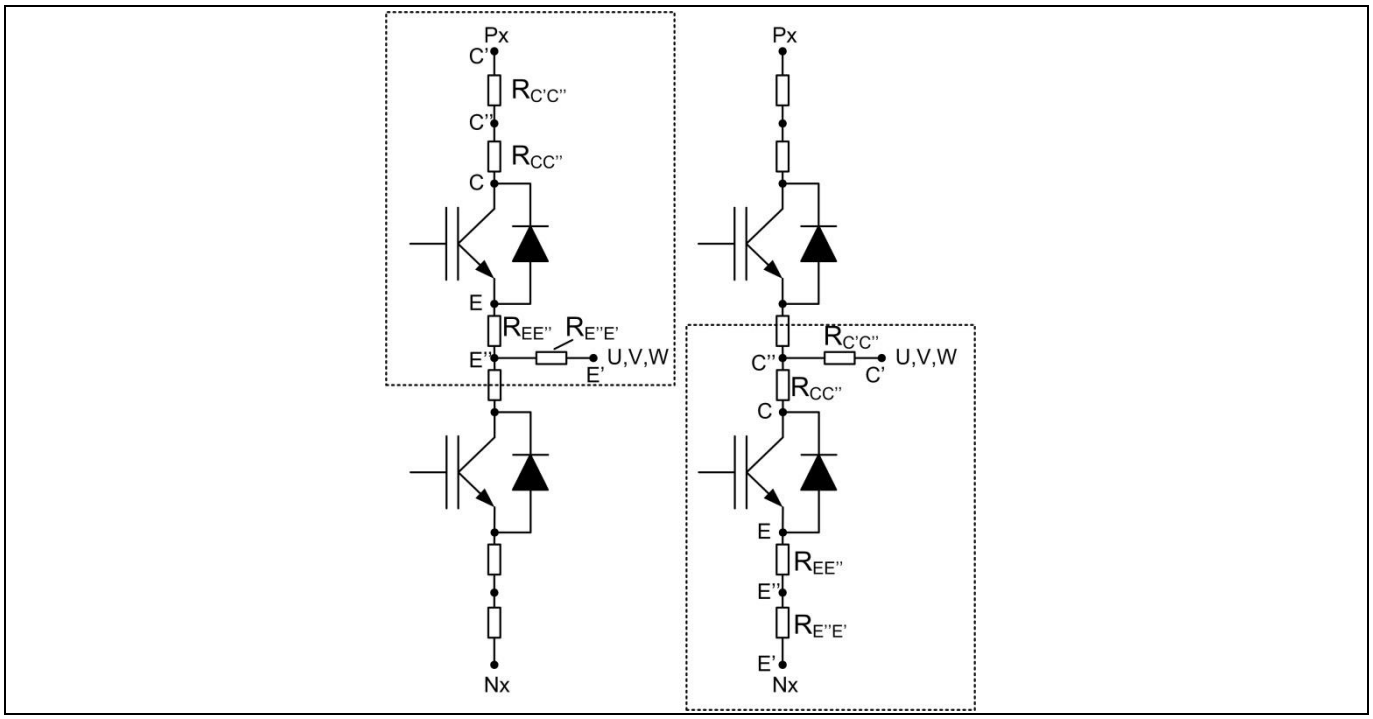

Figure 26 Equivalent circuit of module lead resistances.

Please note that for chip junction temperature estimation and calculations, it is not intended to add the power losses of the lead resistances to the chip power losses before multiplication with the chip thermal resistance. The dissipated power in the leads, copper, etc. are dissipated mainly in different thermal paths compared to the active silicon area. Nevertheless, the lead resistances contribute to the total system power losses and thus energy efficiency of the end product.

7.6 Maximum RMS module terminal current (I_{tRMS})

The maximum RMS module terminal current I_{tRMS} is an optional rating and specifies a maximum current value for a thermal steady state condition with specified boundary conditions. This rating is mainly given in order not to exceed the maximum temperature of the plastics housing. For the terminal current rating a fixed terminal temperature outside of the module is assumed (T_{Ct}). Under the nominal cooling conditions (see Rth specification) and the defined temperatures of the cooling fluid or the module case temperature the suitable terminal current is noted.

Please note that depending on the customer specific busbar and connections, the equivalent thermal mass at the power tab connection can be significantly different and typically it take several minutes until such a steady state condition may occur. For short term operation or transient pulses it is allowed to drive higher terminal currents.

7.7 Storage temperature (T_{stg})

The storage temperature defines the allowed long term storage conditions of the power module. More detailed information is in the mounting/assembly instructions of the corresponding power module product family.

7.8 Mounting torque for module mounting (M)

The screw torque for the mounting to the cooler, fixing PCBs or electrical connection are specified in the datasheet. These values are important to ensure the right clamping force of the module to the heatsink and ensure a reliable sealing in case of direct fluid cooled power modules.
More detailed information is in the assembly/mounting instructions of the corresponding power module product family.

7.9 Weight (G)

The total weight of the power module is defined in the product datasheet. A full declaration of materials present in the product with average mass in percent is included in the material content datasheet (MCDS), which can be downloaded on the Infineon website or requested on demand.

8 Frequently asked Questions (FAQ)

8.1 Maximum switching frequency

IGBTs can be designed with highly p doped collector for low conduction but high switching losses (i.e. typical IGBTs for drives applications) as well as with low p doped collector for high conduction but low switching losses (i.e. HighSpeed IGBTs). By means of such different collector doping an IGBT can be optimized for a given switching frequency range.
Even if an IGBT is optimized for e.g. 10kHz it is possible to drive the device at x times of this optimized range. The designer just has to ensure that the dissipated power (conduction + switching losses) together in combination with the thermal resistance (Rth) will not exceed the maximum T_{vjop} specified for the device.

As a conclusion IGBTs can be driven at a quite high switching frequency as long as the power dissipation in the considered operating point is low (e.g. lower currents, good cooling conditions, etc.). Due to this correlation, it is fairly possible to give a general switching frequency limit for a device without knowing exactly the boundary conditions of the specific application.

8.2 PWM Dead Time

In order to avoid current shoot through in the half bridges with exceedance of I_{CRM} and T_{vjop} it is required to set PWM dead times where both high- and low-side IGBTs are in the off state before the next switch is turned-on. Setting optimal (i.e. sufficient but minimum) dead times is a complex task as every gate driver leads to a different control timing (see examples in section 3.2.1 and 3.2.2 where the different switching characteristic also affect the appropriate dead time setting) and furthermore different operation conditions like temperate, voltage and current also affect the timing. A guideline to set appropriate PWM dead times can be found in [9].

8.3 Linear mode (i.e. desaturated IGBT)

The modern trench IGBT cells (also micro-pattern trench) are not suitable for linear mode operation. Such an operation must be strictly avoided in applications. Modern IGBTs are designed for switching application only.

Exceptional case is a short circuit (desaturated IGBT) which is a special use-case of linear mode. The main difference to a regular linear mode application is that the short circuit time is specified with a limited time. In this short time it is ensured that thermal runaway of individual cells will not occur and thus this short term linear mode is allowed for exceptional cases like short circuit.

8.4 Repetitive short circuit

A repetitive short circuit with repetition rate of typical switching frequencies (e.g. 10kHz) is not allowed. After a short circuit, where the IGBT is in a desaturated mode with full working voltage across V_{ce} and full short circuit current I_{SC}, the IGBT internal junction is heated rapidly far beyond the maximum allowed temperature for switching operation T_{vjop}. After a short circuit it is mandatory to wait until the IGBT is internally cooled down to the allowed T_{vjop} area before normal switching operation is continued.

8.5 Cooling fluid compatibility

For power modules with direct fluid cooling, the recommended mixture of the cooling fluid type is specified (like 50% water / 50% ethylenglycol). The fluid mixture has to provide enough anti-freeze for the application conditions. Freezing events of the fluid has to be strictly avoided. Freezing fluid will lead to plastic deformation of the power module baseplate and may lead to fluid leakage and/or isolation failure consequently. Furthermore, it is important to ensure that the fluid type with its corrosion protection is compatible with the material of the cooler (typical aluminium) and the baseplate plating type (typical nickel; specified under the Module section at baseplate specification).

Please note that incompatible fluid types can damage the cooling circuit in a short time, please consult your cooler fluid manufacturer for more information about its specific material compatibility.

8.6 Module Type Designation basics

The module type designation follows a basic structure. The **FX** defines the electric topology like FS for B6 bridges (six pack) followed by **###** the implemented DC collector current rating.

The **Y** indicates if the module is only forward or reverse conducting. When “R” is placed at the Y position of the type designation this means that antiparallel diodes are used for freewheeling and reverse conducting.

The blocking voltage of the chipset is divided by 10 and rounded and placed at the **zz** position.

The **XX** notes the package family followed by **YY** the chip technology.

The *** are used to indicate different package derivates and/or also customized products.

Modules with **_ENG** ending indicates that it is not a released part and can be solely used for evaluation purpose and lab testing. Parameters in an _ENG part may be subject to change without notice. They are not released products. For more information about _ENG parts please see also section 3.

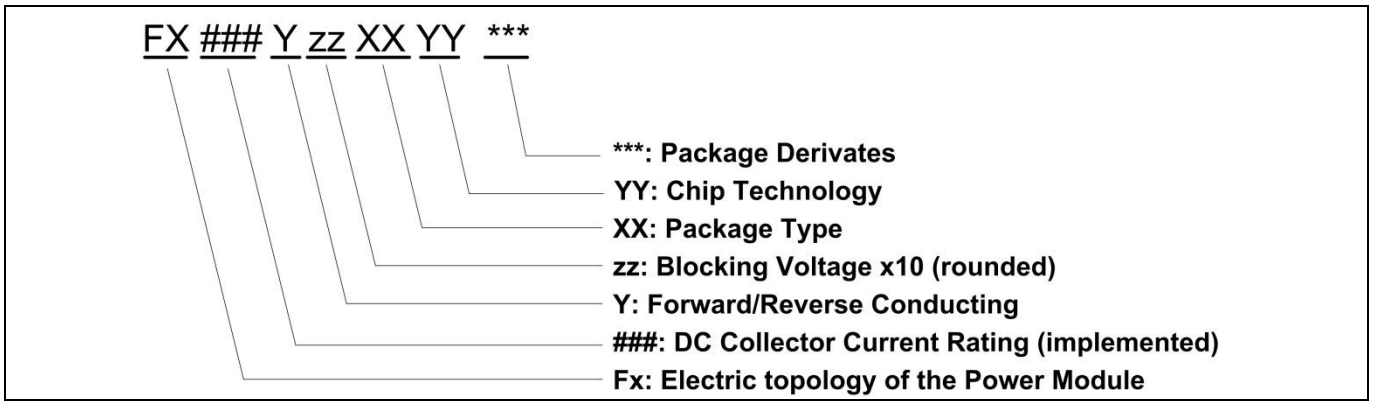

Figure 27 Module type designation principle.

Type designation overview of other automotive parts like discrete MOSFETs, smart switches, etc. can be found in [11].

9 References and Revision History

The referenced application notes can be found at http://www.infineon.com

[1] IEC 60747-15: Semiconductor Devices – Discrete Devices – Part 15: Isolated power semiconductor devices. Edition 2.0 2010-12.

[2] IEC 60747-2: Semiconductor Devices – Discrete Devices – Part 2: Rectifier diodes. Edition 3.0 2016-04.

[3] IEC 60747-9: Semiconductor Devices – Discrete Devices – Part 9: Insulated-gate bipolar transistors (IGBTs). Edition 3.0 2019-11.

[4] ZVEI AQG 324: ECPE Guideline, Qualification of Power Modules for Use in Power Electronics Converter Units in Motor Vehicles. Edition 02.1/2019. https://www.ecpe.org/research/working-groups/automotive-aqg-324/

[5] IEC 61140: Protection against electric shock – Common aspects for installation and equipment. Edition 3.1 2009-09.

[6] UL 1557: Safety for Electrically Isolated Semiconductor Devices. Edition 4 2006-06.

[7] Infineon Application note “2008-03: Thermal equivalent circuit model”.

[8] Infineon Application note “2008-01: Definition and use of junction temperature values”

[9] Infineon Application note “2007-04: How to calculate and minimize the dead time requirement for IGBTs”

[10] http://www.glykolundsole.de/Downloaddateien/Glykosol_N_Datenblatt_D.pdf

[11] Infineon Product Brochure “Automotive Power Selection Guide”

Revision History

Date	Version	Changed By	Change Description
2010-09	1.0	Tomas Reiter	Initial version
2017-11	2.0	Tomas Reiter (IFAG ATV HP EDT MD)	Update to new datasheet templates. Switching characteristic explanation with more examples. FAQ chapter added. Many minor updates.
2019-11	2.1	Tomas Reiter (IFAG ATV HP HMD AE)	Nomenclature Eon, Eoff, Erec revised according to latest datasheets.
2020-01	2.1b	Tomas Reiter (IFAG ATV HP HMD AE PDE)	Revised typos and reference list. No change in technical content.

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