

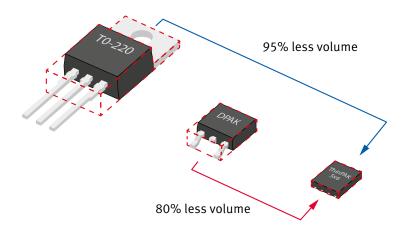
**Product Brief** 

# CoolMOS<sup>TM</sup> in ThinPAK 5x6

# The new leadless SMD package for CoolMOS™

ThinPAK 5x6 is a leadless SMD package especially designed for High Voltage MOSFETs. This new package has a very small footprint of 5x6mm² (30mm² vs. 77mm² for the DPAK) and a very low profile with only 1mm height (1.0mm vs. 2.3mm for the DPAK). This significantly smaller package size in combination with its benchmark low parasitic inductances can be used as a new and effective way to decrease system solution size in power-density driven designs. The ThinPAK 5x6 package is characterized by a very low source inductance 1.6nH (vs. 4.7nH for DPAK), as well as a similar thermal performance as DPAK. The package hence enables faster and thus more efficient switching of Power MOSFETs and is easier to handle in terms of switching behavior and EMI.

Comparison between TO220FP, standard SMD package DPAK and the new leadless SMD package ThinPAK 5x6



The new ThinPAK 5x6 shows 80% less volume vs. conventional DPAK making designs more compact and efficient.

### **Key Features**

- Small footprint (5x6mm²)
- Low profile (1mm)
- Low parasitic inductance
- RoHS compliant
- Halogen free mold compound

### **Key Benefits**

- Reduced board space consumption
- Increased power density
- Short commutation loop
- Smooth switching waveform
- Easy to use products
- Environmentally friendly

## **Applications**

- Adapter
- Consumer
- Lighting





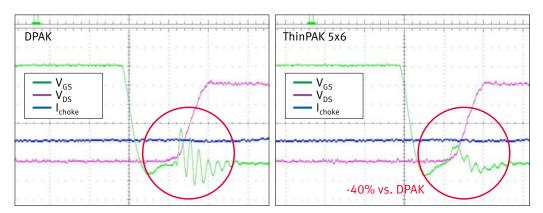


# CoolMOS™ in ThinPAK 5x6

# The new leadless SMD package for CoolMOS™

This smaller footprint of ThinPAK 5x6 offers a space saving advantage and a reduction of the internal and external MOSFET parasitics normally induced by conventional leaded packages. In particular, the source inductance, which influences the gate

drive voltages when switching with high di/dt, and the drain inductance, could drive the drain source voltage internally seen on the chip over the maximum allowed break down voltage (rated in the equivalent datasheets).



 $R_{G.ext}$ =0.5 $\Omega$ ;  $I_D$  = 4A;  $C_{GD,ext}$  = 5pF

The additional voltage drop (oscillation) on the gate-source signal is dependent on the internal and external source inductance.

## Product Portfolio for CoolMOS™ in ThinPAK 5x6

	Maximum Ratings		$R_{DS(on)}\left[\Omega ight]$		
Part number	V <sub>DSS</sub> [V]	I <sub>D</sub> [A]	Тур	Max	Q <sub>g</sub> (typ) [nC]
IPL60R360P6S	600	30.0	0.32	0.36	22.0
IPL60R650P6S	600	16.5	0.59	0.65	12.0
IPL60R1k5C6S	600	7.7	1.35	1.5	9.4
IPL60R2k1C6S	600	5.4	1.89	2.1	6.7
IPL65R650C6S	650	16.6	0.59	0.65	23.0
IPL65R1k0C6S	650	12.3	0.9	1.0	15.0
IPL65R1k5C6S	650	8.4	1.35	1.5	11.0

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