

High Current Voltage Regulator Module Employs Novel Packaging Technology to Achieve Over 100A in a Compact Footprint to Power Next Generation Servers

By Carl Blake, Ralph Monteiro and Andrew Sawle
International Rectifier, El Segundo CA, USA

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Abstract - The benefits of the first surface mount package optimized for dual sided cooling will be discussed as they apply to advanced voltage regulator module (VRM) design. A VRM will be designed using this new surface mount packaging technology for power MOSFETs, and shown to deliver the highest current in a compact footprint to meet the needs of next generation GHz class processors.

I. INTRODUCTION

DC-DC converters for performance desktop PCs, notebooks and servers use surface mount packaged power MOSFETs, which to date have offered poor thermal performance and are not easy to heatsink. The result of this is that the power MOSFET generates a large amount of heat that is transferred directly to the PCB making thermal management difficult. As current density requirements for the next generation processors increase this problem will only escalate. This is especially true in 32-bit server applications where current requirements of the next generation GHz class processors approach 100A, while at the same time system users demand that the server fit into a smaller 1U sized rack. This paper discusses the design of a VRM using a novel surface mount packaging technology, which allows double sided cooling for power MOSFETs. The new package technology improves performance through better integration of the MOSFET package into the VRM electrical and mechanical design.

II. NEED FOR NEW PACKAGING TECHNOLOGY

Optimized silicon technology has driven MOSFET performance to the point where packaging now is a limiting factor to higher performance MOSFETs. Existing packages for silicon die introduce parasitic resistances and inductances, which compromise system performance. 40% of the $R_{DS(on)}$ of the best MOSFETs available on the market today is due to the package. New packaging technologies are

therefore employing radical new concepts in order to minimize the package related parasitics and to

resolve the electrical and thermal management challenges due to heat dissipation in power

MOSFETs. Any new solution would have to be easy to implement and improve layout simplicity to reduce time to market in one of the fastest moving industries. An example of one such solution is a novel surface mount packaging technology, which allows double sided cooling for power MOSFETs. The proprietary package is the first surface mount package developed especially for power applications and can address most of the thermal and electrical efficiency problems faced by today's advanced DC-DC converters.

III. DIRECTFET™ PACKAGING TECHNOLOGY

Patented DirectFET™ technology is the first surface-mount package designed from the ground up for power semiconductors. It has a unique construction that provides breakthroughs in die free package resistance and heat dissipation capabilities, dramatically increasing efficiency and current carrying capacity of the device in a given footprint.

The silicon die is contained in a copper housing (copper 'can'). The bottom of the package consists of a die specifically designed with source and gate contact pads that can be soldered directly to the PCB. The copper 'can' forms the drain connection from the other side of the die to the board (See Fig. 1). A proprietary passivation system on the silicon die isolates the gate and the source pads to prevent shorting and acts as a solder mask when the device is mounted on the PCB. The passivation layer also protects the termination and gate structures from moisture and other contamination.

This design eliminates the lead-frame and wire bonds, reducing die-free package resistance (DFPR) to a mere 0.1mOhm in an SO-8 footprint compared to 1.5 mOhm for the standard SO-8 package [2].

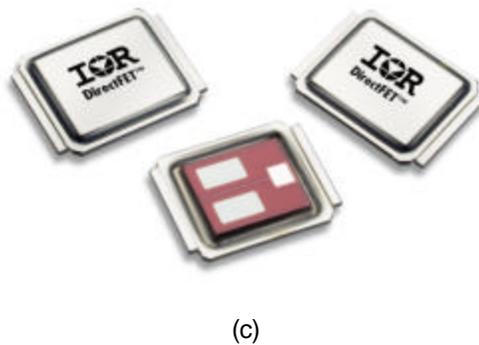
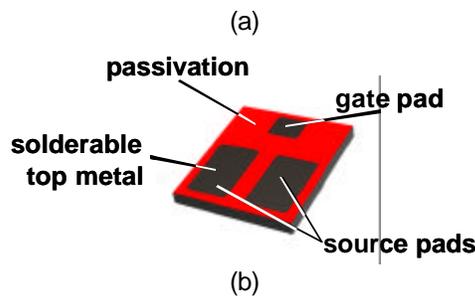
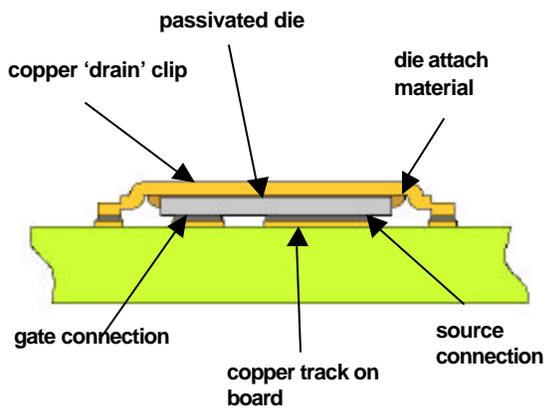


Fig. 1. DirectFET Packaging (a) Cross Section (b) MOSFET die (c) Photograph

The large-area contacts combined with the copper housing significantly improve heat dissipation compared to a SOIC plastic molded package: the junction-to-PCB thermal resistance is reduced to 1°C/W, compared to 20°C/W for a standard SO-8 package. The copper 'can' provides a heat sink surface, improving top junction-to-case thermal resistance to 3°C/W compared to 18°C/W for a SO-8.

Extensive use of finite element analysis (FEA) modeling was employed in order to determine the gains that could be made from the various

methods of top-side cooling that could be applied to DirectFET devices. Thermal solutions such as airflow, a heatsink with no airflow and both a heatsink and airflow were considered. Fig. 2. below shows one such solution condition where a finned heat sink and airflow is used to increase the power that can be dissipated through the top of the package and away from the board. As can be seen from the figure, the airflow over the finned heatsink heats up considerably showing how well the DirectFET package transfers heat out through the top of the device and away from the PCB.

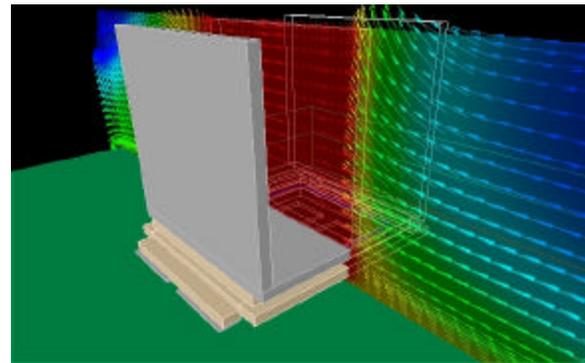


Fig. 2. FEA modeling employed to show the thermal profile of cooling air over DirectFET Technology and finned heat sink

With the use of heatsinks and cooling air flow, the DirectFET package can dissipate more heat out of the top of the package, reducing operating temperatures by up to 50°C compared to the SO-8 solution. Effective top-side cooling means that heat dissipated can be pulled away from the circuit board, increasing the currents that the device can safely carry. High top $R_{th(j-c)}$ explains why standard and derivative SO-8 packages are only used with single-side cooling through the PCB.

As current requirements exceed 100A, multiphase buck converters will be required to deliver over 25A/phase. The new packaging technology improves efficiency and thermal performance to a great extent allowing these high current levels to be achieved by a single control and synchronous FET per phase, eliminating the need to parallel multiple devices and thus simplifying board layout. As transient response requirements increase with higher current and higher frequency, designers need to increase operating frequencies. At higher operating frequencies, package and PCB trace parasitics compromise system performance. The new packaging technology allows easy layout (see Fig. 3.), simplifying board design and therefore

reduces board parasitics [2]. The improved electrical and thermal performance allows smaller solution footprints, higher current density and stable board temperatures.

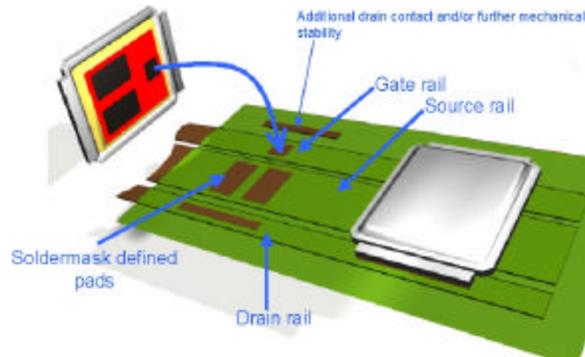


Fig. 3. DirectFET Packaging technology simplifies board layout and design complexity.

IV. VRM DESIGN

To demonstrate the benefits of this new packaging technology in a VRM design, a high current 4-phase VRM was designed using DirectFET MOSFETs. A photograph of the VRM design is shown in Fig. 4.

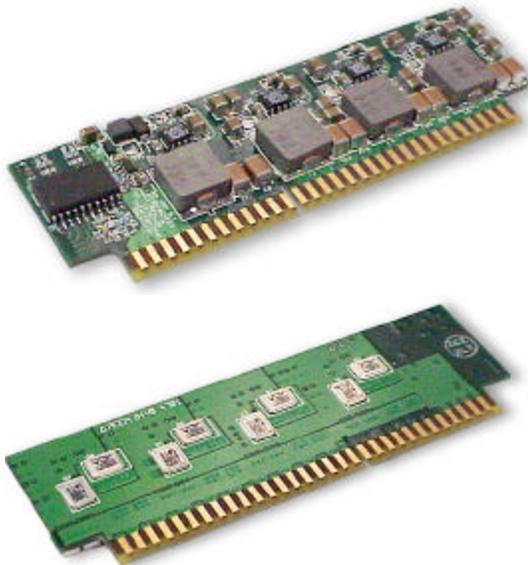


Fig. 4. Photograph of top and bottom side (heat sink over FETs on the bottom side not shown) of a VRM design (95mm X 31mm).

The VRM design uses a 4-phase controller and a driver per phase which are able to operate at up to 1MHz switching speed across all 4 phases. The drivers are able to provide drive currents of up to

1.5A and implement an integral diode for the boost drive.

The board is 6-layer, 2oz. copper using pad-in-via technology. It employs an "All-Ceramic" solution for the output and input filters. The input capacitors were supplied by Murata (Part # GRM32 E R6 1C 106K) and the output capacitors were supplied by TDK (Part # C452X5R0J107MT). The inductor is a 400nH high-current, small footprint coil (10mmX10mm). This was supplied by Panasonic (Part # ZM104LR36).

The design is capable of over 100A (> 25A/phase) in a 95mm x 31mm (3.8in x 1.25in) footprint and uses a single control and synchronous DirectFET MOSFET per phase. The low profile of the devices allows the converter design to be configured with the DirectFET MOSFETs on the back of the board and a heat sink to be mounted on top of them while still staying within VRM 9.1 outline specifications [3]. The heat sink is an aluminum finned heat sink measuring in 94mm x 19mm (3.75in x 0.75in). It was attached on top of the DirectFET MOSFETs using an electrically isolating, heat conducting epoxy. The current density achievable by such a design is greater than 20A/in² providing a viable solution for the next generation VRM.

The specifications of the 30V DirectFET control and synchronous FET are shown in TABLE I, note the high current capability (I_D) of both the devices.

TABLE I: SPECIFICATIONS

Part #	$R_{DS(on)}$ mOhm @10V _{GS}	Q_G (nC)	Q_{GD} (nC)	Q_{GS} (nC)	I_D (A)
IRF6603	2.8	69	19	14.5	84*
IRF6604	10	20	7	6.8	59*

Note: All values typical

* $T_{CASE} = 25^\circ C$

As can be seen, the devices have been optimized as per the socket requirements, with the low $R_{DS(on)}$ device used in the synchronous FET socket, which has the maximum duty cycle. The IRF6604 is used in the control FET socket with a short duty cycle where switching losses dominate. The gate charge of this device is extremely low to limit driver losses.

The high current carrying capability of the DirectFET MOSFETs simplifies the layout since

only a single pair of devices is required per phase eliminating the need to parallel devices to achieve the desired levels of efficiency.

Similar designs using D-Pak or SO-8 packaged devices use 4-5 devices per phase. Paralleling devices is the only path to achieve the required current handling capability. However with increasing device count, package losses and gate charges also increase, thereby increasing driver losses and compromising efficiency. Board size and layout complexity also increases and power density crucial for 1U servers also suffers.

Increase in board size can, not only increase the cost of the design significantly, but also compromise efficiency as parasitic losses come into play.

Let us consider the effect of trace resistance of the copper tracks on the board. A trace resistance of 4mOhms/phase is entirely possible in a VRM design. The heat dissipated through the PCB board due to the trace resistance is given by I^2R . For a design with 25A/phase and a trace resistance of 4mOhms, the power loss is 2.5W or 10W for 4 phases. For a design which is capable of 100A @ 1.7V, this contributes to a 5.8% loss in efficiency.

An SO-8 or D-Pak based design uses 4-5 devices/phase. In order to dissipate the heat better, the devices have to be laid out in a wider area. The solution footprint for these devices is typically twice that of DirectFET. Let us calculate the effect the solution size increase has on the efficiency.

The trace resistivity is directly proportional to the length of the trace.

i.e. $r \propto \frac{L}{A}$ where L is the length of the trace and A the cross sectional area.

If the board size increases two-fold and we assume that the thickness of the traces is the same for both boards while the trace length increases by a factor of $\sqrt{2}$, then the parasitic resistance will increase by 41%. This contributes to a significant drop in efficiency.

The small board size and efficient board layout are all achieved due to the high thermal and electrical efficiency of the DirectFET package. This has a direct impact on the efficiency levels achievable using this packaging technology.

V. OPTIMIZING EFFICIENCY AND CURRENT HANDLING CAPABILITY

In order to optimize the VRM design, efficiency measurements were made under various thermal and electrical operating conditions. These are discussed in further detail below.

Fig. 5. shows the efficiency curves generated by the 12V input, 1.3V output VRM operating at 250kHz under various heat sinking conditions. As can be seen, using the finned heatsink and airflow over the DirectFET devices for effective topside cooling increases the current capacity to well over 100A.

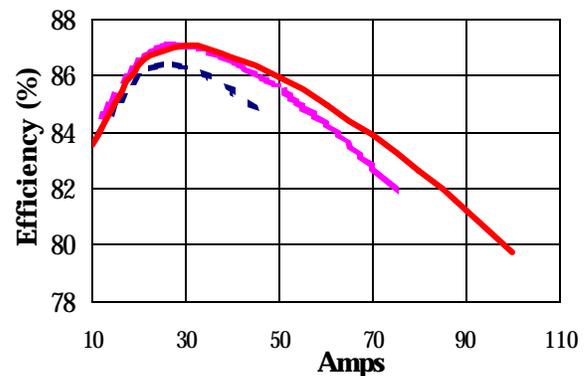


Fig. 5. Efficiency curves generated under various thermal environments

Even as frequency is increased, efficiency levels of 77% can be achieved at 100A load current as can be seen from Fig. 6. The ease of layout of the DirectFET package and the low package inductance and resistance at higher frequencies contributes to the high efficiency levels achievable

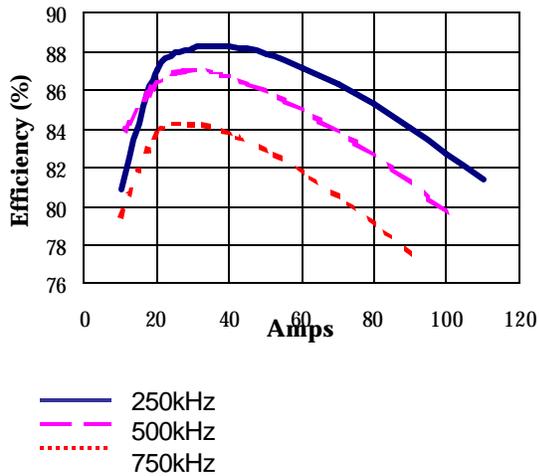


Fig. 6. Efficiency curves generated at 250kHz, 500kHz and 750kHz.

at high frequencies. The DFPR of packages such as the D-Pak increase tremendously at higher frequencies. When that is compounded with paralleling of devices and layout complexity, efficiencies can be severely compromised.

Since the DirectFET MOSFETs have a V_{GS} rating of 20V, they require a gate drive voltage of 5V or above to hard switch the devices. In order to determine the effect of gate drive voltage on the efficiency of the VRM design a number of efficiency curves were generated under similar ambient conditions and 500 kHz operating frequency while increasing drive voltages. At a V_{GS} of 9V, the efficiency at 1.7Vout and 100A load current was found to be 85%.

In order to improve the efficiency further, a Schottky diode was used in parallel with the synchronous FET IRF6603. Since the DirectFET package inductance is very low, even at higher frequencies, the parasitic inductance between the Schottky diode and the synchronous FET are low allowing an increase in efficiency.

Efficiency curves were generated at 1.7Vout and 1.3Vout at 500kHz operating frequency using 600LFM airflow and a heat sink on top of the DirectFETs. As can be seen from Fig. 8., peak efficiencies of greater than 90% can be achieved under such conditions, while the efficiency at 100A load current is a phenomenal 86% at 1.7Vout.

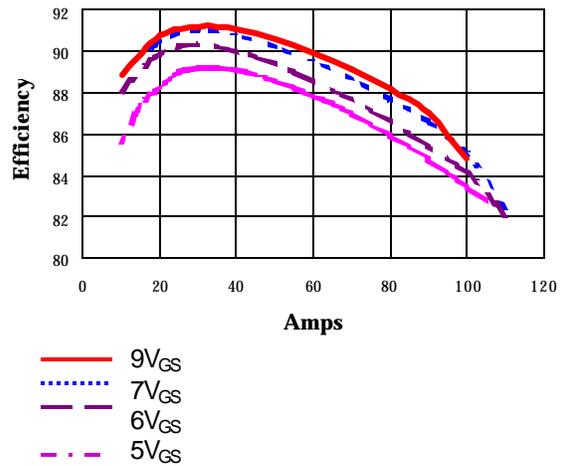


Fig. 7. Efficiency curves generated at 1.7Vout and 500kHz at various gate drive voltages.

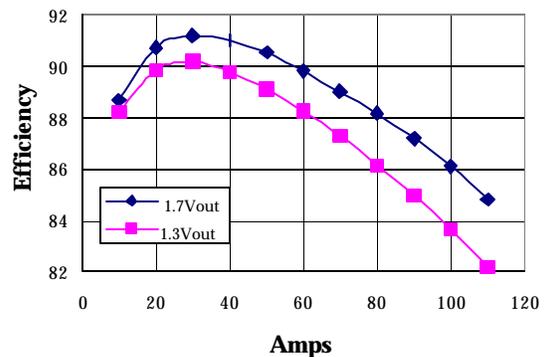


Fig. 8. Efficiency curves generated at 1.7Vout and 1.3Vout at 500kHz, 600LFM airflow + heatsink

Thermal images of the PCB board were also taken at full load (110A), as shown in Fig. 9. and Fig. 10. As can be seen, the increase in frequency from 250kHz to 500kHz, contributes to a very small rise in temperature confirming that the VRM design can be safely operated at higher frequencies. The high frequency operation results in faster transient response and a further reduction in size and cost of the passive components.

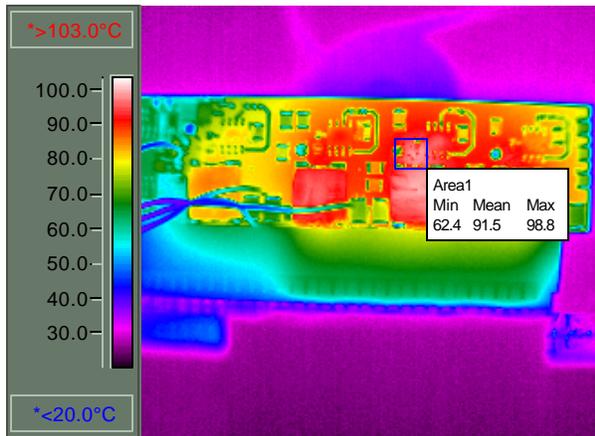


Fig. 9. VRM operated at 250kHz, 110A load. (Heat sink and 600LFM)

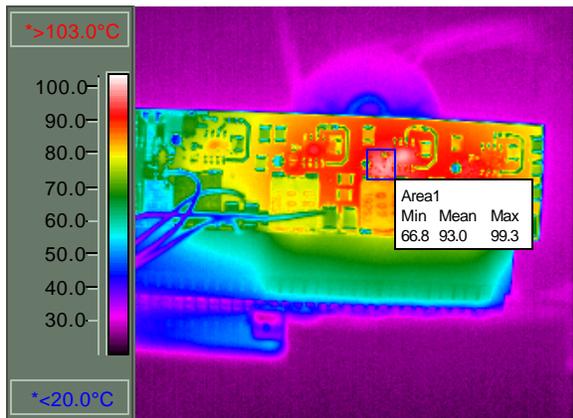


Fig. 10. VRM operated at 500kHz, 110A load. (Heat sink and 600 LFM)

VI. CONCLUSIONS

DirectFET technology is the first surface-mount package specifically designed for high performance power semiconductors and makes use of a new proprietary passivation and interconnection methodology to achieve radical gains in electrical and thermal performance.

The first devices using DirectFET technology were demonstrated to have tremendous improvements in current carrying capability and in circuit efficiency. Utilizing double sided cooling, a single synchronous and control FET chipset can provide more than 25A per phase, doubling current density and paving the way for high current, compact DC-DC converters for next generation processors used in 1U servers.

While these improvements in system performance alone are phenomenal, the real benefit of DirectFET technology comes from the fact that it can reduce system cost at the same time. Thermal design can be simplified since the improved performance of the DirectFET package means that the PCB size and the amount of copper used in it can be reduced. Expensive thermal management solutions such as heat pipes can also be eliminated. As performance demands increase traditional SMT type packages will gradually become obsolete and used only in low end cost driven designs while the high-end power management systems will migrate to using packages that exhibit order-of-magnitude lower electrical resistance, thermal resistance, and parasitic inductance characteristics. The most successful platforms will offer the lowest cost/amp while delivering the performance required by the system in form factors which allow straightforward design and manufacturing integration. The fact that DirectFET packaging technology meets all these requirements, makes it one of the most important advances in power semiconductor packaging technology.

ACKNOWLEDGEMENT

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