IRS2505L µPFC™ Control IC Design Guide

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Application Note

About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and guide to using the IRS2505L power factor correction control IC at the front end of a switch mode power supply (SMPS). The scope applies to all technical aspects that should be considered in the design process, including calculation of external component values, MOSFET selection, PCB layout optimization as well as additional circuitry that may be added if needed in certain cases.

Intended audience

Power supply design engineers, applications engineers, students.

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1 Introduction and Device Overview

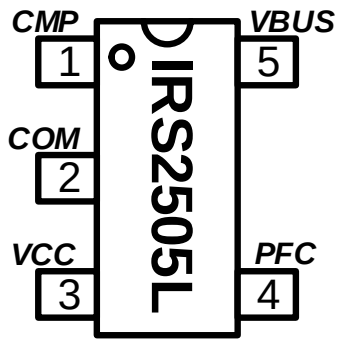
The IRS2505L is a critical conduction mode (CrCM) Boost PFC controller IC primarily intended for front end PFC pre-regulators typically used in power supply and lighting applications up to 150W. It may also be used in other SMPS topologies such as Buck, Buck-Boost and Flyback, which are not covered here. All of the functionality required for controlling the PFC converter has been integrated into an SOT23 package requiring only 5 pins. This unique low pin count solution operates by using multi-functional VBUS and PFC pins so that the cycle by cycle current sense input is combined with the output voltage feedback at the VBUS pin and the zero-crossing (ZX) sensing function is combined with the gate drive at the PFC pin.

The IRS2505L based PFC is able to meet the requirements of EN61000-3-2, including class C limits for lighting applications.

The design procedure for a PFC stage based on the IRS2505L differs slightly from the procedure used for industry standard 8 pin CrCM PFC control ICs and will be explained in detail here. In order for the circuit to produce optimum performance care must be taken to select the correct component values and ratings. The PCB must also be designed according to the correct practices for SMPS design to avoid noise susceptibility for which guidelines are provided.

In order to save design time a simple design tool in the form of a spreadsheet is available, which calculates all of the component values based on user inputs as well as providing a simple means for designing the inductor.

IRS2505L uses a 5-pin SOT-23 package as shown below:



Pin	Name	Description
1	***CMP***	PFC error amplifier compensation
2	***COM***	IC power and signal ground
3	***VCC***	Logic and gate drive supply voltage
4	***PFC***	PFC gate driver output and zero-crossing detection
5	***VBUS***	DC bus sensing input and OCP

Figure 1 IRS2505L pin assignments

2 IRS2505L startup and supply circuitry

The VCC supply for the IRS2505L is initially derived from the rectified voltage at the input bridge rectifier positive terminal (VRECT+) through two series resistors, RVCC1 and RVCC2. Two resistors are needed in order to properly withstand the high voltage between the bridge rectifier output and VCC.

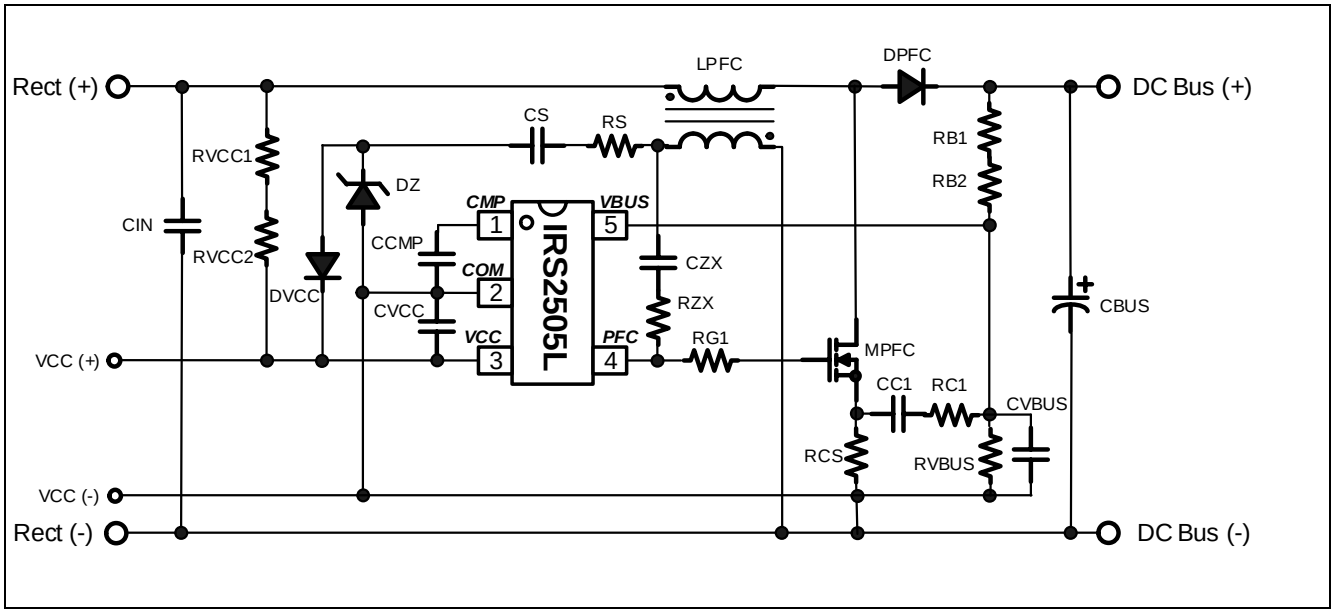


Figure 2 IRS2505 Boost PFC pre-regulator

An auxiliary winding on the PFC inductor (LPFC) can be used in conjunction with the charge pump circuit made up of RS, CS, DZ and DVCC, to supply VCC during circuit operation. However, in many applications VCC is derived from the back end converter stage and this is not necessary.

In both cases the auxiliary supply is able to take over supplying VCC when the converter starts switching.

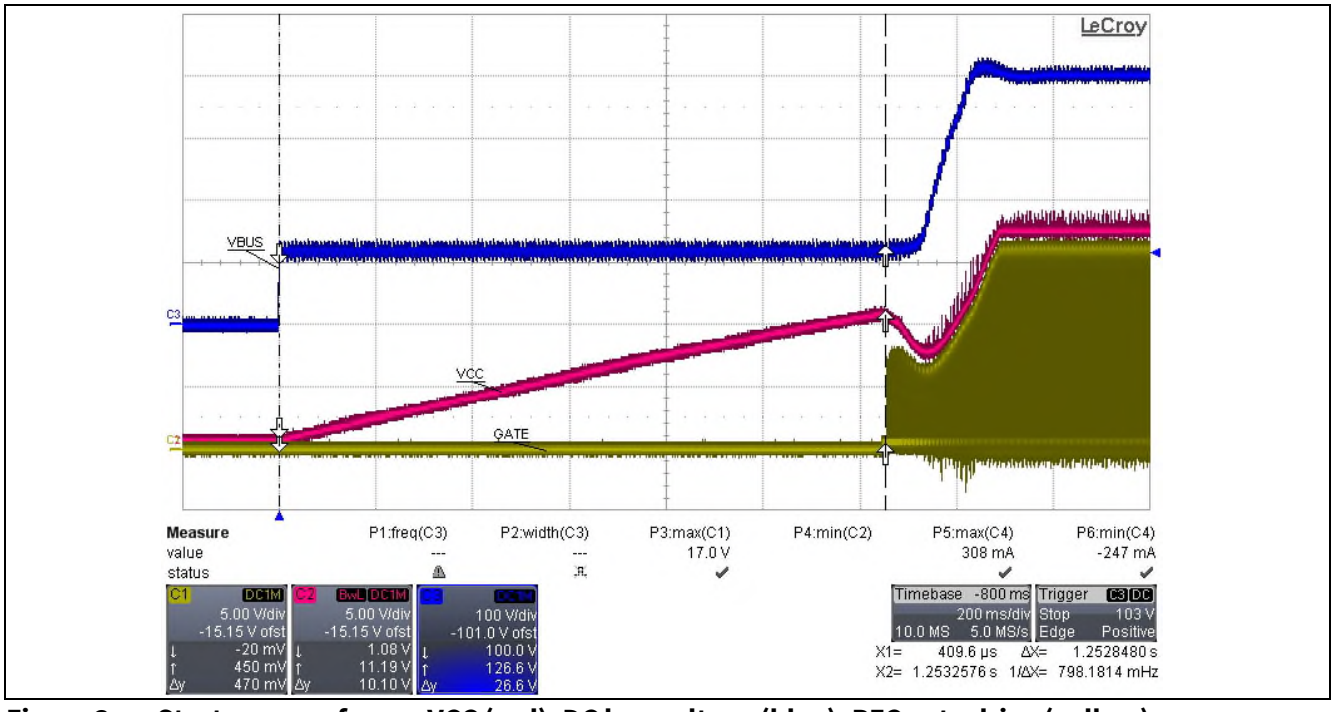


Figure 3 Start up waveforms, VCC (red), DC bus voltage (blue), PFC gate drive (yellow)

IRS2505L startup and supply circuitry

The values of resistors RVCC1 and RVCC2 should be equal and as large as possible to minimize power dissipation, however start up delay occurs due to the initial charging of CVCC to VCCUV+ that needs to be kept to a minimum so there is a tradeoff. The value of each resistor based on a specified start up time and value of CVCC is calculated as follows:

$$RVCC1 = RVCC2 \approx \frac{\sqrt{2}\cdot VAC_{MIN(RMS)} - \frac{VCCUV^+}{2}}{2\cdot C_{VCC}\cdot\left(\frac{VCCUV^+}{t_{START}}\right) + IQCCUV} \quad [\Omega] \quad [1]$$

Equation 1 accounts for the effect of CIN and CBUS, which means that before startup VRECT+ will be a smoothed DC voltage of $\sqrt{2}$ times VACMIN(RMS), which becomes full wave rectified only after the converter has started switching. The values of VCCUV+ (11.1V) and IQCCUV (60µA) are obtained from the IRS2505L datasheet. The equation is re-arranged to give t_{START}:

$$t_{START} \approx \frac{C_{VCC}\cdot VCCUV^+}{\left(\frac{\sqrt{2}\cdot VAC_{MIN(RMS)} - \frac{VCCUV^+}{2}}{RVCC1+RVCC2}\right) - \frac{IQCCUV}{2}} \quad [s] \quad [2]$$

The value of CVCC must be sufficiently large to supply the PFC circuit long enough for the auxiliary supply to take over, which typically requires a value in the tens of µF. The minimum value required for CVCC can be calculated by first calculating the necessary hold up time from the compensation capacitor (CCMP) and error amplifier drive current (ICMP+):

$$t_{HOLD} \approx \frac{1.4\cdot CCMP}{ICMP^+} + t_{TOVER} \quad [s] \quad [3]$$

Where t_{TOVER} is the time required for the auxiliary supply to take over supplying VCC after the gate drive first starts switching. In the example shown in figure 3 this is approximately 100ms. It is now possible to calculate CVCC from datasheet parameters IQCC (800µA) and VCCUVHYS (3.2V) allowing for the gate drive current (I_{GD}) which is 500uA in this example:

$$C_{VCC(MIN)} = \left(IQCC + I_{GD} - \frac{\sqrt{2}\cdot VAC_{MIN} - VCCUV^+}{RVCC1 + RVCC2}\right)\cdot\frac{t_{HOLD}}{VCCUV_{HYS}} \quad [F] \quad [4]$$

The value calculated in this example is 46.6µF.

The maximum power dissipation in each resistor during normal running (not startup) is given by:

$$P_{RVCC1} = P_{RVCC2} = \frac{\left(VAC_{MAX(RMS)} - VCC\right)^2}{2\cdot(R_{VCC1}+R_{VCC2})} \quad [W] \quad [5]$$

The waveforms in figure 3 show start up behavior with CVCC=43µF and RVCC1=RVCC2=150kΩ with an AC input voltage of 90Vrms. From equation 2, the start up time is calculated as 1.27s. The measured value is very close to the calculated value according to figure 3, measuring to the point when VCC first reaches VCCUV+. Power dissipation should be calculated for the worst case, which is at high line, therefore if the PFC

is operating over a wide range from 90 to 265VAC and VCC=14V in steady state operation the power dissipation per resistor at high line would be 102mW and 0.25W rated resistors are therefore sufficient.

3 Boost PFC circuit

3.1 Basic principles

The main elements of the PFC Boost converter are illustrated in figure 4, with the graph showing how in critical conduction mode (CrCM), the inductor current ramps up to a peak level and then ramps down to zero before beginning the next cycle. This is sometimes also referred to transition mode or boundary mode.

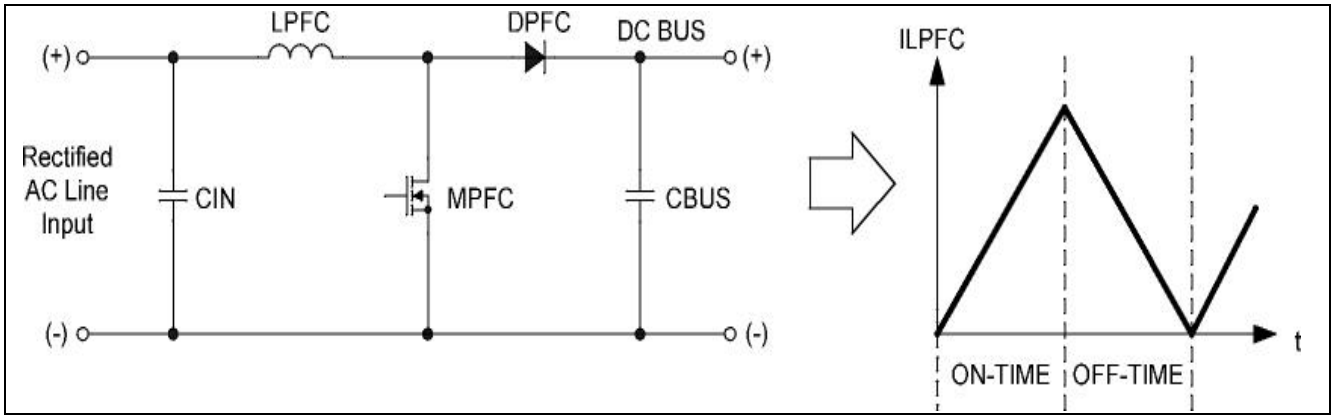


Figure 4 CrCM PFC Boost converter

Parameter	Unit	Definition
VAC	V	AC line input voltage
f_{IN}	Hz	Line frequency
VBUS	V	DC Output voltage
η		Efficiency
f_{MIN}	Hz	Minimum switching frequency
POUT	W	Output power
IPFC	A	Peak inductor current at the peak of the AC line cycle
$IPFC_{MAX}$	A	Peak inductor current at the peak of the AC line at minimum line input
tON	S	Gate drive ON time
tOFF	S	Gate drive OFF time
LPFC	H	Inductor value

Table 1 Definition of terms

During the period when the gate drive is high and the MOSFET (MPFC) is on, the inductor current rises according to equation 6 and during the the gate is low and MPFC is off it falls according to equation 7:

$$\frac{diL+}{dt} = \frac{VAC(t)}{LPFC} = \frac{\sqrt{2}\cdot VAC_{RMS}\cdot\sin(2\pi f_{IN}\cdot t)}{LPFC} \quad [A/s] \quad [6]$$

$$\frac{diL-}{dt} = \frac{VBUS-VAC(t)}{LPFC} = \frac{VBUS-\sqrt{2}\cdot VAC_{RMS}\cdot\sin(2\pi f_{IN}\cdot t)}{LPFC} \quad [A/s] \quad [7]$$

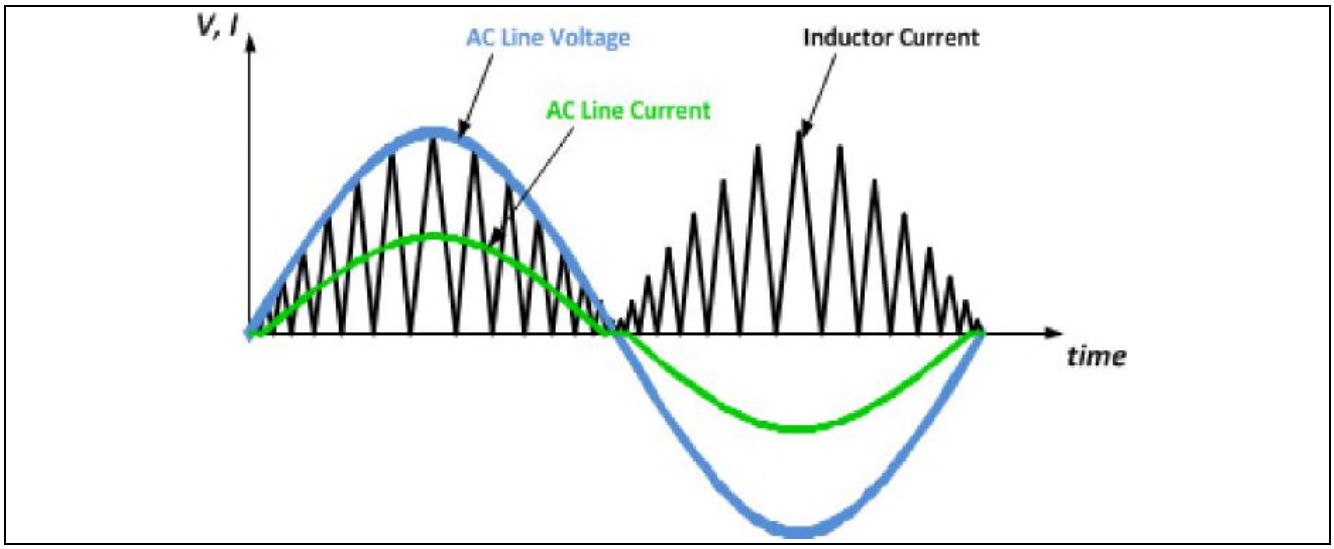


Figure 5 CrCM PFC inductor and AC line input current

The peak inductor current shown in black in figure 5 follows the sinusoidal envelope of the rectified input voltage ramping down to zero before the next switching cycle begins. The result is that when the high frequency switching component has been filtered out so the average input current becomes sinusoidal providing a high power factor and low THD. The IRS2505L operates with constant on time over the majority of the line voltage half cycle with some increase occurring as voltage approaches the AC line zero crossing. This “on time modulation” function is built in to compensate for cross over distortion and reduce harmonics in the line input current. The on time modulation function operates when the off time is greater than 7µs. To optimize THD, the inductance of LPFC needs to be selected so that at the peak of the AC line at the desired nominal AC input voltage, the off time is close to 15µs. Under this condition the on time modulation will operate as the voltage approaches the zero crossings but will have no effect close to the peaks.

Equation 6 shows that for a constant on time the slope of the inductor current must be proportional to the instantaneous input voltage explaining why the peak current follows the sinusoidal voltage envelope. The peak current at low line is calculated as follows:

$$IPFC_{MAX} = \frac{2\sqrt{2}\cdot POUT}{VAC_{MIN}\cdot\eta} \quad [A] \quad [8]$$

The maximum peak inductor cycle by cycle current limit is performed at the VBUS input of the IRS2505L. An external current sense resistor (RCS) is connected from the source of MPFC to the zero volts bus. The voltage developed across RCS is AC coupled onto the VBUS feedback divider through CC1 and RC1. The value of RCS is calculated by:

$$RCS = \frac{2\cdot V_{BUSOC+}}{IPFC_{MAX}} \quad [\Omega] \quad [9]$$

Where, VBUSOC+ is 0.56V (from the datasheet).

It can be seen from equation 7 that during the off time the downward slope of the current depends on the difference between the instantaneous input voltage and the output voltage that is effectively constant in

steady state operation. This means that the off time is longest at the peak of the line input and becomes progressively shorter as it approaches the zero crossing.

3.2 Inductor calculation

Since line input current distortion increases with line input voltage, on time modulation is necessary at higher input voltages. In a typical wide input range PFC circuit, the input voltage could vary from 90VRMS to 265VRMS (or even 305VRMS to support 277VAC power outlets found in the United States). A nominal input voltage is selected at which level THD reduction through the on time modulation function is most needed. This would typically be 230VAC in an application required to operate from 120VAC lines where the THD will be low and further reduction is uneccesary as well as from 220-240VAC voltage supplies where THD reduction offers the maximum benefit. For this reason the inductor (LPFC) value is calculated based on THD optimization, setting the off time to 15µs at the peak of the line voltage at the nominal level from the following formula:

$$LPFC = \frac{15 \cdot 10^{-6} \cdot \left(VBUS - \sqrt{2} \cdot VAC_{NOM(RMS)}\right) \cdot VAC_{NOM(RMS)} \cdot \eta}{2\sqrt{2} \cdot POUT} \quad [H] \quad [10]$$

The switching frequency at the peak of the line voltage can be calculated for a specified input voltage according to:

$$fs = \frac{VAC^2 \cdot (VBUS - \sqrt{2} \cdot VAC) \cdot \eta}{2 \cdot POUT \cdot LPFC \cdot VBUS} \quad [Hz] \quad [11]$$

3.3 Loop compensation

In order for the converter to provide high power factor and low THD the loop response must be slow enough that the on time remains effectively constant (except for on time modulation) throughout each line frequency half cycle as explained by equation 6. Since the AC line frequency is 50-60Hz the error amplifier gain has to roll off at a lower frequency. The recommended value for this cut off frequency (or bandwidth) is 20Hz to give the best possible loop response without degrading the power factor. The loop speed is determined by the compensation capacitor CCMP whose value is calculated from the transconductance of the error amplifier g_m (approximately 100µΩ^{-1}) as follows:

$$C_{CMP} = \frac{g_m}{2\pi \cdot f_c} = \frac{100}{2\pi \cdot 20} = 0.796 \quad [\mu F] \quad [12]$$

A value of 0.68µF is typically used in the application and is suitable for all power and voltage ranges.

3.4 Voltage feedback

The DC output bus voltage is regulated using a resistor divider to provide feedback to the error amplifier through the VBUS input. The cycle by cycle current sense signal is also superimposed onto this DC voltage however this can be ignored for the purposes of calculating the voltage divider. The internal reference for the error amplifier VBUSREG is nominally 4.1V in the IRS2505L. The resistor divider values are calculated as follows where two equal series resistors RB1 and RB2, are used for the upper branch of the divider:

Boost PFC circuit

$$R_{VBUS} = \frac{VBUSREG \cdot (R_{B1}+R_{B2})}{VBUS-VBUSREG} \quad [\Omega] \quad [13]$$

RB1 and RB2 are selected for minimal power dissipation:

$$P_{RB1} = P_{RB2} \approx \frac{V_{BUS}^2}{2 \cdot (R_{B1} + R_{B2})} \quad [W] \quad [14]$$

3.5 Output capacitor calculation

The output bulk capacitor (CBUS) can be a single capacitor rated at 450V for nominal output voltages up to 410V, or two 250V rated capacitors in series for higher output voltages. This ensures that under startup and transient conditions the output voltage will not exceed the maximum voltage ratings. If two series capacitors are used each must have approximately twice the calculated value of CBUS. This value can be calculated according to:

$$C_{BUS} = \frac{P_{OUT}}{2 \cdot \pi \cdot f_{IN(MIN)} \cdot \Delta V_{RIPPLE} \cdot V_{BUS}} \quad [F] \quad [15]$$

Where $f_{IN(MIN)}$ is the minimum line input frequency (set at 50Hz in the spreadsheet) and ΔV_{RIPPLE} is the acceptable peak to peak ripple amplitude. It is not recommended for ΔV_{RIPPLE} to be greater than 20V.

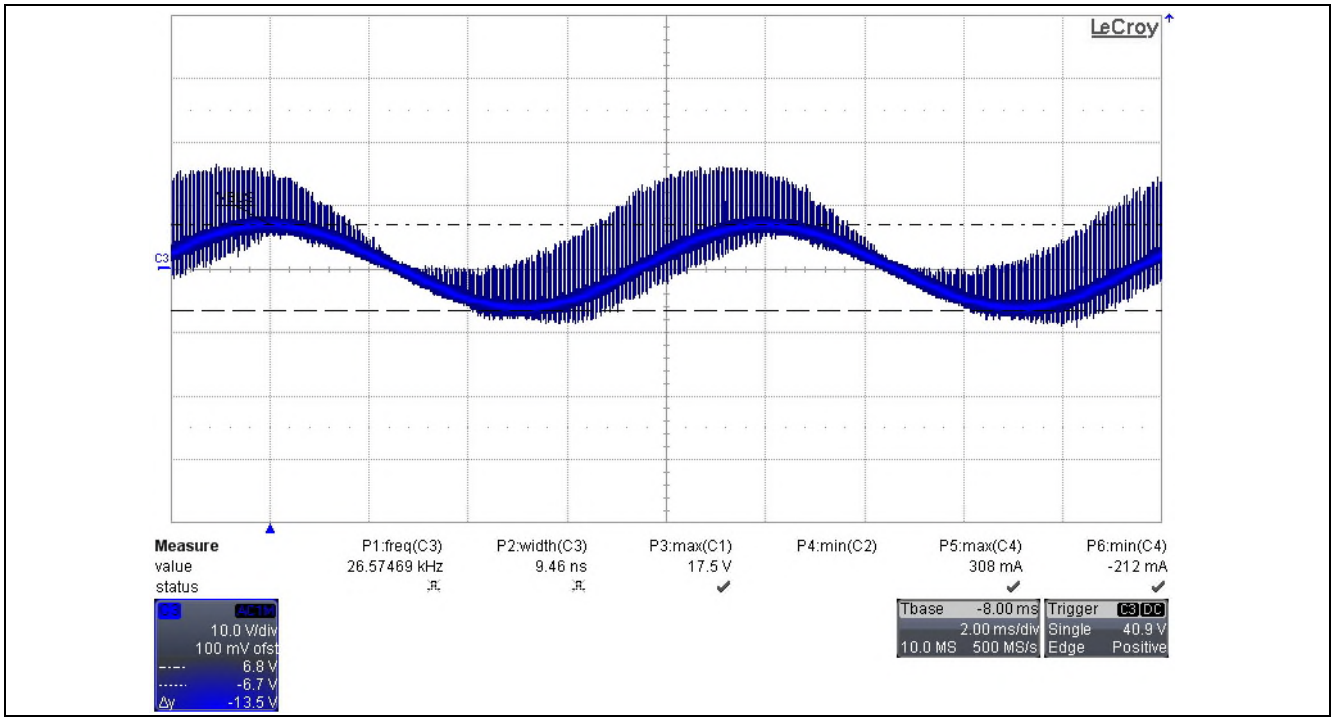


Figure 6 Output voltage ripple at 90W load, input 90Vac, 50Hz, Cout = 56µF

4 Zero crossing detection

The zero crossing (ZX) detection in CrCM PFC controllers is usually done via an auxiliary winding of the inductor through a dedicated pin. However the IRS2505L is able to detect this through its advanced gate driver system, which in addition to switching the MOSFET on and off is able to detect the rising and falling edges of the drain voltage coupled through the drain to gate capacitance C_{GD}. This smart ZX detection can eliminate the need for an auxiliary winding.

During the on time the gate drive output is pulled high then at switch off the gate is pulled low for a period of t_{PD} (~500ns) after which it is clamped to a level of VPFCOFF which is one diode forward voltage drop ~0.6V. For the remaining off time the gate voltage is floating between zero and VPFCOFF with a weak pull up. Since VPFCOFF is well below the gate threshold the MOSFET remains safely off.

At gate drive switch off the drain voltage transitions positive to VBUS causing the gate voltage to be pulled up to VPCOFF. As the inductor current falls to zero the drain voltage transitions negatively coupling to the gate and causing the voltage to fall. A new switching cycle is started when the gate voltage falls below VPFCZX- (0.4V) with the gate drive going high again.

In order for the IRS2505L smart ZX detection to operate, there must be sufficient voltage headroom between the peak input voltage at maximum line input and the DC output bus voltage. A value of at least 70V is recommended! However, in many cases the converter is required to work with smaller headrooms, in which case, some additional aid is then needed to ensure ZX triggering occurs near the peak input voltage at high line. If LPFC has an auxiliary winding this can be easily implemented by adding a series resistor and capacitor RZX and CZX to the gate drive output (shown in figure 2), which could be 10kΩ and 220pF. If no auxiliary winding is available then a low value (in the 100pF range), high voltage capacitor may be placed between the gate and drain of the MOSFET to increase coupling. If this value is too high it will add to switching losses and over stress the IRS2505L gate driver output.

In both cases adding a schottky diode from the gate output to ground (anode to ground) protects the IRS2505L from being over stressed.

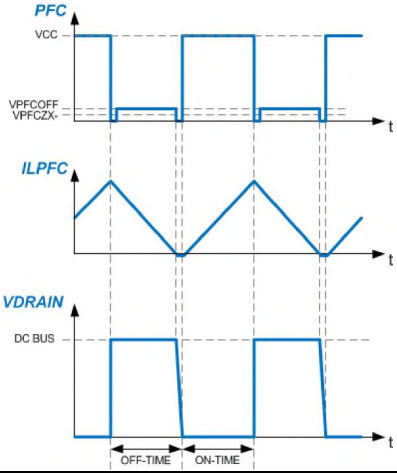


Figure 7 PFC gate voltage, PFC inductor current and PFC MOSFET drain voltage

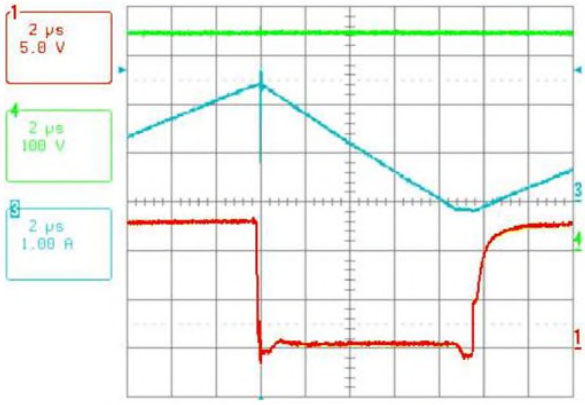


Figure 8 PFC gate voltage (red), PFC inductor current (blue) and DC bus voltage (green) waveforms

5 Over current protection

The IRS2505L incorporates cycle by cycle over current protection, which causes the gate drive to switch off rapidly if the source current exceeds a fixed threshold VBUSOC+. A current sense resistor (RCS) is included in the circuit as shown in figure 2, whose value is calculated according to equation 9. The voltage from RCS is coupled to the voltage divider by CC1 and RC1 shown below in figure 9. The IRS2505L internally separates the current sense signal from the voltage feedback signal.

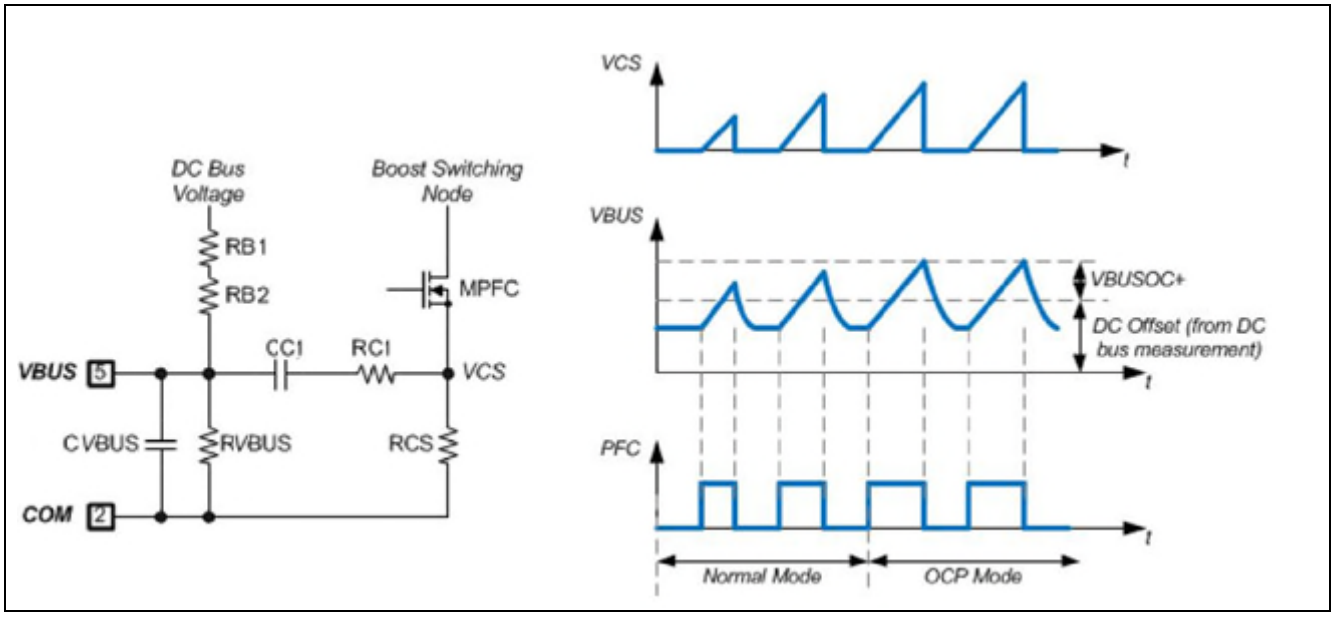


Figure 9 Cycle by cycle current sensing network and protection

As the line voltage is reduced or the load increased the regulation loop increases the on time to try to maintain the output voltage. As the on time increases, the peak current increases as shown in the VCS waveform diagram of figure 8. The VBUS waveform shows the current superimposed onto the voltage feedback through AC coupling. When this voltage reaches VBUSREG plus VBUSOC+ the gate drive is switched off. The values of RC1=1kΩ, CC1=100nF may be used in any circuit. CVBUS must be selected to provide a triangular shaped ripple as shown in the second graph of figure 9 and the purple waveform of figure 10, without reducing amplitude significantly.

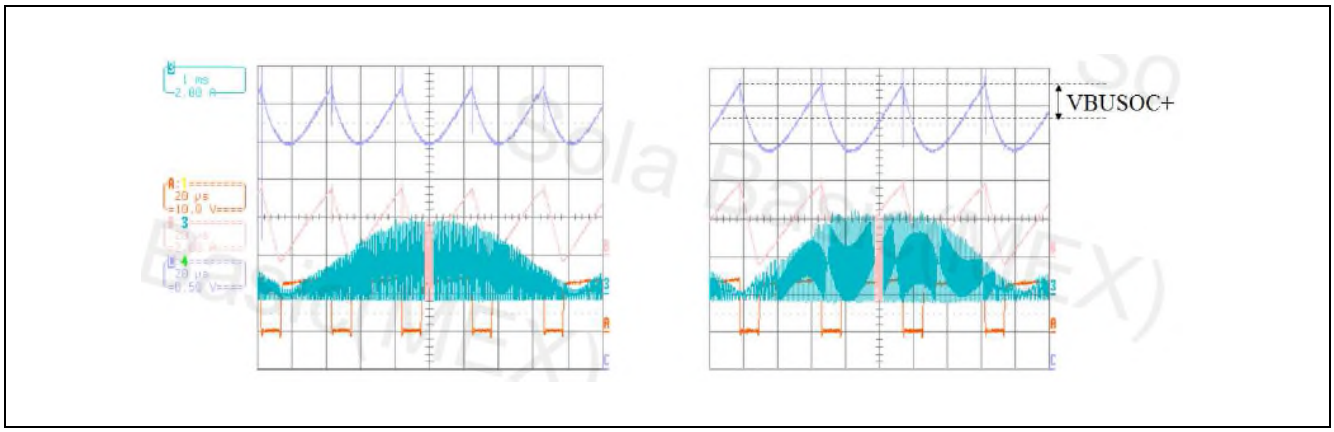


Figure 10 VBUS voltage (purple), VRCS (blue), Zoomed VRCS (red), Zoomed gate voltage (orange)

Over current protection

The left waveform in figure 10 shows normal operation where the peak of VBUS does not reach VBUSREG plus VBUSOC+ and the right waveform shows clipping of the sinusoidal current envelope as the peak of VBUS reaches this threshold to trigger cycle by cycle current limit.

6 Design spreadsheet

A design spreadsheet entitled “IRS2505L PFC Design Calculations” is available which contains all of the calculations included in this application note. Please be sure to the latest version (Rev 3 at the time of writing). The spreadsheet assumes a line frequency in the 50-60Hz range.

The following example shows the calculations for a PFC stage with the following input parameters:

POUT = 90W, VACMIN = 90V_{RMS}, VACMAX = 265V_{RMS}, VBUS = 420V and VACNOM is chosen at 230V_{RMS} for THD optimization. These values are input into the yellow fields of the “User input parameters” section of the spreadsheet. If there is insufficient headroom between the peak of the high line input voltage and the output voltage the VBUS value color will change to red as a warning (see page 7).

Parameter	User Input Value	Units	Description
VAC_nom	**230**	Vrms	Nominal r.m.s. input voltage
VAC_min	**90**	Vrms	Minimum r.m.s. input voltage
VAC_max	**265**	Vrms	Maximum r.m.s. input voltage
VBUS	**420**	VDC	DC bus voltage **(RED indicates insufficient headroom without additional ZX trigger network)**
Max pp Ripple	**15**	Vpp	Pk-Pk output voltage ripple **(RED indicates too high)**
POUT	**90**	W	Output power

Table 2 User input parameters

The peak current at minimum line input ($IPFC_{MAX}$), inductor value (LPFC) and minimum frequency at the nominal and minimum line input voltages are then calculated:

Parameter	Calculated Value	Units	Description
I_LPFC_max	**3.0**	Apk	Maximum peak inductor current at VAC_min
LPFC	**1.2**	mH	PFC inductance value
f_min(nom)	**52**	kHz	Minimum switching frequency at VAC_nom
f_min(min)	**24**	kHz	Minimum switching frequency at VAC_min
Cout	**45.5**	uF	Output capacitor

Table 3 Boost circuit calculations

The values of RVCC1, RVCC2 and CVCC1 can then be entered so that the startup time can be calculated according to equation (1). If the selected value for CVCC is smaller than the calculated minimum value, the value color changes to red as a warning that the converter may not start up because the VCC holdup time is insufficient.

Design spreadsheet

Parameter	Calculated Value	Units	Description
CVCC2	0.1	µF	VCC filter capacitor value (fixed)
CVCC1 MIN	39.1	µF	VCC capacitor minimum value to startup
CVCC1	39	µF	VCC capacitor value (user input value) **(RED indicates value too small!)**
RVCC1	150	kΩ	VCC start-up resistor no. 1 (user input)
RVCC2	150	kΩ	VCC start-up resistor no. 2 (user input)
PRVCC	0.105	W	VCC start resistor highest dissipation
t_startup	1.25	s	VCC start-up time at VAC_min

Table 4 IRS2505L VCC supply

In table 4 the selected value of CVCC1 is slightly lower than the calculated minimum value causing it to be displayed red as a warning. However the difference is marginal and this value would work in practice.

Next CCMP is calculated according to equation (9) and the current sense resistor according to equation (6). Then the output voltage divider lower resistor (RVBUS) is calculated based on user defined values of RB1 and RB2 whose power dissipation is also calculated according to equation (2). The fixed values are also given for RC1, CC1 and CVBUS:

BW	20	Hz	Loop speed bandwidth (user input)
CCMP	0.80	µF	CMP pin compensation capacitor value

RCS	0.19	Ω	MOSFET current-sensing resistor value

RB1	1.0	MΩ	DC Bus divider resistor no. 1 (user input)
RB2	1.0	MΩ	DC Bus divider resistor no. 2 (user input)
RVBUS	19.7	kΩ	Lower DC Bus divider resistor value
RC1	1.0	kΩ	Current-sense coupling resistor value (fixed)
CC1	0.1	µF	Current-sense coupling capacitor value (fixed)
CVBUS	1.0	nF	VBUS pin filter capacitor value (fixed)

Table 5 IRS2505L programming components

The final section simplifies the inductor design process. The user can select a core size from a drop down menu, which will retrieve the parameters required for a built in database. Alternatively the user can enter the parameters manually for a core that is not included in this database. The user then selects values for the fill factor and air gap as well as current density and number of strands of wire for the winding. The spreadsheet calculates the peak flux density (BMAX) and the wire size needed to support the current. The BMAX cell turns red if the value is too high and the inductor would saturate based on the chosen set of parameters. The user may then adjust the core and gap sizes until a suitable result is reached. Since the method used in this case is iterative, the spreadsheet saves the user time by removing the need for manual calculations.

Design spreadsheet

Inductor Parameter	Value	Unit	*Comments*	User Defined Core	Enter Value	Unit
Core Selected:	E32/16/9		*Core specs can be found in the manufacturer's datasheet*	Core Type:		
Effective area (Ae)	83	mm2		Effective area (Ae)		mm2
Effective length (le)	74	mm		Effective length (le)		mm
Core factor Σ(l/A)	0.89	mm-1		Core factor Σ(l/A)		mm-1
				Winding Area (Aw)		mm2
Fill Factor	0.4		*Typically 0.7, varies between 0.3-0.7 depending on core*	Winding Length (lw) (optional)		mm
Air Gap	1	mm	*Select an airgap that gives BMAX between 0.25-0.30*			
BMAX	0.40	T	*Bmax > 0.3T -- Increase airgap or select a larger core*			
Primary Turns (Np)	110					
Current Density	4	A/mm2	*Range 4 to 8A/mm2*			
Number of Strands	2		*Range 1 to 8*			
Primary Wire Gauge	25	AWG				
Available Winding Area	64.4	mm2	*Winding Area > Available Area --- Select Larger Core*			
Required Winding Area	83.56	mm2				

Table 6 Inductor design

7 PCB layout guidelines

To achieve correct circuit functionality and avoid high-frequency noise problems, proper care should be taken when designing the PCB layout. Poor PCB layout can lead to noise coupling into sensitive IC inputs, which can cause interference with normal operation resulting in instability, poor EMC performance, audible noise and component failure. The following layout guidelines (see Figure 10) should be in order to reduce circuit problems, shorten design cycles, and to increase reliability and manufacturability:

1) Keep high frequency, high current traces (PFC MOSFET drain) as short as possible. This will help reduce noise due to parasitic inductance of PCB traces.
2) Keep high frequency, high voltage switching nodes (PFC MOSFET drain) away from sensitive circuit nodes (CMP pin, VBUS pin). This will reduce noise coupling that can cause unstable operation of the IRS2505L.
3) Place high-frequency noise decoupling capacitors directly at the IC pins (VCC pin, VBUS pin). This will ensure the best possible filtering against high-frequency noise.
4) Place all critical timing capacitors directly at their IC pins (CMP pin). This will help prevent faulty switching due to noise coupling.
5) Do not connect power ground through IC/small-signal ground including the programming component ground traces. Keep separate traces for power and small-signal grounds and connect small-signal ground to power ground at a single point only. This is essential to prevent high-frequency noise from occurring on critical small-signal nodes or IC pins, which can cause circuit malfunction or failures.
6) Keep the distance from the power MOSFET to the gate drive pin as short as possible. This reduces the parasitic inductance in the gate drive traces to minimize signal distortion and ringing and possible voltage spikes due to deficient gate drive switching. This helps to help prevent latch up due to voltage over or under-shoot.
7) Always place a limiting resistor from the auxiliary supply to VCC. This will prevent stress and possible damage to the IRS2505L due to high-current spikes from the auxiliary supply that could cause electrical overstress.
8) Place critical sensing nodes (current-sensing resistors, etc.) as close to the IC as possible. This will help eliminate false triggering or circuit malfunction due to noise being coupled onto to sensitive control signals.
9) Ensure the PFC inductor does not saturate under worst case line/load and temperature conditions. Saturation results in currents with very high di/dt levels that can induce noise everywhere in the circuit causing many different noise related issues.

An example PCB layout for the IRS2505L following good design practices is shown in figure 11.

PCB layout guidelines

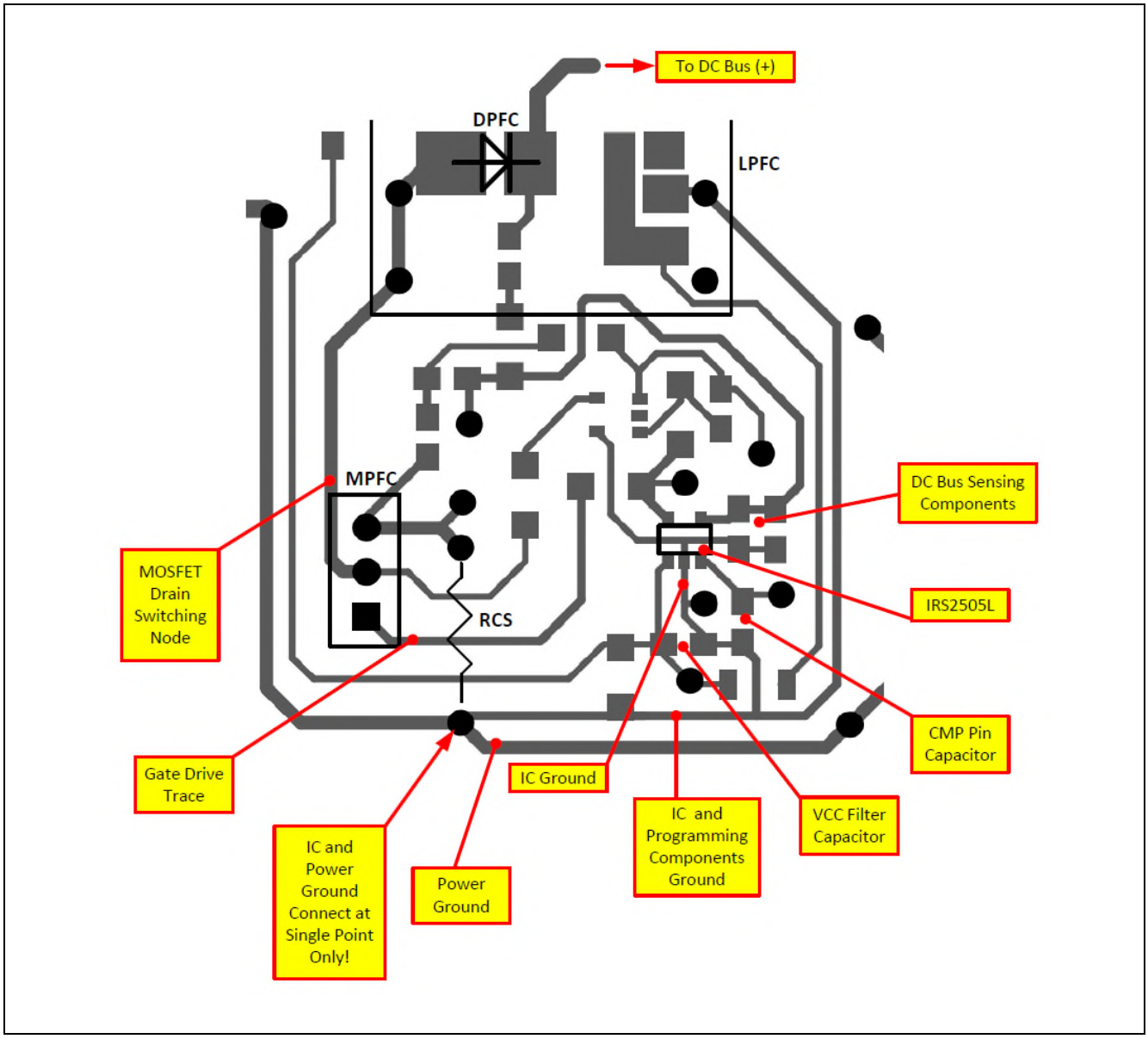


Figure 11 IRS2505L example PCB layout

8 Appendix

8.1 Inductor design equations

Calculation of the effective permeability (μ_e) of a core with a specified gap (g) based on initial permeability (μ_i) quoted in the datasheet for the grade of material:

$$\mu_e = \frac{\mu_i}{1+\left(\frac{g \cdot \mu_i}{l_e}\right)} \quad [12]$$

Calculation of the A_L value for a core based on the previously calculated effective permeability (μ_e), the effective length (l_e) and cross-sectional area (A_e) quoted in the core data sheet:

$$A_L = \frac{\mu_0 \cdot \mu_e \cdot 10^6}{\Sigma\left(\frac{l_e}{A_e}\right)} \quad [\text{nH/Turn}^2] \quad [11]$$

Calculation of the number of turns required for the target inductance (LPFC):

$$N = \sqrt{\frac{LPFC}{A_L}} \quad [13]$$

Calculation of the peak flux density:

To avoid saturation this should not exceed the maximum data sheet limit for the core material.

$$B_{MAX} = \frac{N \cdot IPFC_{MAX} \cdot A_L}{A_e} \quad [\text{T}] \quad [14]$$

Calculation of maximum RMS current in a strand of wire based on diameter (mm) and current density (J_{MAX}) (A typical value of current density is 4A/mm^2):

$$I_{RMS} = \frac{\pi}{4} \cdot d^2 \cdot J_{MAX} \quad [\text{A}] \quad [15]$$

8.2 PFC basics

Total harmonic distortion (THD) is defined as the RMS value of harmonic distortion from all components of an AC signal excluding the fundamental, expressed as a percentage of the RMS of the fundamental. In other words it quantifies the amount by which the signal deviates from a pure sinusoid:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} A_n^2}}{A_1} = \frac{\sqrt{\left(A_{RMS} - A_1^2\right)}}{A_1}$$

Where A_1 is the RMS amplitude of the fundamental and A_{RMS} is the total RMS value of the complete current waveform. THD of the current is often referred to as THDi to differentiate it from the voltage THD.
It should be noted that THDi is not the only quantity contributing to power factor (PF) since phase shift between current and voltage inputs is not factored into the THD calculation. Power factor is defined as the ratio of the *real power*, which is utilized by the load, to the *apparent power* which also includes *reactive and distortion power*. Power factor (PF) includes *displacement* power factor (DPF) resulting from phase displacement created by circuit reactances and *distortion* power factor (DF) produced by harmonics.

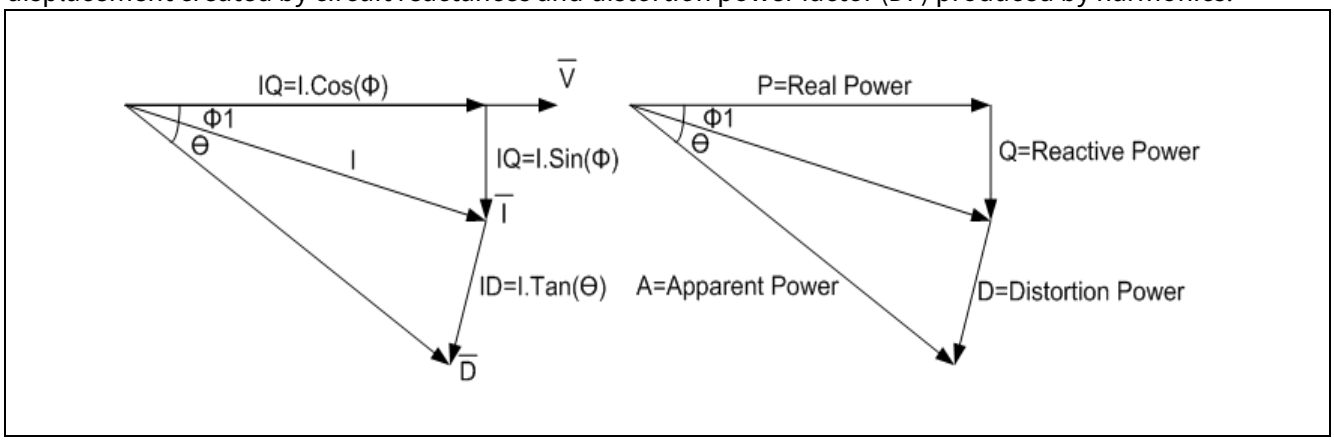


Figure 12 Power vector diagram

The general formula for power factor is:

$$PF = \frac{P_{RMS}}{V_{RMS} \cdot I_{RMS}}$$

Where P_{RMS} is the real power consumed by the load.

The *displacement power factor* is given by the formula:

$$DPF = \cos(\phi)$$

Where, ϕ is the phase shift between the voltage (assumed to be a purely sinusoidal) and current.
If the current is non-sinusoidal (containing harmonic distortion) the fundamental, ϕ1 is used.

The following formula gives the *distortion power factor:*

Appendix

$$DF = \frac{1}{\sqrt{1 + THD^2}}$$

These are combined to give the total power factor according to:

$$PF = \frac{\cos(\phi_1)}{\sqrt{1 + THD^2}}$$

Where ϕ_1 refers to the phase shift between the voltage and the *fundamental* component of the current and THD is expressed as a fraction (usually converted from a percentage).

Measurement of current THD

For accurate current THD test results a good quality AC power source is necessary!
If the AC supply voltage contains harmonic distortion, the current THD will increase. This is because the power factor correction circuit operates by controlling the shape of the input current to match that of the voltage as well as possible.
Accurate current THD measurements can be made only with a good quality sinusoidal AC supply such as from an electronic AC source. Auto-transformers and isolation transformers often used in laboratory bench set-ups, which operate directly from the AC line do not produce pure sinusoidal voltage output.

References

[1] IRS2505LPBF µPFC™ control IC datasheet, International Rectifier (an Infineon company).

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First Release

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