International IOR Rectifier

Application Note AN-986

ESD Testing of MOS Gated Power Transistors

Table of Contents

Page

1. Background 1
   Introduction 2

2. A model for the ESD test circuit
   A Simple Model and its Implications 3

3. Experimental verification 5
   Observations 6

4. Classification of devices 7

5. Tests with different connections 8

6. Conclusions 9

All semiconductor components have been proven to be static sensitive to varying degrees. Users' concerns on this subject has resulted in a significant effort being expended on the following areas:

1. Device design aimed at improving ESD tolerance
2. Device handling techniques
3. Device characterization for ESD
4. ESD inspection of incoming devices

Unfortunately, MOS-gated power transistors have not yet benefited from a specific characterization effort and users have been specifying, by default, testing and inspection procedures that were aimed at integrated circuits. This note analyzes the behavior of MOS-gated power transistors undergoing an ESD test, without discussing the fundamental premise that a capacitive discharge is a meaningful simulation of an ESD event.

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TITLE:

ESD Testing of MOS Gated Power Transistors

Notices:
(HEXFET is the trademark for International Rectifier Power MOSFETs)

Summary:

Topics Covered:

- I. Background
- II. A model for the ESD test circuit
- III. Experimental verification
- IV. Classification of devices
- V. Tests with different connections
- VI. Conclusions

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I. Background

Introduction

All semiconductor components have been proven to be static sensitive to varying degrees. User's concern on this subject has resulted in a significant effort being expended on the following areas:

1. Device design aimed at improving ESD tolerance
2. Device handling techniques
3. Device characterization for ESD
4. ESD inspection of incoming devices

Unfortunately, MOS-gated power transistors have not yet benefited from a specific characterization effort and users have been specifying, by default, testing and inspection procedures that were aimed at integrated circuits.

As shown in Figure 1, integrated circuits have specific input protection networks that rely on a combination of bypass and avalanche discharge to keep the voltage at the input pin within safe limits. Test methods have been developed to measure and classify the effectiveness of this input protection network, notably Method 3015 of MIL-STD-883 and the EIAJ IC-121-1981.

In these tests the effects of an electrostatic discharge are simulated by discharging a capacitor into the input pins of the IC. To take into account that a true electrostatic discharge can be generated by sources with different characteristics, two different test circuits have evolved, commonly referred to as the "Human Body Model" (HBM) and "Machine Model" (MM). As shown in Figure 2, the difference between these test circuits is in the RC values, the basic principle being the same.

These test circuits can be used to perform a pass/fail test (for inspection) or to take the IC to failure (for characterization). Since the discriminating parameter in these tests is the current waveform during the discharge, a preliminary characterization is necessary to establish the failure threshold for a given family and the correct current waveform below that threshold.

This note analyzes the behavior of MOS-gated power transistors undergoing an ESD test, without discussing the fundamental premise that a capacitive discharge is a meaningful simulation of an ESD event.

IR Application Note AN-986

(Section 2 of 6)

Title:

ESD Testing of MOS Gated Power Transistors

(HEXFET is the trademark for International Rectifier Power MOSFETs)

II. A model for the ESD test circuit

A Simple Model And Its Implications

The capacitive nature of the MOS gate suggests that a simple electrical model can describe the events occurring when a MOS-gated transistor undergoes ESD testing with circuits like those shown in Figure 2.

The model is shown in Figure 3, together with the equations to calculate the voltage and energy after the discharge. Two items are noteworthy:

a. The ratio between the initial voltage across C, and the final voltage across both capacitors ("discharge ratio") is determined by the capacitance values and is independent from the series resistance.
b. The energy lost during the discharge depends on the value of the capacitors and is independent from the value of the series resistance.

The following will show in detail that waveforms, discharge ratio and other characteristics are representative of the discharge of one capacitor into another. Meanwhile, "prima facie" evidence of the validity of this model can be obtained from the oscilloscope traces of Figures 4a and 4b.

With reference to the circuit in Figure 6, one of the traces shows the voltage across C1 (initially at the supply voltage), the other shows the voltage between gate and source of the D.U.T. (initially at 0). When C1 is shorted to the gate, a discharge occurs and the common voltage decays exponentially. If the scale on the two traces were the same, the two waveforms would overlap.

The most far-reaching implications of this model are the following:

1. Apart from the exponential decay, as will be explained later, current flows at one instant only: when the relay establishes the contact between the capacitor and the gate. Since the gate capacitance of power devices is significant, the discharge current is a large spike, limited only by the series resistance. As shown in Figure 7b, the spike lasts for a period of time in the order of tens of nanoseconds and it is difficult to capture on digitizing oscilloscopes or memoscopes. In fact, the waveform in Figure 7b is not a reliable representation; different waveforms could be obtained with successive samplings1. In the absence of an input protection network, the shape of this waveform, which is the discriminating parameter in Method 3015, is not conducive to the detection of gate degradation, even with good instrumentation. It follows that, in attempting to apply Method 3015 to MOS-gated power transistors, the spirit of the test will certainly be violated and, because of the difficulty of the measurement, its results are questionable.

   It will be shown in the next section that some subtle changes do occur at the breakdown limit of the oxide. This does not contradict the above statement since these changes are too minor to be the discriminating parameter for an acceptance test. A failure, on the other hand, is easily detected by the fact that the voltage goes to zero after the discharge.
2. Since the Human Body Model and the Machine Model differ only in the component values and since the series resistance does not change the "discharge ratio," the two test circuits will yield the same results for the same value of C, and initial voltage. It follows that the high value resistor in the Human Body Model is basically irrelevant to the outcome of the test, which is totally determined by the initial charge in the capacitor. This is clearly shown by Figures 4a and 4b, where the voltage after the discharge is the same, in spite of the fact that the series resistance is much different.

   Thus, the existence of two different test circuits for the evaluation of MOS-gated power transistors does not seem to be justified. On the other hand, in their proper field of application, i.e., ICs, these two tests circuits will yield different results.
3. If the behavior of a MOS gate under capacitive discharge is, in principle, as simple as the discharge of a capacitor into another capacitor, it follows that, once these capacitances are known, the outcome of the test is fairly predictable: the device under test will fail if the final voltage is above the dielectric strength of its gate oxide. Hence, the ESD test circuits, when applied to MOS-gated power transistors without input protection networks, do nothing more than measure, in a complex and inaccurate way, the gate dielectric strength of gate oxide.

IR Application Note AN-986

Title:

ESD Testing of MOS Gated Power Transistors

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III. Experimental verification

Although the series resistor does not, in principle, affect the outcome of the test, taking this measurements without any resistor is somewhat dangerous because the circuit is highly underdamped and significant overshoots occur at the time of the discharge. On a different time scale, the oscilloscope traces of Figure 4a or Figure 5a (taken under the same conditions) show significant and dangerous amounts of ringing (Figure 5b and 5c). For this reason a series resistor of 470 was inserted in its test circuit (Figure 6) a series resistor of 470 Ohms and as a result, the spread of voltages at the point of failure became much narrower. A larger resistor may be required if the circuit is not compact and with little stray inductance.

A series gate resistor is also useful in improving the accuracy of the discharge ratio measurement. If no discrete resistor is present in the discharge circuit, the resistance of the gate structure itself will be the only current limiting component and a significant voltage drop will be developed across it. This will prevent making an accurate reading of the voltage across the gate capacitance.

An additional feature of the test circuit in Figure 6 is the debouncing latch. The contacts of a mercury relay do not bounce if the coil is not released. Unfortunately, this is what happens when the relay is controlled by a momentary pushbutton.

The exponential decay that occurs after the charge transfer requires some explanation. With reference to Figure 4, this decay has a time constant of approximately 9ms. The capacitive element of this time constant is the series combination of the two capacitances and it comes up to approximately 210pF. It follows that the resistive component is in the order of 43 MOhms with a peak current of approximately 700nA. Since the gate leakage is normally in the order of 10nA (gigaOhms), it was concluded that this current flows mostly in the oscilloscope probes.

While it would be desirable to reduce this leakage by three orders of magnitude, it is clearly not possible with the instrumentation that can be reasonably made available to perform these tests. Thus, it would be appropriate for Method 3015 to provide procedural guidelines to limit these errors.As shown in Figure 3, for a given value of C1 and a given transistor, the discharge ratio is a function of its input capacitance when drain and source are both connected to ground. Unfortunately, this value is not normally specified in the data sheet and has to be specifically measured or derived from gate charge values taken under (or extrapolated down to) these conditions.

This was done for International Rectifier devices with the results tabulated in Table I, together with the discharge ratio, calculated from the equation in Figure 3 for a 235pF capacitor, and other useful information which follows later.

The calculations, confirmed by the ESD testing, show that a large die requires an initial voltage in the order of 1kV in 235pF to take the gate to its failure point. Since the supply immediately available for experimental verification was limited to 820V, limited testing was done on International Rectifier HEX-4 dies and none on HEX-5, 6 and 7. These values of voltage are unlikely to be reached in the parts of an assembly machine.

The value of 235pF should not be seen as an appropriate value to simulate an ESD event. It was chosen as a convenient value in light of the limits of the available power supply. A large range of capacitance values would have been appropriate to confirm that ESD testing conforms to the model of Figure 3.

It will be noticed, from Table I, that logic level gates are not necessarily weaker. Since discharge ratio, input capacitance and gate dielectric strength are inter-related, a device with lower dielectric strength or lower input capacitance will not necessarily perform poorly under ESD testing.

To confirm that the ESD test amounts to nothing more than a gate dielectric strength test, three batches of devices were split in two groups. One was taken to failure on the ESD test circuit shown in Figure 6, the other was taken to failure on a curve tracer. The results are shown in Table II.

NOTES:

(1) Refer to AN-964 for die characteristics and nomenclature to identify die type in a part number

(2) Ratio between capacitor voltage after the discharge divided by its voltage before the discharge capacitor value: 235 pF for Machine Model and 100 pF for Human Body Model

(3) Survivability of device to ESD test as guaranteed by gate dielectric strength test at the end of the assembly line. Capacitor value: 235 pF for Machine Model, 100 pF for Human Body Model. Test assumed at 30V for standard gates and 15V for logic level gates

(4) Gate voltage after the discharge at which failure occurred. Capacitor value: 235 pF for Machine Model, 100 pF for Human Body Model

(5) Gate dielectric strength as measured on curve tracer

(6) Max voltage from available supply was 820V. No failures occurred at that voltage

Several observations can be made on the basis of these tests:

1. The gate dielectric strength measured on a curve tracer was consistently between 45 and 50V for a logic level gate and between 70 and 80V for a standard gate. Generally speaking, the gate dielectric strength of a large population of devices should follow a distribution whose standard deviation is determined by the accuracy of the process control and with the lower end truncated by the final test. This, however, was not apparent in the curve tracer tests, possibly due to the limited accuracy of this type of instrument or to the limited number of the devices that were measured.

   The fail points measured in the test circuit of Figure 6, translated into gate voltage by means of the discharge ratio (Table I), are in agreement with the gate dielectric strength. Due consideration should be given to the limited accuracy of the results from the ESD test method and to the factors listed in points 3 and 4 below.

2. The agreement between the calculated and measured discharge ratios is an indirect confirmation of the correctness of the values of capacitance listed in Table I.

3. In the process of establishing the dielectric strength on the curve tracer it was found that the gate leakage had a knee at the point of failure. This knee is similar to that of a p-n junction, except symmetrical in voltage, with a similar tendency to "walk out." If this leakage was contained within 100 microA or so, the gate would not be damaged. To verify this, 11 devices where "gate avalanched" and then tested on the ESD tester of Figure 6. Their failure points were in the same range as those of 12 devices from the same lot which had not undergone this preliminary stress. The results are shown in Table II for lot code 7P9F.

   This behavior was confirmed with the ESD test circuit. As the initial voltage of C1 is increased, a point is reached at which the voltage after the discharge does not increase any further because the gate leakage exerts a clamping action. As shown in Figure 8, in spite of the fact that the initial voltage is increased by approximately 30V, the two traces corresponding to the voltage after the discharge are superimposed. If the initial voltage is increased further, the gate punctures (figure 9) at a voltage that is approximatly 10V higher. The discrepancy between this number and what was measured on the curve tracer is probably due to the more forgiving nature of the ESD test.

   No attempt was made to explain the energy absorbing capability of the gate oxide.

4. The more forgiving nature of the ESD test is also apparent from some aggregate results shown in Table I that show some lots having a failure point under ESD testing that is higher than their dielectric strength measured with the curve tracer. In the specific case of Figures 8 and 9, gate clamping action started at approximately 600V, but failure did not occur until well over 700V. The gate dielectric strength on a curve tracer would have been measured at a voltage equivalent to the 600V, while the ESD test failure would have been measured at over 700V.

   Should this waveform be used as a discriminating parameter (Method 3015), the results would be affected by personal judgment to an unacceptable level. As a matter of fact, the lots with significant gate energy capability resulted in a wider spread of failure voltages in the measurements.

   Once again, a curve tracer test would provide the same information in a simpler and more accurate form.

   Other lots were failed in the same test circuit to increase the statistical significance of our findings. The results are also listed in Table I.

IR Application Note AN-986

Title:

ESD Testing of MOS Gated Power Transistors

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IV. Classification of devices

Method 3015 has provisions for a "Classification Testing" (para. 3.3), based on the "failure threshold" of a device in the test circuit (HBM), as a guideline for handling procedures.

As it has been shown, the device performance under ESD testing can be calculated from 3 parameters: gate capacitance, gate dielectric strength and capacitance of C1. The results will be on the conservative side since they ignore the energy capability of the gate.

Given a value for C1, two main classifications can be generated: one that uses the gate voltage guaranteed by final test and one that uses the actual dielectric strength.

The first appears in Table I in the column labeled "Min. ESD Capability." Since gate integrity of all devices is tested at the end of the assembly line to a voltage that is normally 30V for standard gates and 15V for logic level gates, the initial capacitor voltage that is required to take the gate to 30 (or 15) volts can be easily calculated. This voltage is the guaranteed ESD withstanding capability (per Figure 2) of that particular device.

The ESD classification based on the actual gate didectric strength is also listed in Table I in the column "Voltage at Failure." Considering that this classification is not a design parameter but an indicator for handling procedures, it is suggested that an average and a standard deviation be used, rather than a minimum value. Being aggregates, they provide a more accurate and useful representation of the population behavior.
Smaller values of C1 would, of course, give higher classification values.

IR Application Note AN-986

Title:

ESD Testing of MOS Gated Power Transistors

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V. Tests with different connections

For the sake of completeness, ESD sensitivity of MOS-gated transistors in different connections should also be mentioned.

a. *Gate shorted to drain.* With Vgs = Vds > 0, the transistor will go into conduction as soon as its threshold is exceeded, thereby shorting the capacitor. With Vgs = Vds < 0, if the device is a MOSFET, the internal diode shorts the capacitor. If the device is an IGBT the leakage in the reverse direction exerts a clamping action between 20 and 50V that discharges the capacitor very rapidly.

b. *Gate shorted to source.* With Vds = Vdg > 0, nothing happens until the voltage across C1 exceeds the breakdown voltage of the transistor, at which point the transistor goes into avalanche. The energies involved in this test are normally much lower than those applied by a curve tracer in the process of measuring breakdown. With Vds = Vdg < 0, the behavior is the same as the one seen in the previous paragraph.

   It is felt that these connections are not representative of real device jeopardy. As far as power devices go, it is doubtful that the test circuits shown in Figure 2 would be an effective tool either in screening out potentially damaged devices or in establishing potential failure mechanisms. For this reason, the capacitive discharge tests were not performed for these connections.

IR Application Note AN-986

(Section 6 of 6)

Title:

ESD Testing of MOS Gated Power Transistors

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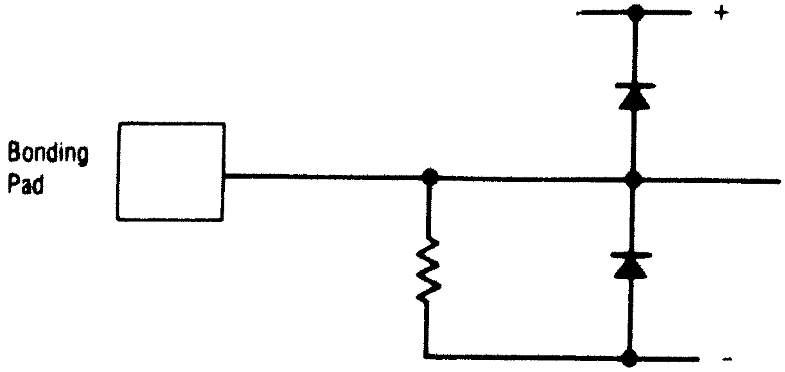
VI. Conclusions

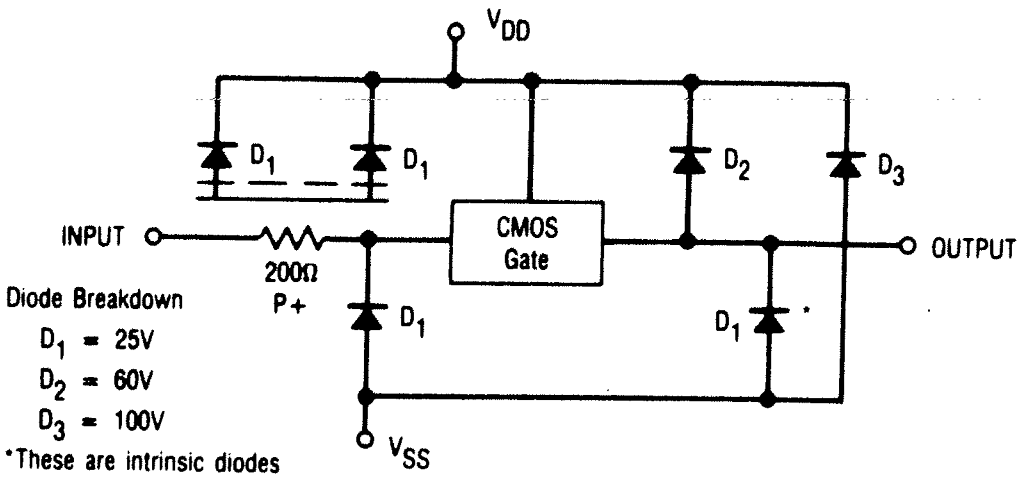
The use of a capacitive discharge into the gate to identify ESD sensitivity of a MOS-gated transistor does not seem to provide any additional information beyond what can be obtained more accurately from a curve tracer and simple calculations.

It is recommended that, for MOS-gated power transistors, the ESD test circuits shown in Figure 2 be replaced by a simple dielectric strength test performed with a curve tracer, completed by simple calculations, as per Figure 3.

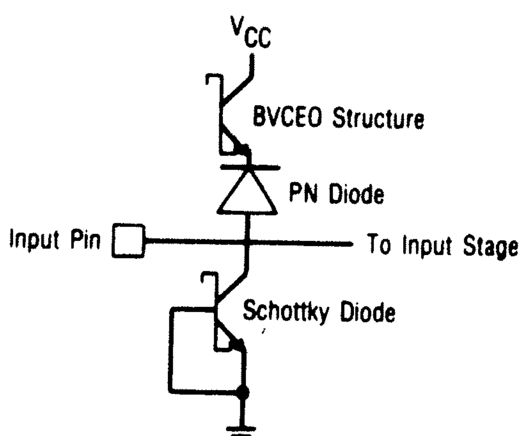
On the basis of these same calculations, a conservative level of ESD capability could be guaranteed on each and every device by a gate dielectric strength test performed in final test.



a. IR2110

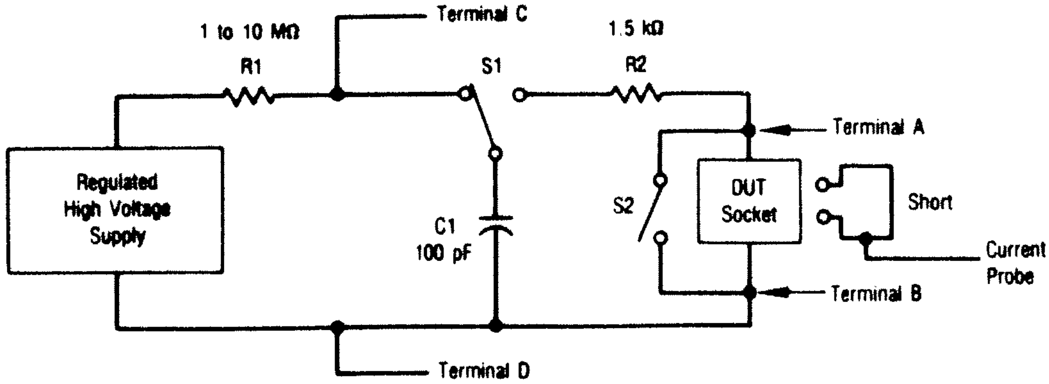


b. Standard CMOS input

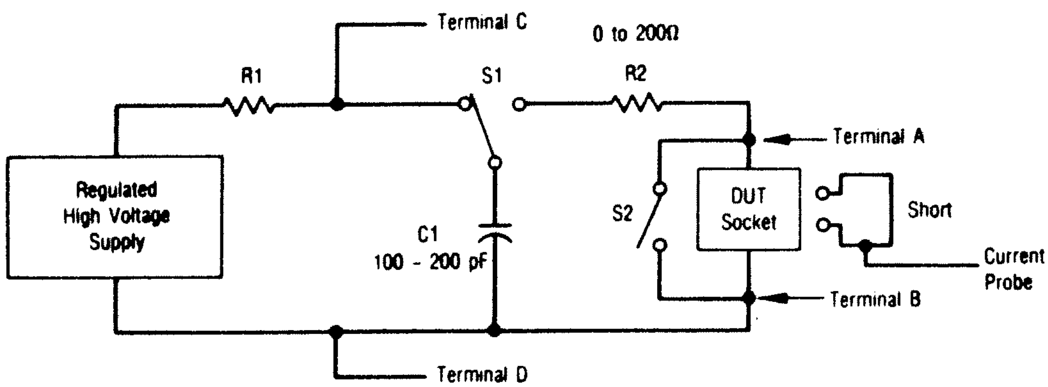


c. National Semiconductor's FAST input

Figure 1. Examples of input protection networks

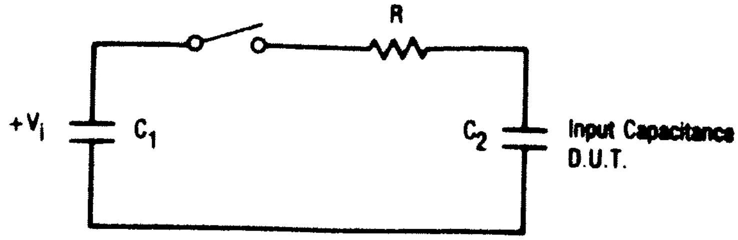


a. Human Body Model (MIL-STD-883 Method 3015)



b. Machine Model

Figure 2. ESD test circuits



From conservation of charge:

$$C_1 V_i = (C_1 + C_2) V_f$$

$$\frac{V_f}{V_i} = \frac{C_1}{C_1 + C_2} = \text{Discharge ratio}$$

The losses in the resistor during the discharge are

$$E = R \int_0^{\infty} i^2 (t)\, dt$$

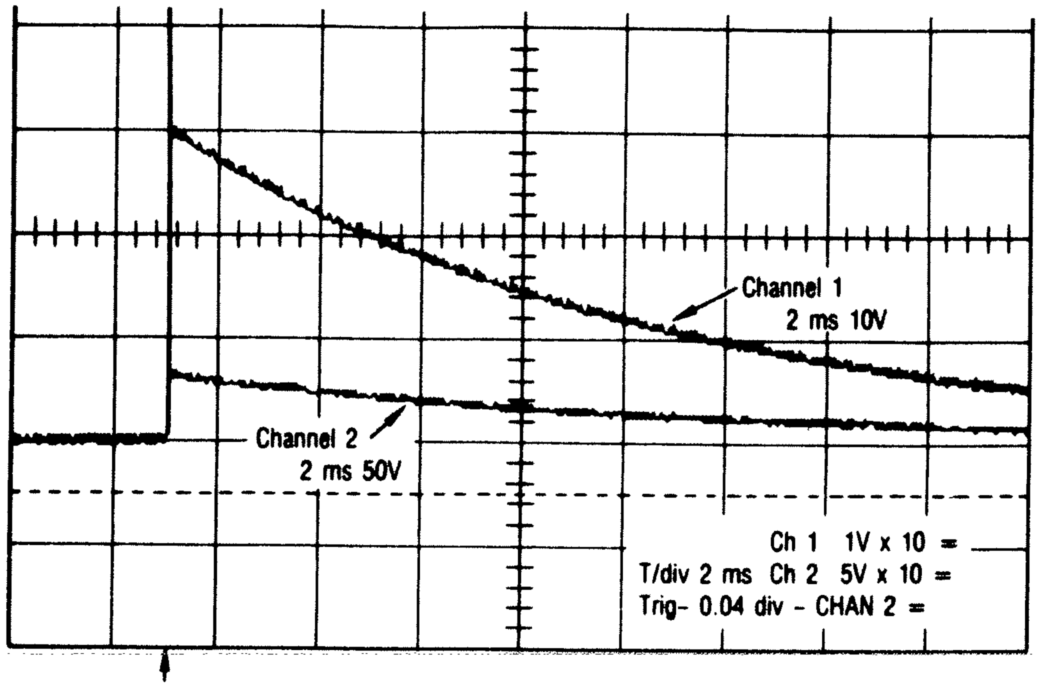
with $$i = \frac{V_i}{R} e^{-t/\tau}$$

and $$\tau = R \frac{C_1 C_2}{C_1 + C_2}$$

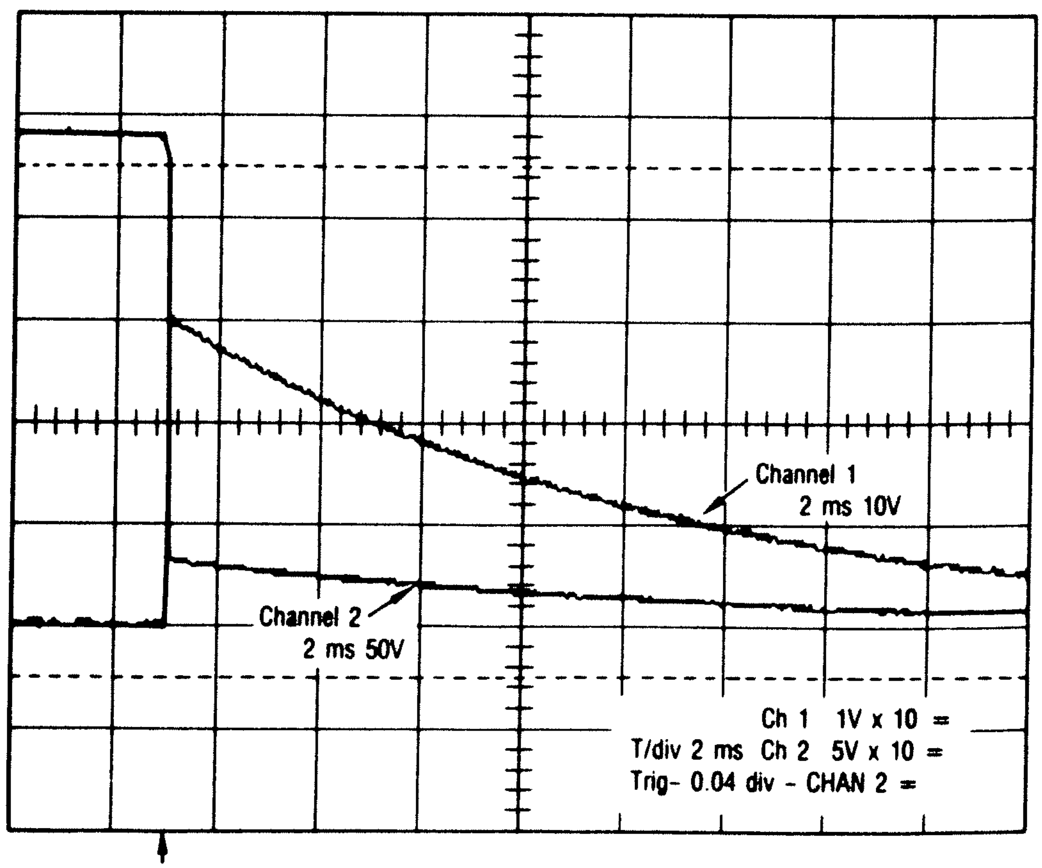
thus $$E = \frac{V_i^2}{R^2} R \int_0^{\infty} e^{-2t/\tau}\, dt = \frac{V_i^2}{R^2} R \frac{\tau}{2}$$

$$= \frac{1}{2} V_i^2 \frac{C_1 C_2}{C_1 + C_2} = \frac{1}{2} Q_i V_i \frac{C_2}{C_1 + C_2}$$

Figure 3. Final voltage at the end of the discharge and losses during the discharge

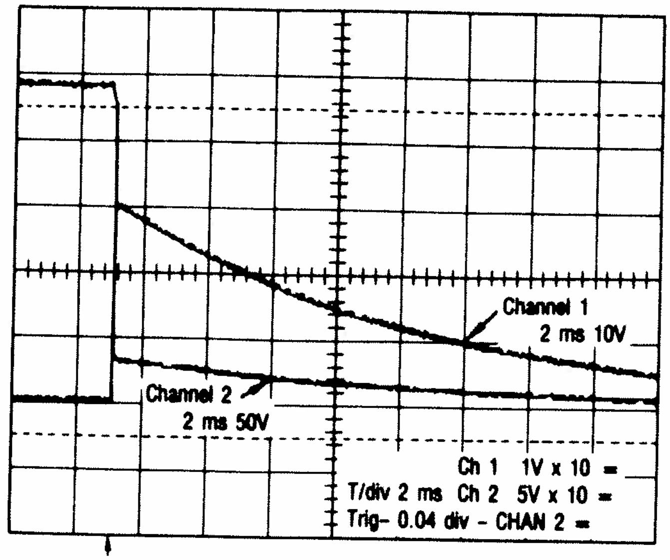


a. 100 Ohm series resistor

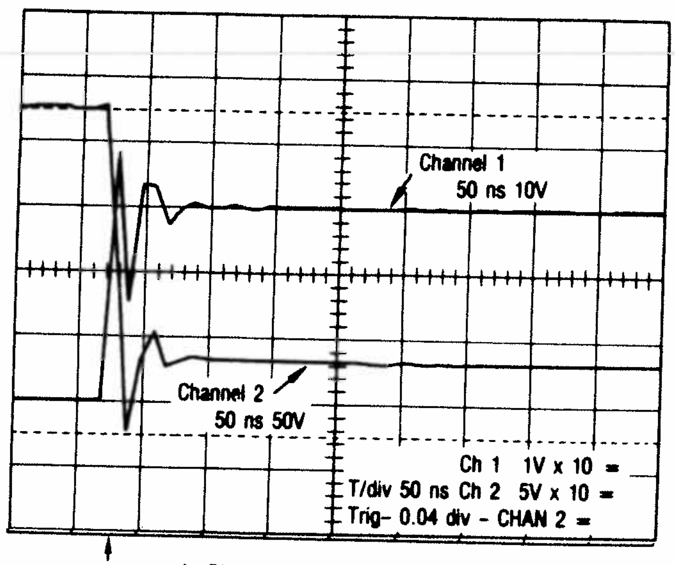


b. 1500 Ohm series resistor

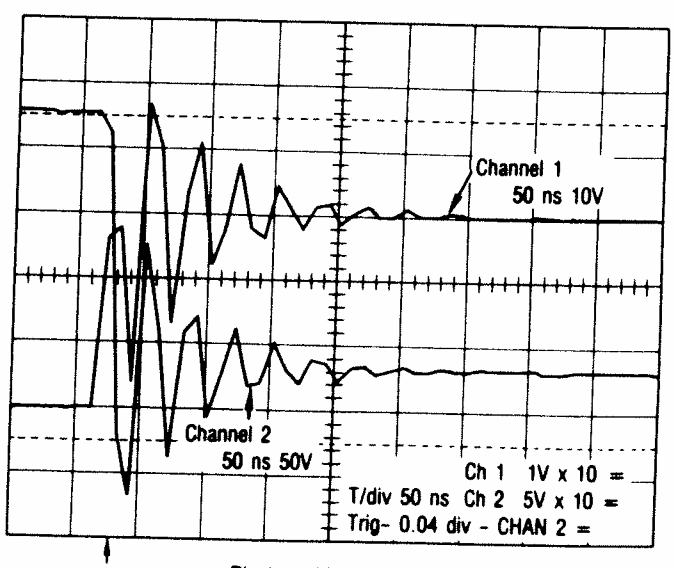
Figure 4. Capacitive discharge into gate of IRF730. Test circuit of Figure 6, initial voltage 240V



a. Ringing does not appear on a long time scale



b. Ringing with 100 Ohm resistor



c. Ringing without resistor

Figure 5. The need for a series resistor

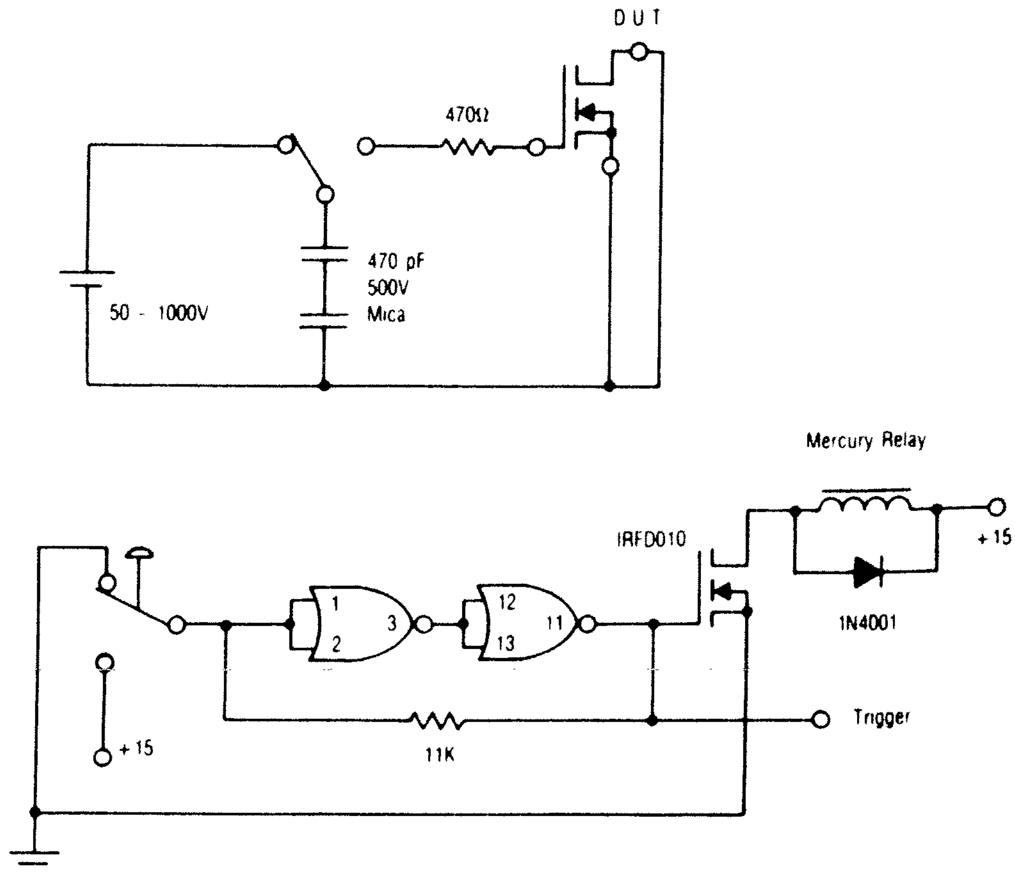
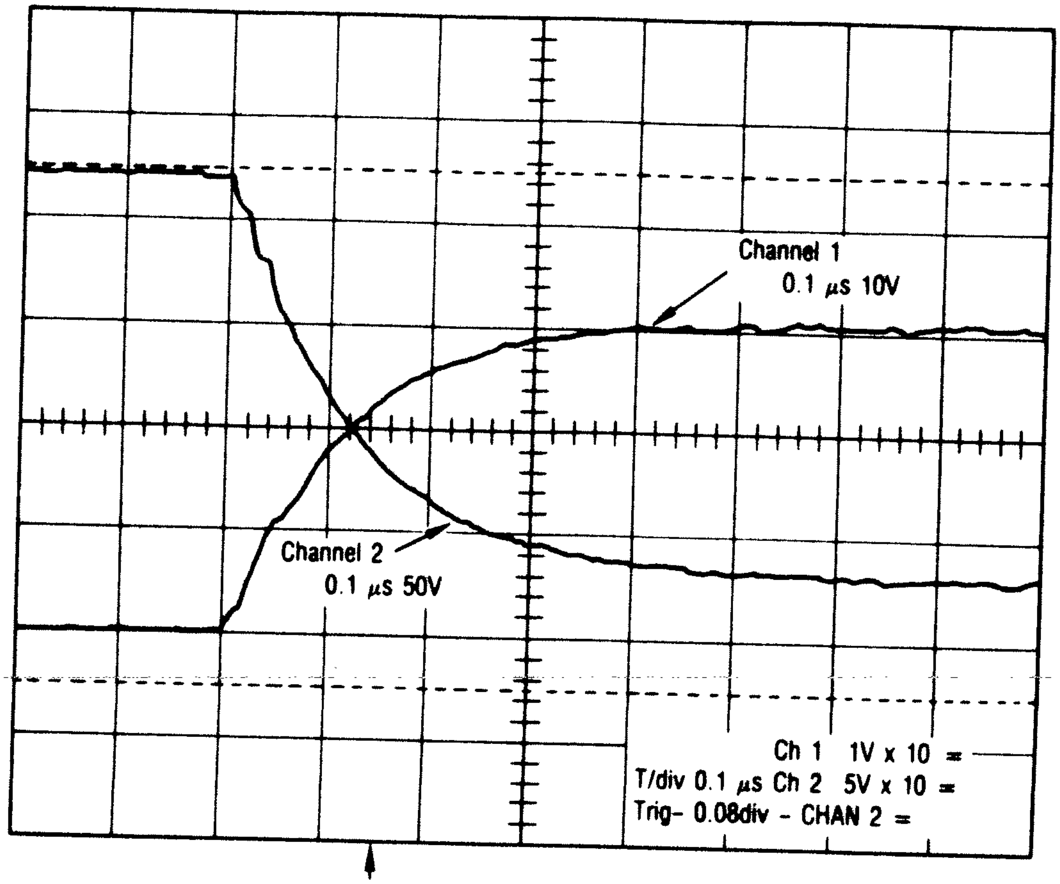
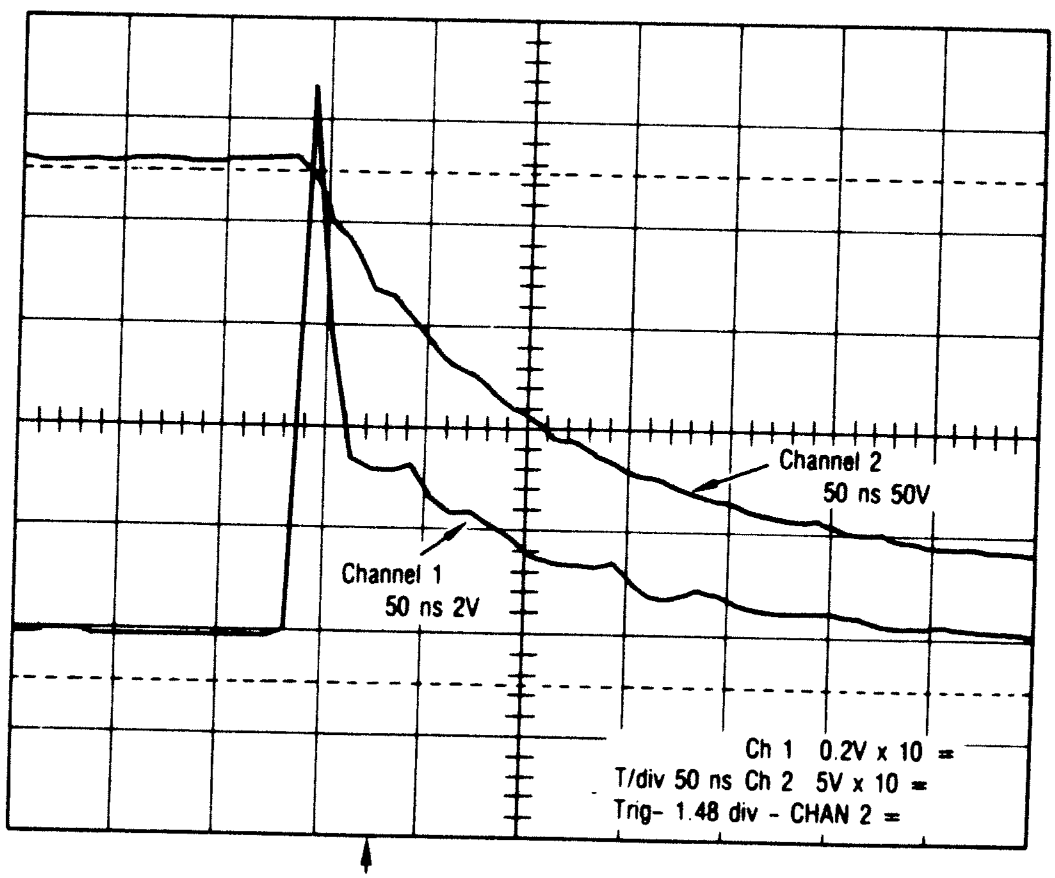


Figure 6. Schematic diagram of test circuit



a. Discharge voltages



b. Current (0.2A per div.) during discharge

Figure 7. Discharge waveforms into gate of IRF730.

Test circuit of Figure 6. Initial volt

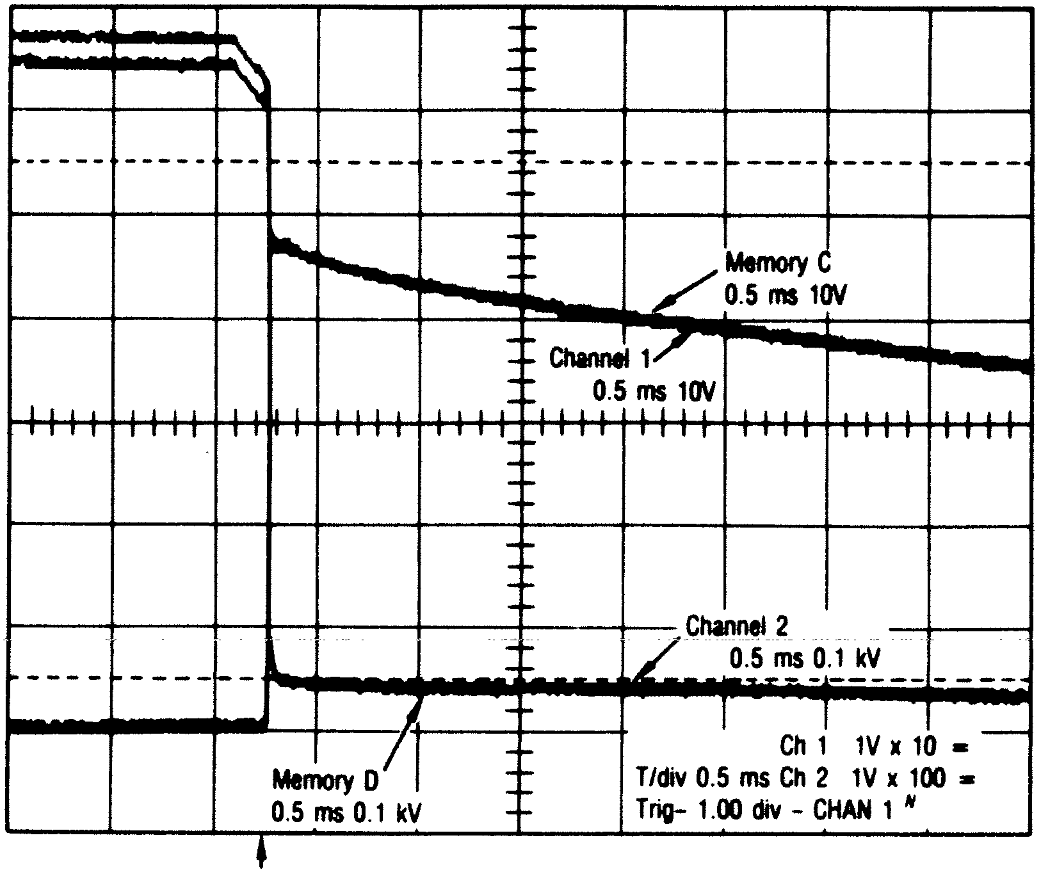


Figure 8. Discharge behavior at the limits of gate puncture. IRL530, lot 5U7C

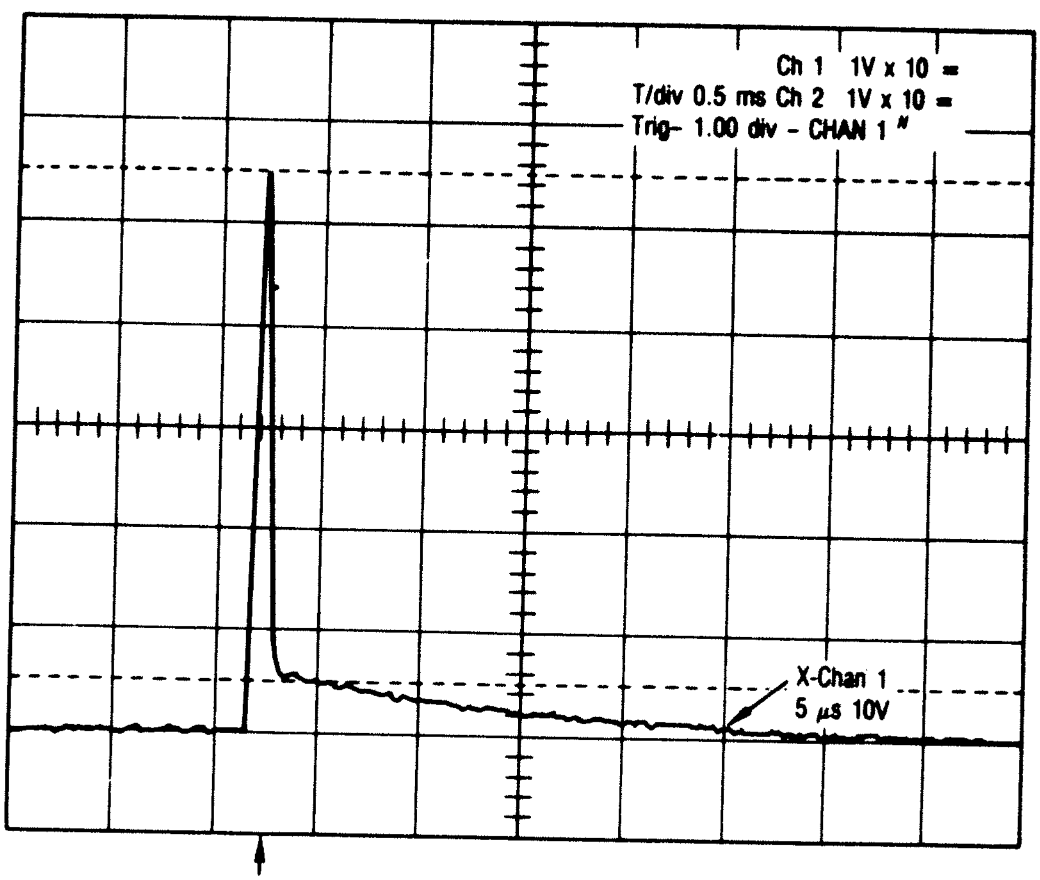


Figure 9. Gate voltage at failure. Initial voltage 773V, IRL530, lot 5U7C

Table 1

Die Type (1)	C_{iss} @ V_{ds} = 0 nF	Discharge Ratio Calcul. (2)	Meas. (2)	Min ESD Capab. (3)	Gate Voltage at Failure Range Avg (4)	Std Dev (4)	Gate Diel Strength (5)	Voltage at Failure Avg	Std Dev	Lot Code	Devices Tested
IRFC01x	0.72	0.246	0.240	122	65	2		271	8	7Z1D	19
IRFC110	0.48	0.330	0.326	91	84	9	75	257	28	7P9F	34
IRFC21x	0.38	0.382		79							
IRFCx1x	0.51	0.317		95							
IRLC014	1.23	0.160	0.167	94	48	2	50	288	12	9J6R	35
IRLC110	0.82	0.223	0.240	67	52	2	47	218	9	4A8C	14
IRFC9010	0.72	0.246		122							
IRFC9110	0.57	0.290		103							
IRFC9210	0.43	0.355		85			65	229	7	W5B7	13
IRFC02x	1.50	0.136	0.145	221	82	2	70	566	15	4W2G	8
IRFC120	0.97	0.196	0.214	153	76	3	68	355	16	2N4F	
IRFC22x	0.74	0.242		124							
IRFCx2x	1.00	0.190		158							
IRLC024	2.56	0.084	0.103	179	51	2	50	496	19	4L8M	26
IRLC120	1.65	0.124		121							15
IRFC9020	1.50	0.136		221							
IRFC9120	1.10	0.176		170							
IRFC9220	0.94	0.200		150							
IRFC03x	3.10	0.070	0.075	426			67	>820(6)		9Z9Z	15
IRFC130	1.90	0.110	0.121	272	81	2	70	666	19	3Q6Z	9
IRFC23x	2.44	0.088		341							
IRFCx3x	1.90	0.110	0.122	273	73	6	70	596	47	2P8D	20
IRLC034	5.32	0.042	0.051	355			44	>820(6)		8L8M	18
IRLC130	3.25	0.067	0.075	223	50	2	45	661	26	5U7C	20
IRFC9030	3.10	0.070		426		0					
IRFC9130	2.50	0.086	0.092	349			65	>820(6)		8K5Z	10
IRFC9230	2.33	0.091		328							
IRFC04x	6.17	0.037		818							
IRFC140	4.68	0.048		627							
IRFC24x	4.06	0.055	0.064	549			70	>820(6)		6T9K	11
IRFCx4x	4.00	0.055	0.068	541			75	>820(6)		3Q7N	12
IRLC044	10.58	0.022		690							
IRLC140	8.01	0.028		527							
IRFC9040	6.17	0.037		818							
IRFC9140	4.68	0.048		627							
IRFC9240	4.44	0.050		597							
IRFC054	11.15	0.021		1453							
IRFC150	9.21	0.025		1206							
IRFC25x	8.09	0.028		1063							
IRFCx5x	8.09	0.028		1063							
IRFCx6x	11.85	0.019		1543							
IRFCx7x	15.02	0.015		1947							

NOTES:

(1) Refer to AN-964 for die characteristics and nomenclature to identify die type in a part number

(2) Ratio between capacitor voltage after the discharge divided by its voltage before the discharge capacitor value: 235 pF

(3) Survivability of device to ESD test as guaranteed by gate dielectric strength test at the end of the assembly line. Capacitor value: 235 pF. Test assumed at 30V for standard gates and 15V for logic level gates

(4) Gate voltage after the discharge at which failure occurred. Capacitor value: 235 pF

(5) Gate dielectric strength as measured on curve tracer

(6) Max voltage from available supply was 820V. No failures occurred at that voltage

Table II

DEVICE No.	IRF510, LOT 7P9F		IRLZ24, LOT 4L8M		IRLU014, LOT 9J6R	
	FAILURE POINTS		FAILURE POINTS		FAILURE POINTS	
	Curve Tracer	ESD Tester	Curve Tracer	ESD Tester	Curve Tracer	ESD Tester
1	75	265	48		48	
2	75	269	48		48	
3	75	265	48		48	
4	75	258	48		48	
5	75	246	48		48	
6	75	267	48		48	
7	75	267	48		48	
8	75	259	48		48	
9	75	253	48		48	
10	75	254	48		48	
11	75	264		443	48	
12		272		496	48	
13		273		500	48	
14		141		492	48	
15		270		512	48	
16		273		470		298
17		273		503		297
18		234		488		281
19		228		509		278
20		268		524		297
21		276		502		290
22		273		496		301
23		269		482		253
24				492		295
25				522		285
26				503		302
27						274
28						291
29						291
30						286
31						285
32						290
33						300
34						296
35						269
Mean		257.3		495.9		287.9
Std dev		27.6		19.1		12.0