Application Note AN-1153

Low Cost Triac Dimmable CFL Ballast Using IRS2530D *DIM8*™

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INTRODUCTION

It has often been a disadvantage with electronic ballasts that they have been unable to be dimmed with a standard (phase cut) type of dimmer, particularly in the case of small integral ballast-lamp combinations commonly used in the home to save energy. This is due to the fact that, where there is no power factor correction, the ballast circuit input consists of a rectification stage followed by a large storage capacitor connected to the AC mains supply that provides the DC bus from which the high frequency half bridge and output section is supplied. In such a system current is drawn from the mains only near the peak of the mains voltage where the storage capacitor charges and not during the remainder of the mains half-cycle.

Virtually all domestic and professional dimming systems are based on *triacs.* These devices will conduct once they have been fired, only while current flows in excess of the holding current of the device. These dimmers work very well with a resistive load such as an ordinary Tungsten filament light bulb as the triac can be fired at any point during the mains half-cycle and will continue to conduct until very close to the end of the half-cycle as current is drawn continuously over this period. In this way the lamp current can be adjusted from maximum to zero.

A basic 120VAC dimmer circuit

When a compact ballast is connected to a circuit containing such a dimmer, the triac will only conduct if it is fired at a point during the mains half-cycle where the rectified mains voltage is greater than the storage capacitor voltage. In this instance the capacitor will be charged to the same voltage and the triac will then switch off. In this way it would be possible to adjust the DC bus voltage of the ballast to some extent by adjusting the triac firing point from 90º to 180º however this will not provide a satisfactory means of controlling the light output.

There is also an additional problem encountered due to the fact that a dimmer of this kind requires an inductor in series with the triac (Figure 1) to limit the rise time of the current when the device is fired. Without this inductor, mains current harmonics would be produced at frequencies high enough to cause considerable radiated and conducted interference problems. Since the load presented by a ballast circuit is effectively capacitive, when the triac is fired there will be ringing caused by the resonance of the suppression inductor of the dimmer and the capacitive load. This can cause the triac to fire and then switch off as the ringing output voltage swings above and then below the input voltage causing the current to fall below the holding current. This can occur several times during each half cycle, resulting in severe lamp flicker and loss of control of the output.

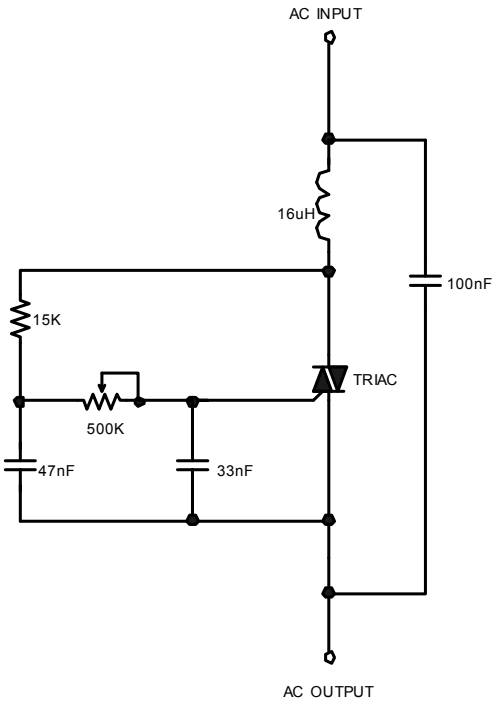


Figure 1: ***Triac Dimmer Circuit***

Triac dimmable CFL ballast

A system has now been developed, based around the 8-pin dimming ballast control IC IRS2530D, where the ballast is able to operate with minimal flicker over a considerable portion of the adjustment range of a dimmer. The light output may be controlled over this range from maximum output down to close to 10%.

In this system, the front end of the ballast has been designed so that when the triac in the dimmer has fired, it will remain on continuously until almost the end of the mains half-cycle. In addition to this there is circuitry that detects the firing angle of the triac and adjusts the lamp current by adjusting the switching frequency hence the controlling light output depending on the level set by the dimmer.

It should be noted that if the dimmer is set too low the triac will never fire when a capacitive load is connected. Also when the ballast is running and the dimmer is turned too low, there will be insufficient bus voltage for the ballast to be able to operate. Because of these factors, it is impossible for the ballast to operate over the complete range of adjustment of the dimmer. There will also be some hysteresis so when the ballast is being dimmed down and reaches the point where the lamp goes out, the dimmer has to be turned back up some way before the lamp will strike again.

This application note is about a dimming CFL ballast, dimmable with phase-cut dimmer, driving a single 15W spiral CFL lamp. The design contains an EMI filter and a dimming ballast control circuit using the IRS2530D. This demo board is intended to help with the evaluation of the IRS2530D dimming ballast control IC, and serve as an aid in the development of production ballasts using the IRS2530D.

CIRCUIT SCHEMATIC

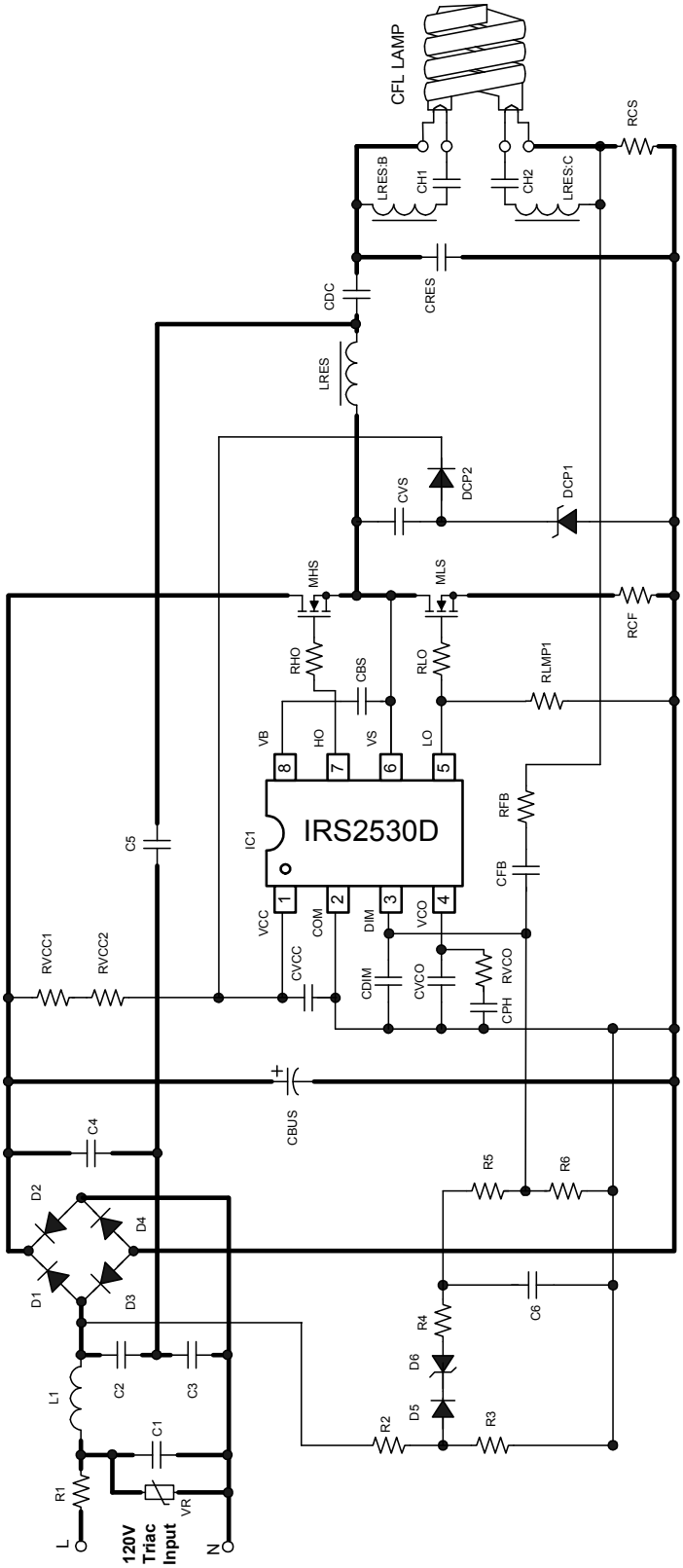


Figure 2: ***Circuit Schematic***

ELECTRICAL AND FAULT PROTECTION CHARACTERISTICS

Parameter	Units	Dimming Level	Value
Lamp Type			15W Spiral CFL
Input Power	[W]	100%	14
		Minimum	6.5
Input Current	[mArms]	100%	233
		Minimum	240
Lamp Running Voltage	[Vpp]	100%	240
		Minimum	450
Lamp Running Current	[mArms]	100%	160
		Minimum	20
Start Frequency	[kHz]		115
Run Frequency	[kHz]	100%	54
		Minimum	54.5
Preheat Time	[s]		1.3
Input AC Voltage Range	[VACrms]		80 – 135

Table 1: ***Electrical Parameter***

Fault	Protection	Ballast	Restart Operation
Brown-out	Non-ZVS	Increase frequency	Line voltage increase
Open filament	Crest Factor Over Current	Deactivates	Lamp exchange
Failure to ignite	VVCOFLT+	Deactivates	Lamp exchange
End of life	Crest Factor Over Current	Deactivates	Lamp exchange

Table 2: ***Fault Protection Characteristic***

FUNCTIONAL DESCRIPTION

IRS2530D *DIM8*™ Dimming Ballast Control IC

The IRS2530D is an application specific solution for dimming CFL and TL lamps in CFL or matchbox (small size ballasts) applications. It integrates all of the necessary functions for preheat, ignition and dimming control of the lamp, plus lamp fault protection, low AC-line protection, lamp exchange auto-restart, and a 600V half-bridge driver into a standard SO8 or DIP8 package.

The IRS2530D includes adaptive zero-voltage switching, non-zero voltage switching (ZVS) protection, as well as an integrated 600V bootstrap MOSFET. The heart of this IC is a voltage-controlled oscillator (VCO) with a dimming reference/feedback input. One of the biggest advantages of the IRS2530D is that it uses the VS pin (the mid-point of the half-bridge) for over-current protection and to detect non-ZVS conditions. The IRS2530D uses the RDSon of the low-side half-bridge MOSFET for current sensing each cycle when the low-side MOSFET is on. An internal 600V MOSFET connects the VS pin to the VS-sensing circuitry and allows for the VS pin to be accurately measured during the time when pin LO is high, while withstanding the high DC bus voltage during the other portion of the switching cycle when the high-side MOSFET is turned on. This eliminates the need for an external, precision current sensing resistor that is typically used to detect over-current. Please refer to the IRS2530D datasheet for further information including electrical parameters, a state diagram and a complete functional description.

When power is turned on, the IRS2530D first starts in Under Voltage Lockout (UVLO) mode. The UVLO mode is designed to maintain an ultra-low (<250µA) supply current, and to guarantee that the IC is fully functional before the high- and low-side output (HO and LO) gate drivers are activated. During UVLO, HO is 'low', and VCO is pulled down to COM for resetting the starting frequency to the maximum. LO is open circuit, and is used as a shutdown/reset input function for automatically restarting the IC when a lamp has been removed and re-inserted. In this CFL ballast application, however, this protection is not necessary and is disabled by pulling LO 'low' using resistor RLMP1.

Once VCC reaches the startup threshold (VCCUV+), the half-bridge FETs start to oscillate and the IC enters Preheat/Ignition Mode. At startup, VCO is 0V and the frequency starts at f_{MAX}. The frequency ramps down towards the resonant frequency of the high-Q ballast output stage, causing the lamp voltage to increase. During this time, the filaments of the lamp are pre-heated to their emission temperature to minimize the necessary ignition voltage and to increase lamp life. The voltage on pin VCO continues to increase and the frequency keeps decreasing until the lamp ignites. If the lamp ignites successfully, the IRS2530D enters the DIM mode. The resonant output stage transitions to a series-L, parallel RC circuit with the Q-value and operating point determined by

the user dim level (Figure 3).

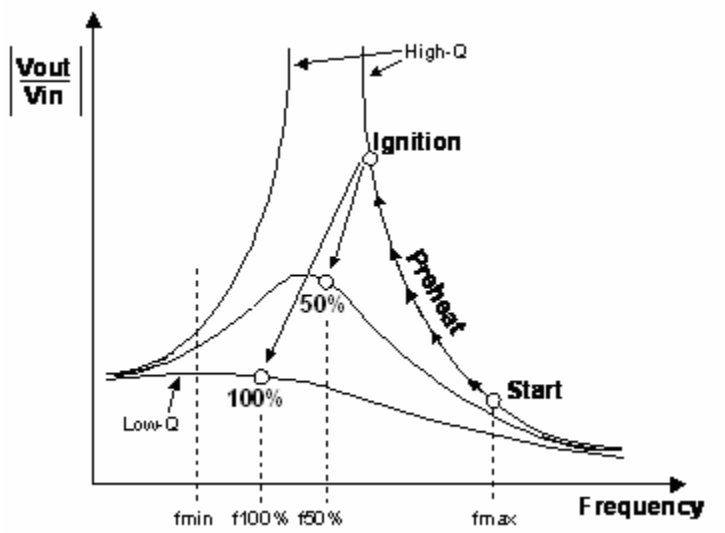


Figure 3: ***Resonant tank Bode plot showing lamp operating points***

Figure 4 shows the VCO voltage, the voltage across the lamp and the current through the lamp during Preheat, Ignition, and Run mode.

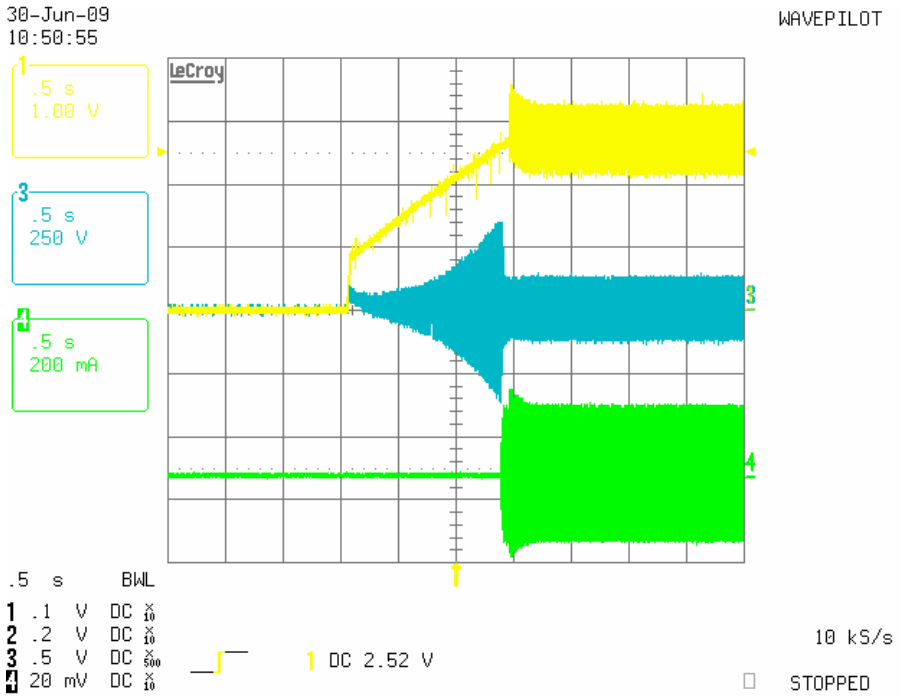


Figure 4: ***Preheat, Ignition, and Run mode: CH1 is the VCO voltage, CH3 is the voltage across the lamp, and CH4 is the lamp current***

IRS2530D-based solution for triac dimmable CFL ballast

When the dimmer triac is fired the current that flows must remain above the holding current until a point close to the end of the mains half cycle at which the voltage is very low. This is achieved by ensuring that the ballast draws current exceeding the holding current of a standard power triac as used in most dimmers with a capacitor network consisting of C2, C3, C4 and C5. When the ballast is operating, the point between LRES and CDC swings low when MLS is on. This charges C2 and C5 during the positive half-cycle of the mains voltage. When MLS switches off and MHS switches on, the voltage between LRES and CDC swings high causing C5 to be discharged through the capacitor C3. During the negative half-cycle of the mains voltage, the opposite happens between C2 and C3. The result is that a continuous series of current pulses are drawn from the input during the period when the triac has been fired until close to the end of the mains half-cycle.

The inductor L1 ensures that a continuous current is drawn from the input and that the triac does not switch off between pulses. In order to do this the inductor must store energy when current is being drawn to charge C5, and release this energy during the period when C5 is discharging.

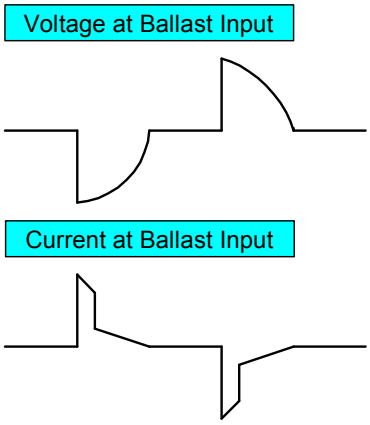


Figure 5: ***Voltage and current at ballast input***

The voltage waveform at the junction of D1 and D3, ignoring high frequency components is equivalent to the output voltage of the dimmer. With respect to the negative rail of the bus this will be a phase cut approximate sine wave with a DC offset such that the negative peak is at 0V. This is reduced by the voltage divider network of R2 and R3 which is then fed into D5 and D6. Only the signal representing the positive half-cycle of the mains is left at the anode of D6 which is then converted to a DC level via the filter of R4 and C6. Because the minimum dimming level occurs at a point where the dimmer is still capable of providing enough output for the ballast to operate, this voltage will never actually be zero. The DC level is further reduced with the voltage divider network of R5 and R6, and used as the dimming reference.

The AC lamp current is sensed by the resistor RCS, and the resulting AC voltage is coupled with the DC dimming level reference through feedback resistor (RFB) and feedback capacitor (CFB), and then fed into the DIM pin (pin #3) of IRS2530D (Figure 6). The DC + AC voltage at the DIM pin is regulated by the control loop such that the valley of the AC voltage always stays at COM. When the DC reference voltage at the DIM pin is decreased for dimming, the valleys of the AC voltage are pushed below COM. The dimming control circuit increases the frequency to decrease the AC lamp current until the AC valleys at the DIM pin are at COM again. When the DC reference in increased to increase the brightness level, the valleys of the AC voltage increase above COM. The control loop decreases the frequency to increase the AC lamp current until the AC valleys at the DIM pin are at COM again. In this way, the dimming control circuit keeps the AC lamp current peak-to-peak amplitude regulated to the desired value at all DC dim level settings.

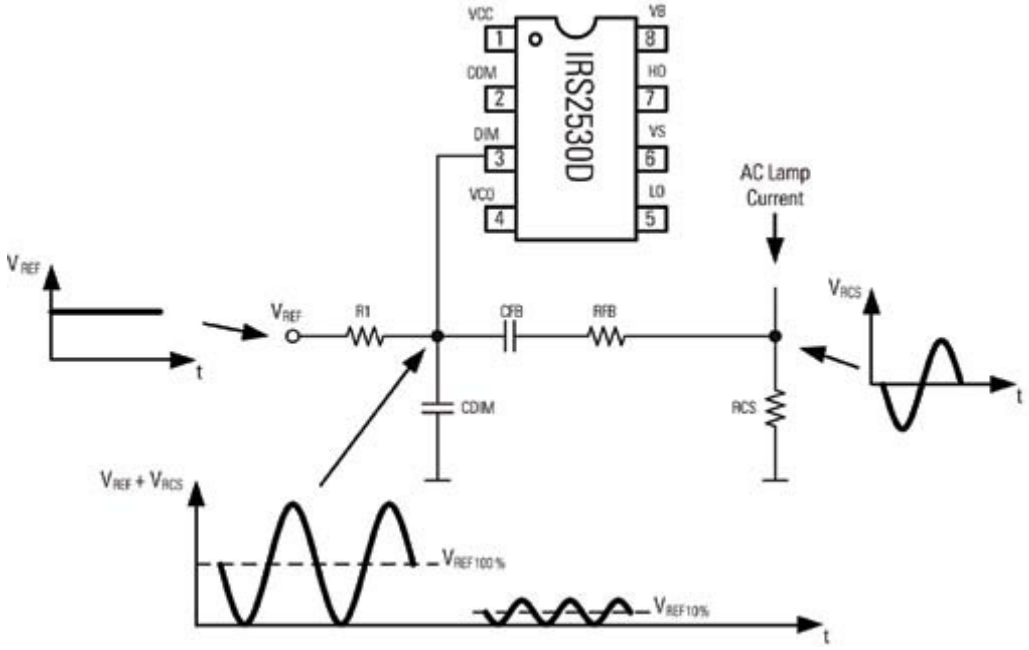


Figure 6: ***IRS2530D AC+DC Dimming Control Method***

Figure 7 shows the voltage at the DIM pin (pin 3 of IRS2530D), the VCO pin (pin 4 of the IC) and the VS pin (half-bridge) voltage during DIM Mode for maximum dimming level. Figure 8 shows these voltages at the minimum dimming level, just before the lamp turn off. The frequency does not change significantly between the maximum and minimum dimming level since the bus voltage is decreased as the lamp is dimmed.

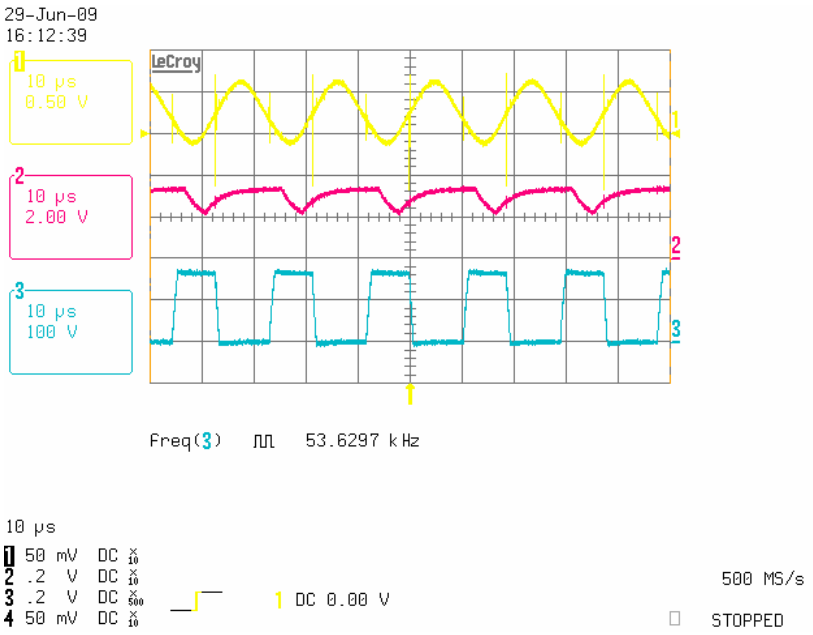


Figure 7: ***Maximum dimming level waveforms: CH1 is the DIM pin (pin 3 of IC1), CH2 is the VCO pin (pin 4 of IC1) and CH3 is the voltage at VS pin***

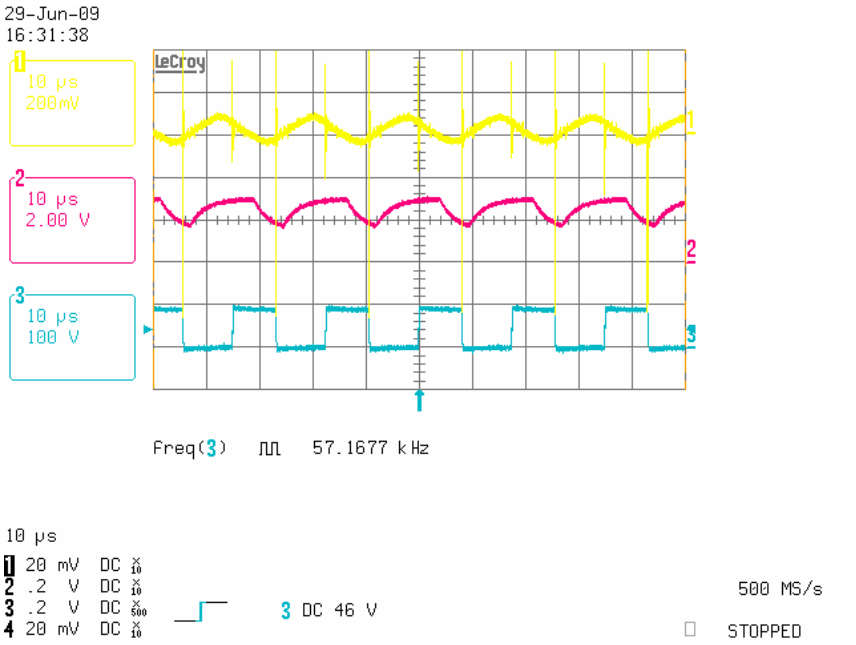


Figure 8: ***Minimum dimming level waveforms: CH1 is the DIM pin (pin 3 of IC1), CH2 is the VCO pin (pin 4 of IC1) and CH3 is the voltage at VS pin***

Figure 9 shows the voltage across, the current through and the power delivered to the lamp during DIM Mode for maximum dimming level. Figure 10 shows these waveforms for the minimum dimming level.

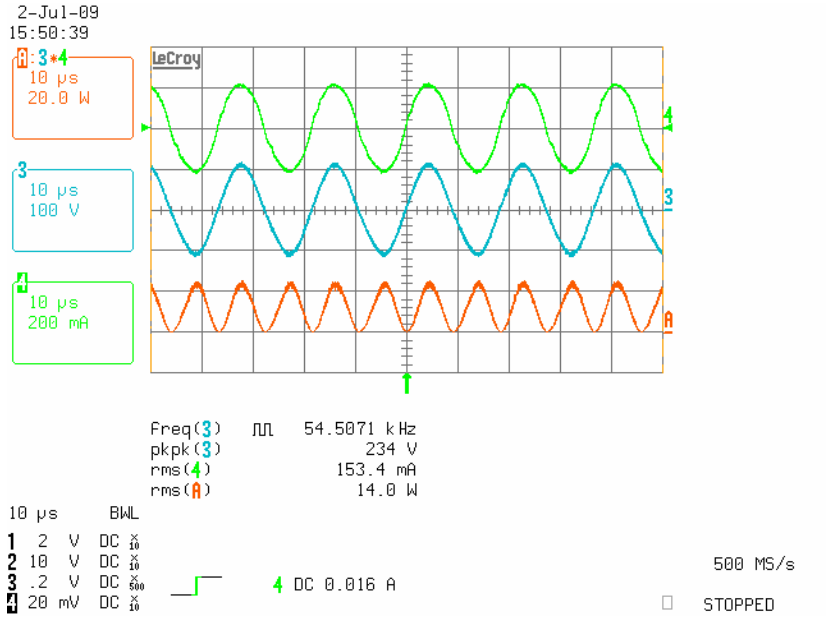


Figure 9: ***Maximum dimming level waveforms: CH3 is the voltage across the lamp, CH4 is the current through the lamp and CHA is the power of the lamp (voltage x current)***

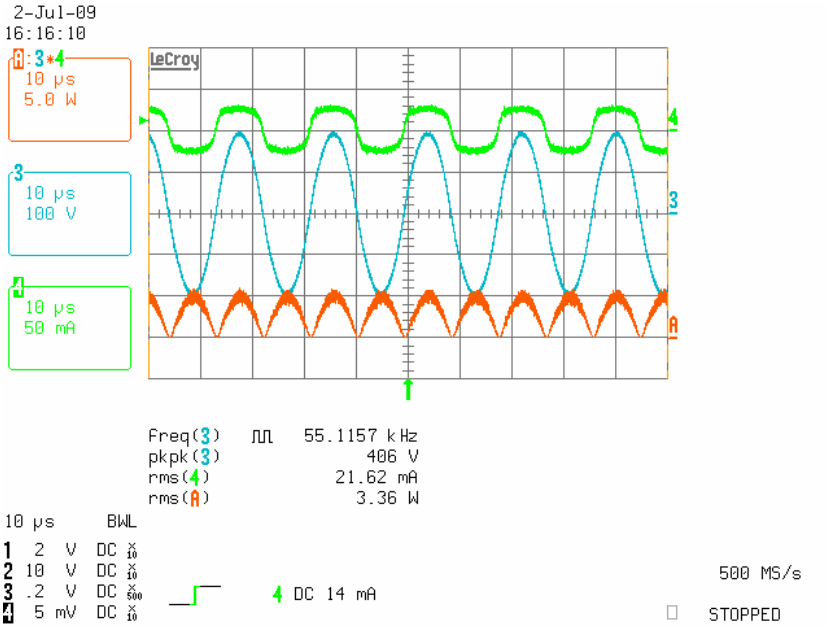


Figure 10: ***Minimum dimming level waveforms: CH3 is the voltage across the lamp, CH4 is the current through the lamp and CHA is the power of the lamp (voltage x current)***

Figure 11 shows the dimming characteristic of the ballast. The light output cannot go down below 10% of dimming level since the bus voltage becomes too low for the ballast to operate. The ballast also possesses a hysteresis behavior where the ballast is turned on at certain angle about midway between the turn-off point and the maximum point. This is necessary to ensure that the bus voltage is high enough to ignite the lamp and allows the ballast to operate sufficiently.

Dimming Characteristic

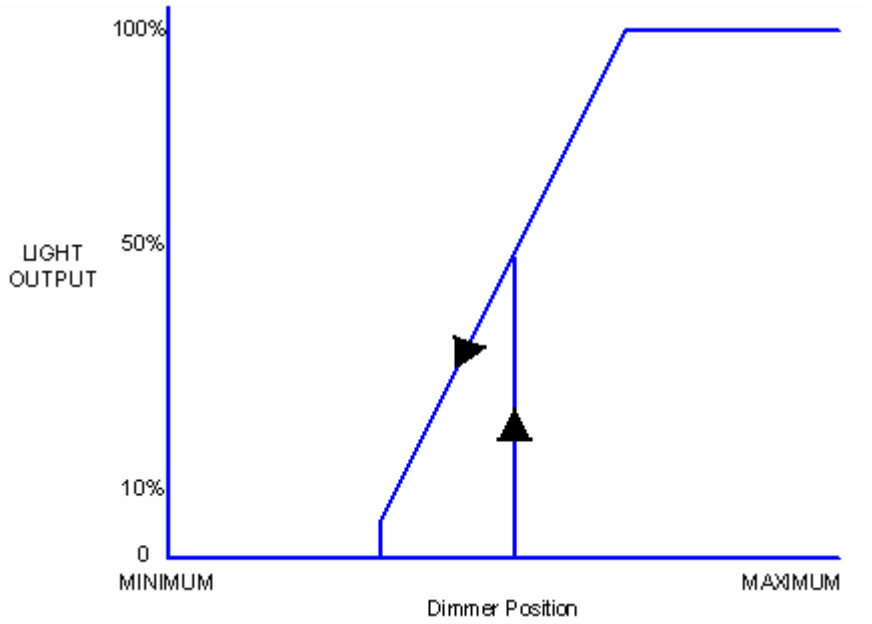


Figure 11: *Dimming Characteristics*

FAULT CONDITIONS

In case of fault conditions such as open filaments, or failure to strike, the IR2530D will go into Fault Mode. In this mode, the internal fault latch is set, HO and LO are low, and the IRS2530D consumes an ultra-low micro-power current. The IR2530D can be reset with a recycling of VCC below and back above the VCCUV thresholds.

Failure to Strike

At initial turn-on of the ballast, the frequency will ramp down from f_{MAX} toward the resonance frequency. When the lamp fails to strike, the VCO voltage continues to increase and the frequency continues to decrease until the VCO voltage exceeds VVCOFLT+ (4.0V, typical), and the IRS2530D enters Fault Mode and shuts down (Figure 12). It should be noted that in case of failure to strike, the system will operate in capacitive side of resonance, but only for short period of time.

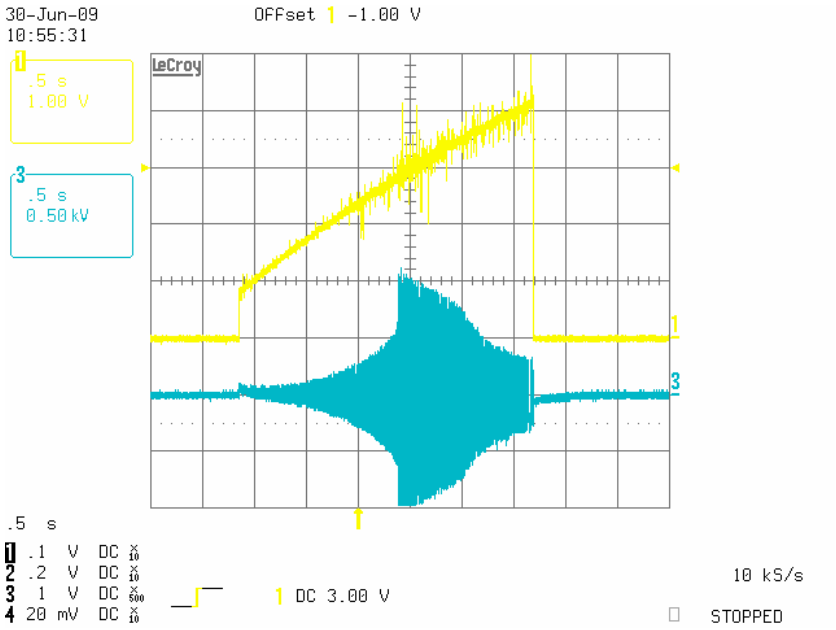


Figure 12: ***Failure to strike: CH1 is the VCO voltage and CH3 is the voltage across lamp***

AC Mains Interrupt / Brown-Out Conditions

This protection relies on the non-ZVS circuit of IRS2530D, enabled in the DIM Mode. During an AC mains interrupt or brown-out condition, the DC bus can decrease and cause the system to operate too close to, or, on the capacitive side of resonance. The result is non-ZVS switching that causes high peak currents to flow in the half-bridge MOSFETs that can damage or destroy them.

To protect against this, the IRS2530D will detect non-ZVS by measuring the VS voltage at each rising edge of LO. If the voltage is greater than VZVSTH (4.5V, typical), the IC will reduce the voltage at VCO pin, and thus increase the frequency until ZVS is reached again.

In case the DC bus decreases too far and the lamp extinguishes, the VCC voltage will go below VCCUV- and the ignition/preheat ramp will be reset to re-ignite the lamp reliably (Figure 13).

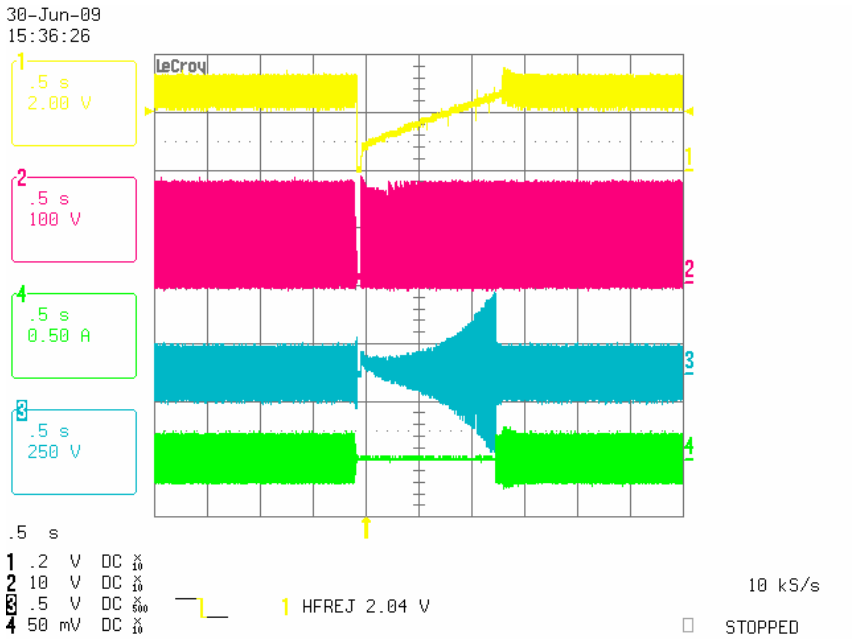


Figure 13: ***DC Bus decreases too far: CH1 is the VCO voltage, CH2 is the VS voltage, CH3 is the voltage across the lamp, CH4 is the lamp current***

Open Filament

The open filament protection relies on the non-ZVS and the Crest Factor Over-current protection, enabled in the DIM mode. When the open filament occurs, the output stage will transition to a series-LC configuration, and hard-switching will occur at the half-bridge because the system operates on the capacitive side of resonance. The non-ZVS circuit of the IRS2530D will detect this condition, increasing the frequency each cycle toward resonant frequency until the inductor saturates. The IRS2530D uses the VS-sensing circuitry and the RDSon of the low-side half-bridge MOSFET to measure the MOSFET current for detecting an over-current fault. Should the peak current exceed the average current by a factor of 5.5 (CF>5.5) during the on-time of LO, the IRS2530D will enter Fault Mode, where the half-bridge is off. Performing crest factor measurement provides a relative current measurement that cancels temperature and/or tolerance variations of the RDSon of the low-side half-bridge MOSFET.

Figure 14 shows the LO pin voltage, the VS voltage, voltage at lamp terminal and inductor current when the inductor saturates and the ballast shuts down.

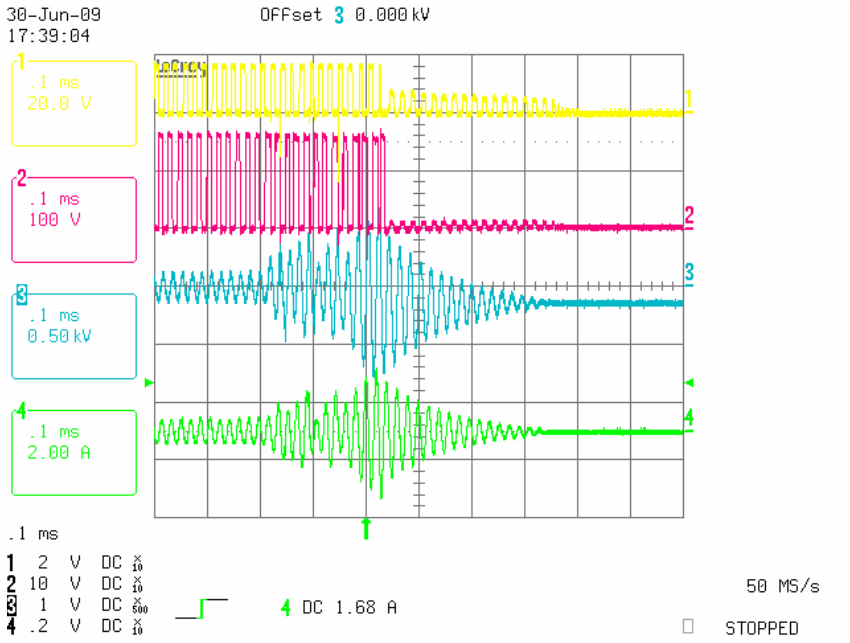


Figure 14: ***Open Filament: CH1 is the LO voltage, CH2 is the VS voltage, CH3 is the voltage at lamp terminal and CH4 is the current through the inductor***

BALLAST DESIGN

Output Inductor Design

The output inductor LRES should be designed to allow a high peak ignition current without saturating. This is important as the IRS2530D shutdown will be triggered if the inductor saturates. The ignition current depends on the type of lamp being used and must be kept to a minimum by ensuring the preheat is sufficient. To minimize losses in the inductor multi-stranded wire should be used in combination with Ferrite cores of adequate quality. The best approach to design is to wind as many turns as possible of multi-stranded wire and have the largest gap possible to achieve the correct inductance. This will produce the highest available peak current before saturating the inductor. It is important to be aware that when the cores are hot, the saturation point and hence the peak current for the inductor will be lower therefore a poorly designed inductor may result in the ballast shutting down during an attempted hot re-strike.

Lamp Preheating

The lamp must be sufficiently preheated before ignition. The correct preheat current can be determined from published data or from International Rectifiers *Ballast Designer* software.

The preheat time can be set by adjusting the value of CPH. As a general rule the lamp filament should glow red before ignition. If preheat is insufficient the ballast is likely to shutdown during ignition because the output inductor will be unable to operate at the high current required. The number of turns in the auxiliary cathode windings of the output inductor LRES should be chosen to provide sufficient preheat.

The lamp filament (Cathode) resistance over the range of dimming levels should be between 3 and 5.5 times the resistance when cold. A simple method for determining the hot resistance is to first connect one cathode to a DC power supply via an ammeter and slowly increase the voltage from zero, noting the current at 1V intervals. This should be done until the cathode can be seen to be glowing red. When this occurs the voltage should not be increased further in order to prevent possible cathode damage. The resistance can then be calculated for each voltage and hence the acceptable voltage range can be found to comply with the 3 to 5.5 times cold resistance, which can be easily measured with a digital multi-meter (DMM).

Then when the ballast is being run a true RMS digital voltmeter can be connected across one cathode and the voltage can be observed at maximum and minimum brightness. The cathode voltage increases as the ballast is dimmed. The values of CH1 and CH2 will control how much it increases by;

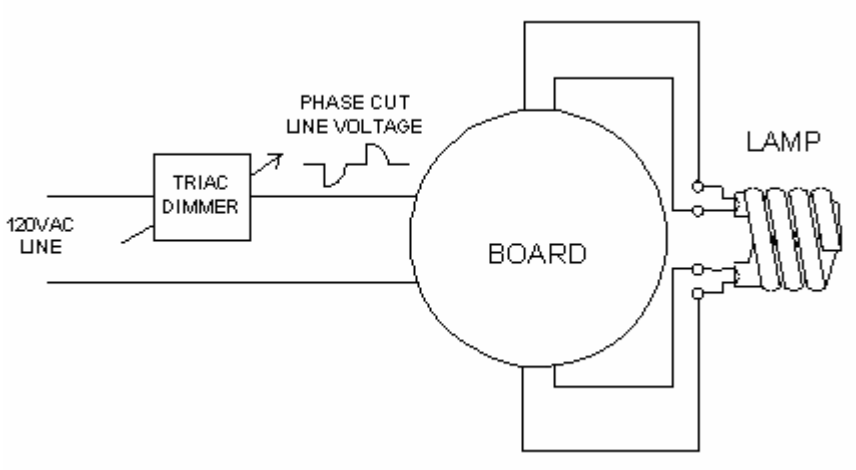
reducing the capacitance will reduce the amount by which the voltage rises. The values should be chosen to prevent the voltage exceeding the upper limit at minimum output.

It is important to consider that using additional windings on the inductor to provide cathode heating means that power is now being transferred through the core and consequently the core losses will increase and hence the core operating temperature. The core will reach its highest operating temperature when the ballast is running at minimum brightness.

The following component values have been selected for a 15W spiral CFL. The circuit will need to be optimized for the particular lamp used to obtain best performance.

Demo Board Connections

The demo board has two test points for connection to the 120VAC mains supply. The board *must not* be connected to a supply greater than 120V. There are four output connections to be connected to a compact lamp. The two upper connections go to one lamp cathode and the two lower connections go to the other lamp cathode.



BILL OF MATERIALS

Item #	Qty	Manufacturer	Part Number	Description	Reference
1	4	Diodes, Inc.	1N4007DICT-ND	Diode, 1000V, 1A	D1, D2, D3, D4
2	1	Renco	RL-5480-3-2700	Filter inductor	L1
3	1	Panasonic	ERZ-V05D221	Varistor / Surge Absorber	VR
4	3	Panasonic-ECG	ECQ-E2333KB	Capacitor, 33nF, 250V	C1, C2, C3
5	1	EPCOS	B32671L0682J	Capacitor, 6.8nF, 1kV, LS=10mm	C4
6	1	EPCOS	B32620A472J	Capacitor, 4.7nF, 1kV, LS=7.5mm	C5
7	1	Panasonic	ECJ-2FB1E105K	Capacitor 1.0uF, 25V, 0805	C6
8	1	Wima	MKS2 Series	Capacitor, 47nF, 400V	CDC
9	1	Panasonic	EEU-EB2D220	Capacitor, 22µF, 200VDC, 105C	CBUS
10	2	Panasonic	ECJ-2FB1H104K	Capacitor, 0.1µF, 50V, 0805	CBS, CFB
11	2	Panasonic	ECJ-3VB1E104K	Capacitor, 0.10µF, 25V, 1206	CH1, CH2
12	1	Panasonic	ECJ-2VB1H222K	Capacitor, 2.2nF, 50V, 0805	CVCO
13	1	AVX	08053D684KAT2A	Capacitor, 0.68µF, 25V, 0805	CPH
14	1	Panasonic	ECJ-3YB1C105K	Capacitor, 1µF, 16V, 1206	CVCC
15	1	Panasonic	ECJ-2VB1H103K	Capacitor, 10nF, 50V, 0805	CDIM
16	1	Panasonic	ECK-A3A102KBP	Capacitor, 1nF, 1KV, Ceramic disk	CVS
17	1	Wima	MKP 472K1K6	Polypropylene Capacitor, 4.7nF/1.6KV, 10%, LS=10mm	CRES
18	1	IR	IRS2530D	Dimming Ballast Control IC	IC1
19	1	Vogt		Ballast Resonant Inductor 1.25mH	LRES
20	2	Digikey/Vishay	IRFU320	Transistor, MOSFET, 400V	MHS, MLS
21	1	Vishay	PPC.47BCT-ND	Resistor, 0.47R, 1/2W	R1
22	2	Panasonic	ERJ-6GEYJ153V	Resistor, 15K, 0805	R3, R6
23	2	Panasonic	ERJ-8GEYJ104V	Resistor, 100K, 1206	RVCC1, R2
24	3	Panasonic	ERJ-6GEYJ104V	Resistor, 100K, 0805	RVCC2, R4, R5
25	1	Panasonic	ERJ-6GEYJ224V	Resistor, 220K, 0805	RLMP1
26	1	Panasonic	ERJ-P08J102V	Resistor, 1K, 1206	RFB
27	1	Panasonic	ERJ-6GEYJ152V	Resistor, 1.5K, 0805	RVCO
28	3	Panasonic	ERJ-6GEYJ100V	Resistor, 10 Ohm, 0805	RHO, RLO, RLIM
29	1	Panasonic	PPC7.5W-1CT-ND	Resistor, 7.5 Ohm, 5%, 1 W, Axial	RCS
30	1	Panasonic	PPC1.0W-1CT-ND	Resistor, 1.0 Ohm, 5%, 1 W, Axial	RCF* (please see note below)
31	2	Diodes, Inc.	LL4148DICT-ND	Diode, 1N4148 SMT DL35	DCP2, D5
32	1	Diodes, Inc.	ZMM5248BDICT-ND	Zener Diode, 18V, 500mV, SMT	DCP1
33	1	Diodes, Inc.	ZMM5240BDICT-ND	Zener Diode, 10V, 500mV, SMT	D6
Total	**48**				

Table 3: ***Bill of Materials. Lamp type: 15W Spiral CFL***

* Some lamp type, when is cold and dimmed down, can trigger the Crest-Factor Over-Current Protection of the IRS2530D. If this is the case, please use the 1.0 Ohm resistor for RCF. Otherwise, put a jumper across RCF.

Resonant Inductor Specification

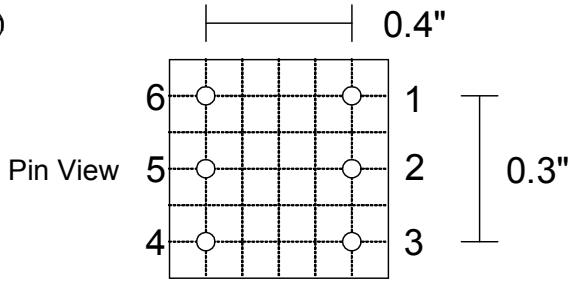
International
IOR Rectifier

INDUCTOR SPECIFICATION

CORE SIZE	E16/ 8 / 8	
GAP LENGTH	1.0	mm
CORE MATERIAL	Philips3C85, Siemens N27 or equivalent	
NOMINAL INDUCTANCE	1.25	mH
TEST TEMPERATURE	100	C

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
MAIN	1	4	130*	8 strands of 40 awg
CATHODE	2	3	5	32 awg insulated
CATHODE	5	6	5	32 awg insulated

PHYSICAL LAYOUT
(Vertical 6- Pin Bobbin)



TEST	TEST TEMPERATURE	100		C
	MAIN WINDING INDUCTANCE	MIN 1.2	mH	MAX 1.3

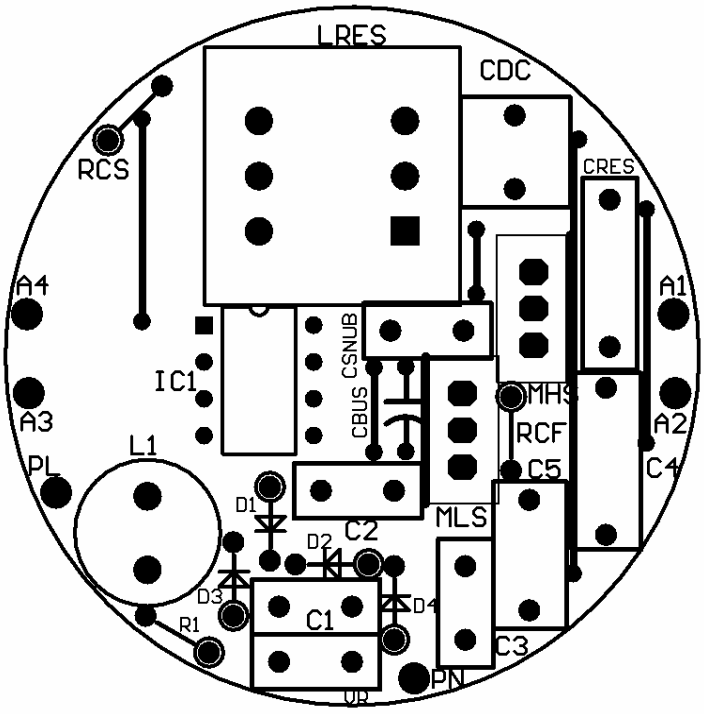
* Adjust turns for specified Inductance

mH

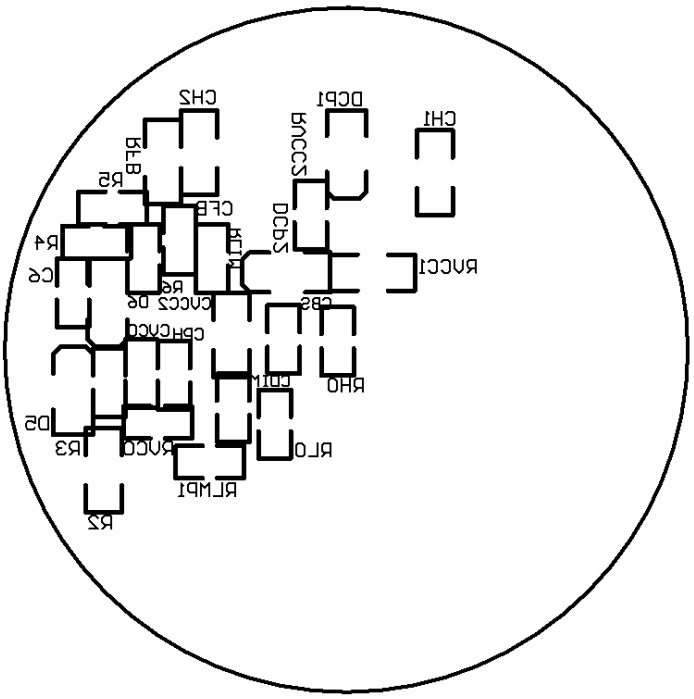
PCB INFORMATION AND LAYOUT

Board Information

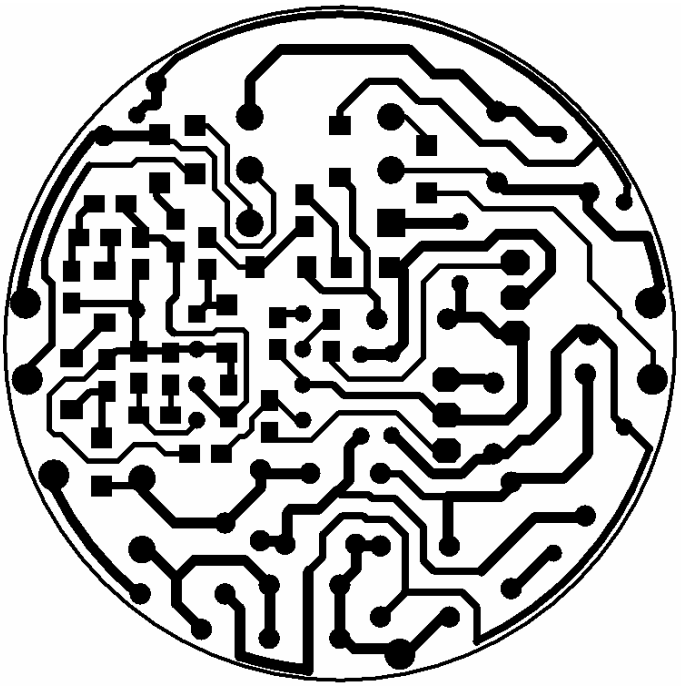
Diameter: 1.87inches (475mm)
Number of copper layer: 1 (bottom layer)
Through hole components: 21
Surface Mount components: 27



Top Assembly



Bottom Assembly



Bottom Copper

CONCLUSIONS

A CFL ballast without PFC is effectively capacitive and by itself, cannot work with a phase-cut (triac) dimmer. This application note suggests a ballast circuit that is dimmable with such dimmer. The design contains an EMI filter and a dimming ballast control circuit using the revolutionary 8-pin dimming ballast IC IRS2530D ***DIM8***™. Because of the simplicity of the dimming method of IRS2530D, this board uses few components counts to realize the minimum dimming level close to 10%. The ballast is also fully protected from fault conditions, such as non-strike, brown-out and open filament.