SmartLEWIS™ TRX

TDA5340

High Sensitivity Multi-Channel Transceiver

User Manual

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Wireless Sense & Control

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 17.02.2012	
Chapter 1.1	Frequency extension of 434MHz Band
Figure 1	Figure changed
Figure 2	Figure changed
Chapter 6.9	Block Diagram changed + RF frequency calculation for TX
Chapter 6.12.1	ASK sloping calculation of register values changed
Chapter 6.12.2	GFSK calculation for NRZ inserted
Signal Detector Range Selection Register	Reset value changed
FSK Noise Detector Configuration Register	Reset value changed
TX RF Configuration Register	Reset value changed
Antenna Switch Configuration Register	Reset value changed
RF Control Register	Reset value changed
RX Control Register	Reset value changed

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1 Introduction

The IC is a low power ASK/FSK/GFSK Transceiver for the frequency bands 300-320, 415-495, 863-960 MHz. Bi-phase modulation schemes, like Manchester, bi-phase mark, bi-phase space and differential Manchester as well as NRZ are supported.

The chip offers a high level of integration and needs only a few external components, like a crystal, several blocking capacitors and the necessary matching elements. For very cost sensitive applications the integrated IF-filter and the internal RX/TX switch may be used but the transceiver enables also the flexibility to build a very robust system against interferer using external frontend and IF-filters.

The device is qualified according to automotive quality standards and operates between -40 and +110 °C at supply voltage ranges of 3.0-3.6 Volts or 4.5-5.5 Volts.

A fully integrated Sigma-Delta Fractional-N PLL Synthesizer, with high frequency resolution and a crystal oscillator as reference, generates the necessary frequencies for the power amplifier or down conversion mixers. The on-chip temperature sensor may be utilized for temperature drift compensation of the crystal oscillator.

The receiver portion is realized as a double down conversion super-heterodyne / low-IF architecture each with image rejection supplemented by digital signal processing in the baseband. This architecture enables outstanding sensitivity performance in combination with very good blocking performance values.

The transmitter section comprises a class C/E power amplifier with a high efficiency and an output power level of 14 dBm. A tuning feature for the output power is possible via several switchable parallel output stages, of course matching to lower power levels is always possible. For higher power applications an external power amplifier can be used and the internal PA serves as a power driver. For ASK modulation a programmable data shaping is provided. With the fractional-N PLL synthesizer and a selectable Gaussian data shaping filter a very accurate and precise FSK modulation is achieved. The transmit data can be either stored in a separate FIFO data buffer or directly provided via the bus interface.

The receiver portion is able to scan autonomously for incoming data by using the self polling feature while the host micro controller can stay in power down mode, which reduces the system current consumption significantly.

The digital baseband processing unit together with the high performance downconverter is the key element for the exceptional sensitivity performance of the device which takes it close to the theoretical top-performance limits. It comprises signal and noise detectors, matched data filter, clock and data recovery, data slicer and a format decoder. It demodulates the received ASK or FSK data stream and recovers the data clock out of the received data with very fast synchronization times which can then be either accessed via separate pins or used for further processing like frame synchronization and intermediate storage in the on-chip FIFO.

The RSSI output signal is converted to the digital domain with an on-chip ADC. All these signals are accessible via the 4-wire SPI interface bus.

Up to 4 pre-configured telegram formats with different data rates and filter bandwidths can be stored into the device offering independent pre-processing of the received and transmitted data. The downconverter can be also configured to single-conversion mode at moderately reduced selectivity and image rejection performance but at the advantage of saving the external IF filter.

1.1 Key Features

Transceiver

- Multiband / Multichannel (300-320 MHz, 415-495 MHz, 863-960 MHz)
- High receiver sensitivity better than -116 dBm
- Power amplifier with up to 14 dBm output power
- Very Low Current consumption:
  - Receive Mode: 12 mA (typ)
  - Transmit Mode at 10 dBm and 434 MHz: 12 mA (typ)
  - Sleep Mode (XTAL ON): 40 uA (typ)
  - Deep Sleep Mode (XTAL OFF): 7 µA (typ)
  - Power down Mode: 0.9 uA (typ)
- ASK and FSK capability with programmable Gaussian data shaping
- 20 dB programmable output power range
- On-chip IF filter with selectable bandwidth (optional an external CER-filter is possible)
- Sigma-delta fractional-N PLL synthesizer with high resolution
- Automatic Frequency Control function (AFC) for offset carrier frequency
- Antenna Diversity by using the RSSI as decision base

Digital Baseband

- Multi protocol handling: Up to 4 parallel parameter sets for autonomous scanning and receiving from different sources
- Integrated data and clock recovery
- Autonomous receive functionality: Frame synchronisation, format decoding, message ID screening
- 288 Bit RX/TX-FIFO for receive and transmit data
- Wake-up generator and polling timer unit
- Ultra-fast wake-up on RSSI
- Supports all bi-phase format schemes and NRZ

General

- Operating temperature range -40 to +110°C
- Supply voltage range 3.0 to 3.6 V or 4.5 to 5.5 V
- Brownout detector
- Integrated 4-wire SPI bus interface
- 32-bit wide Unique ID on chip
- On-chip temperature sensor
- ESD protection +/- 2 kV on all pins (HBM)
- PG-TSSOP-28 package

1.2 Target Applications

- Remote keyless entry (RKE)
- Remote start applications
- Passive Keyless Entry (PKE)
- Security Alarm Systems
- Automatic Meter Reading (AMR) and Infrastructure (AMI)
- Home Automation
- Remote Control
- Sensor Networks
- Short range radio data transmission

1.3 Application Example

The Application examples within this section where optimized for performance and system costs. Of course there exists several steps in between which can be realized by the customer to fulfill the application specific needs.

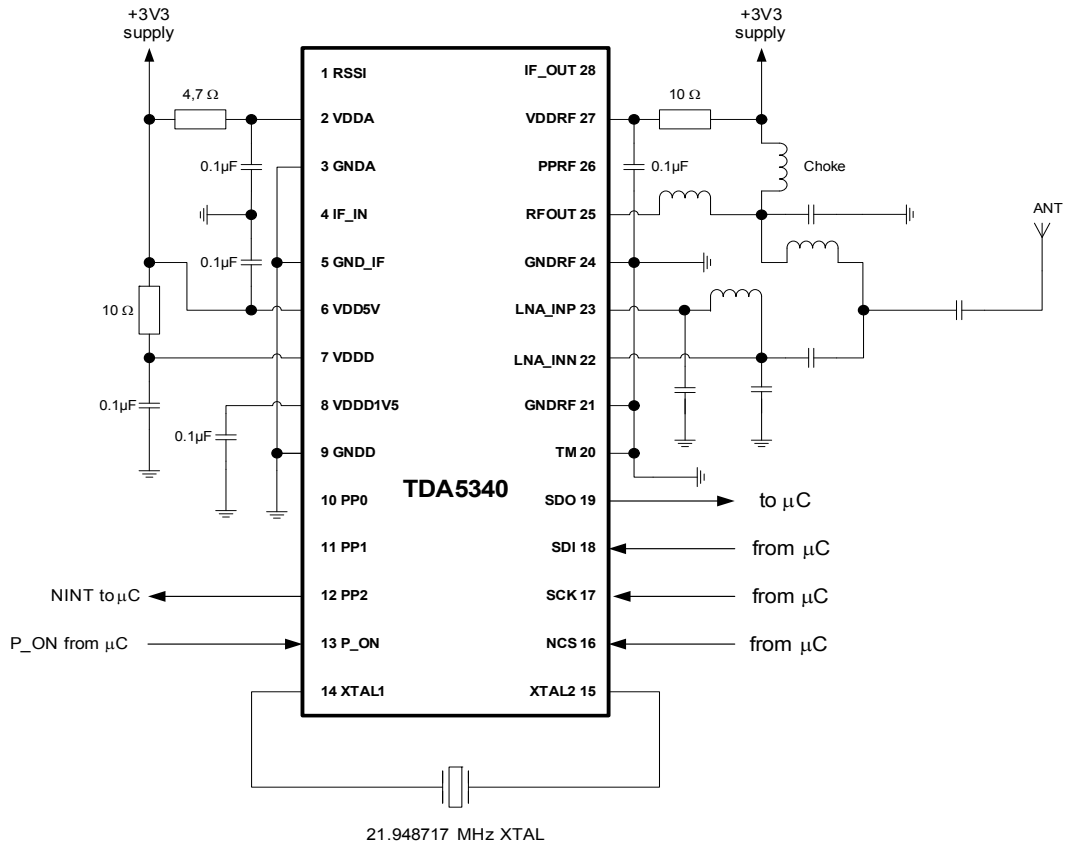


Figure 1 Application Example optimized for System Costs (3V3 Supply)

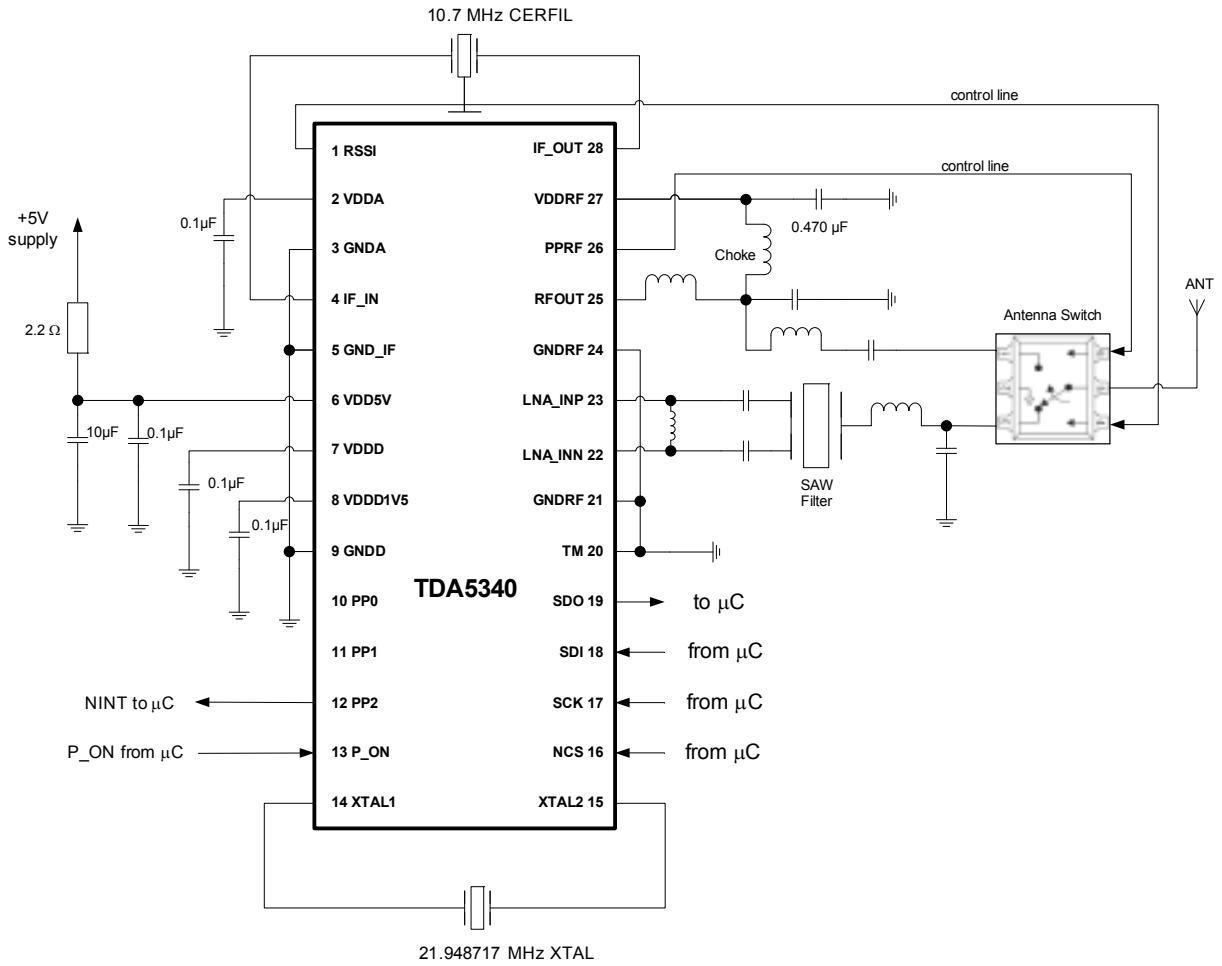


Figure 2 Application Example optimized for RF performance (5V Supply)

1.4 Pin Configuration

The pin configuration of the TDA5340, which is based on the PG-TSSOP-28 package, is shown in **Figure 3**.

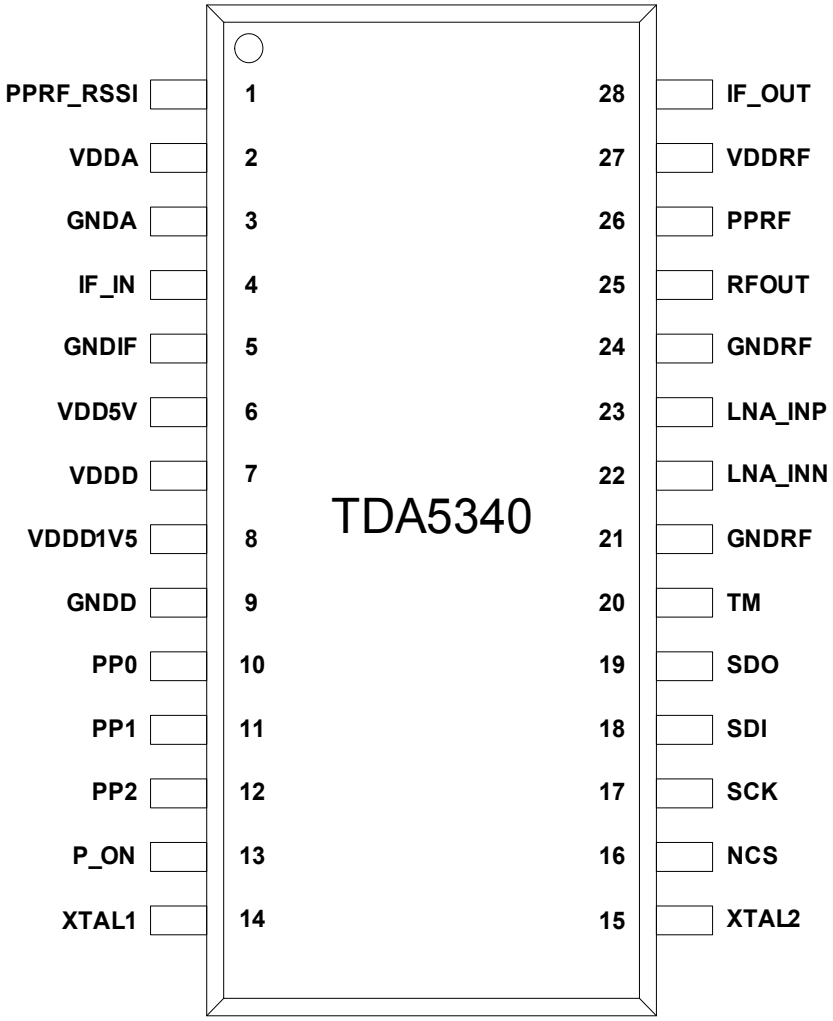


Figure 3 Pin-Out

1.5 Pin Definition

Table 1 Pin Definition and Function

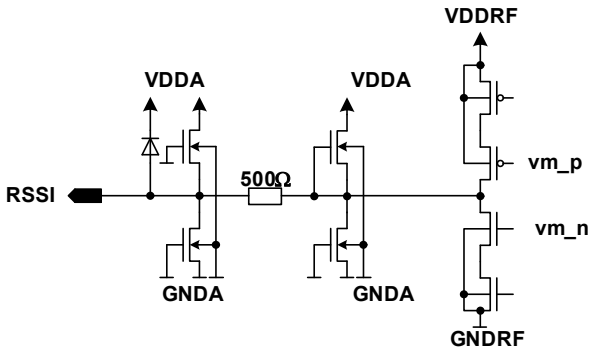
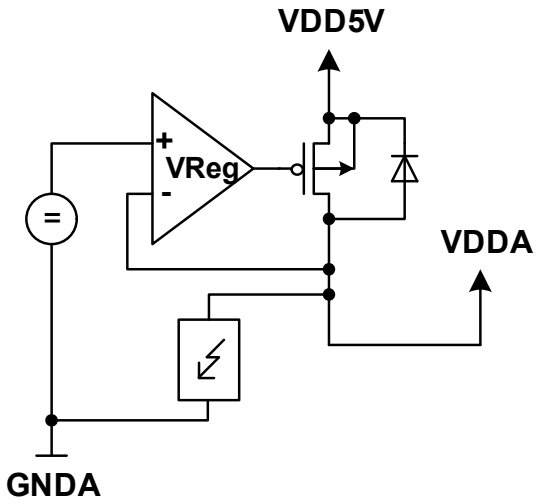
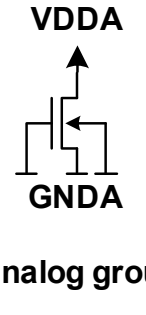
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
1	PPRF_RSSI		Analog output Digital output with weak driver capability, always in 3V domain RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: TRISTATE
2	VDDA		Analog input Analog supply
3	GNDA		Analog Ground

Table 1 Pin Definition and Function

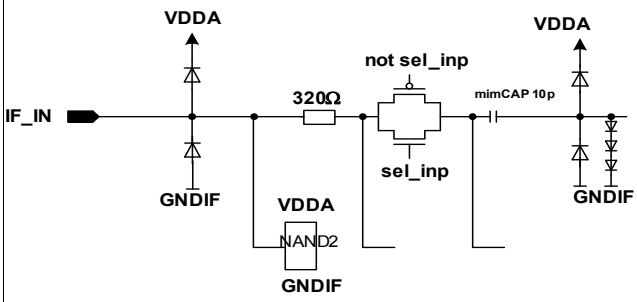
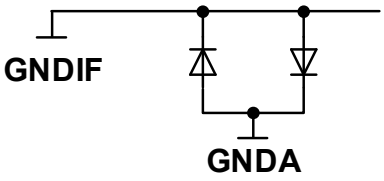
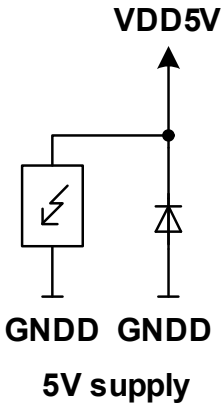
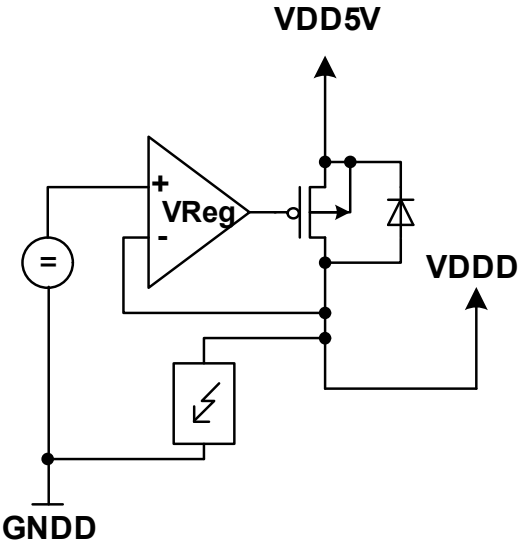
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
4	IF_IN		Analog input IF mixer input
5	GNDIF		Analog Ground
6	VDD5V		Analog input 5 Volt supply input
7	VDDD		Analog input digital supply input

Table 1 Pin Definition and Function

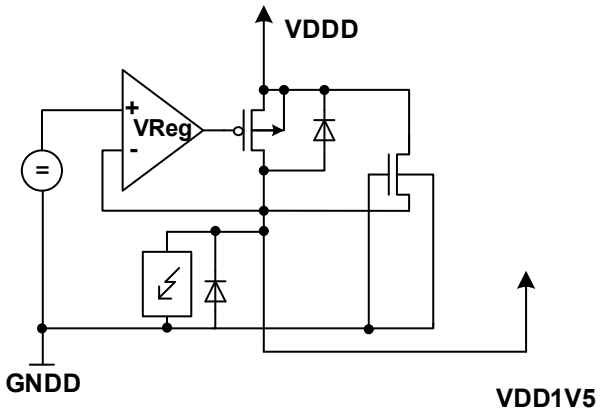
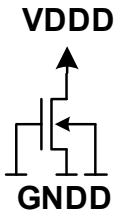
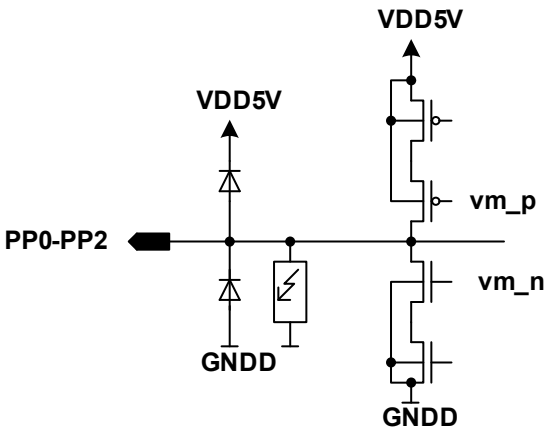
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
8	VDDD1V5		Analog output 1.5V regulator
9	GNDD		Digital ground
10	PP0		Digital output CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: CLK_OUT
11	PP1	same as PP0	Digital output CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: DATA

Table 1 Pin Definition and Function

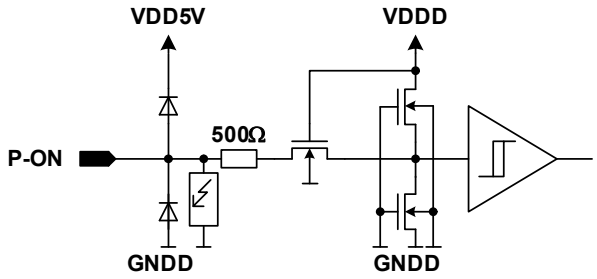
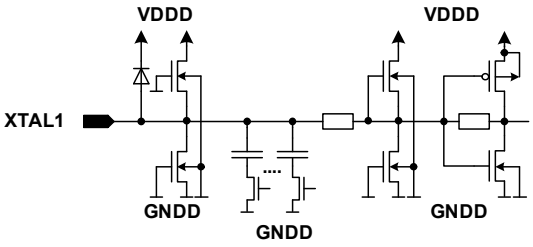
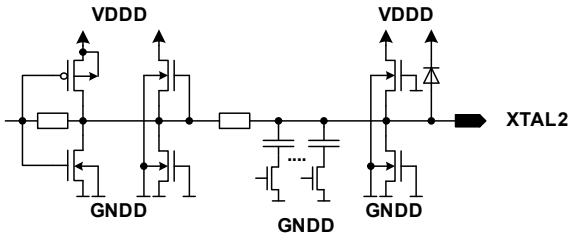
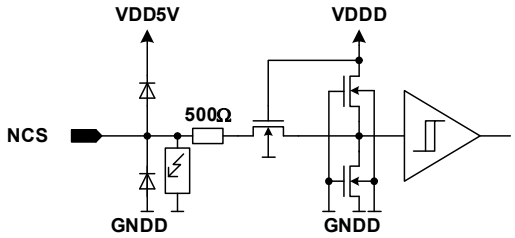
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
12	PP2	same as PP0	Digital output CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: NINT
13	P_ON		Digital input power-on reset
14	XTAL1		Analog input crystal oscillator input
15	XTAL2		Analog output crystal oscillator output
16	NCS		Digital input SPI Not Chip select

Table 1 Pin Definition and Function

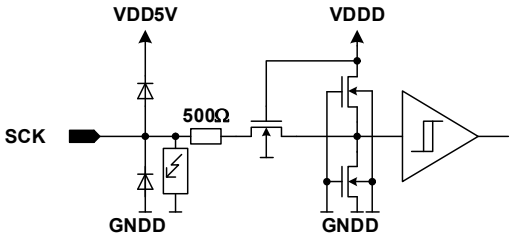
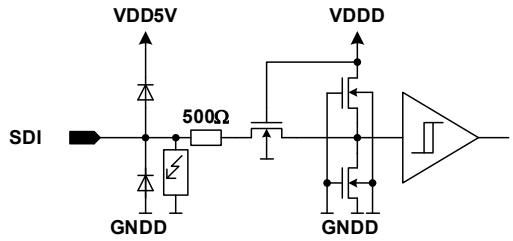
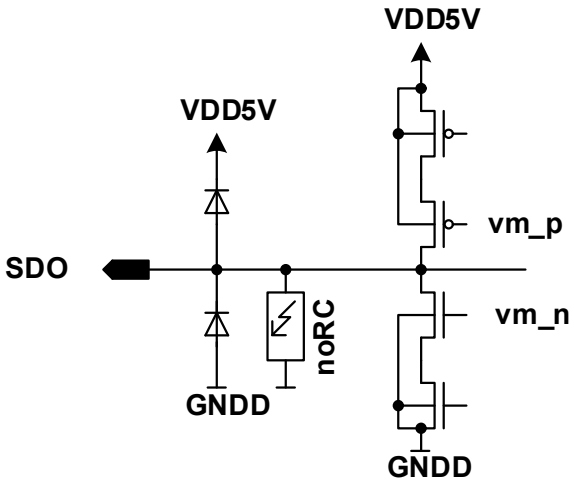
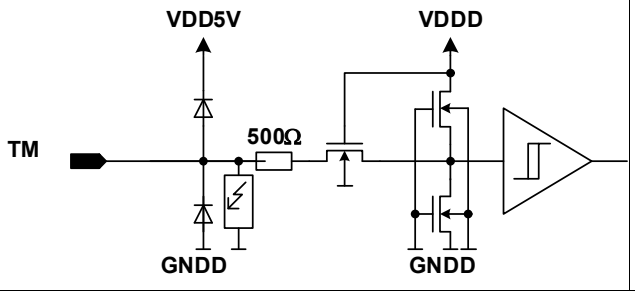
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
17	SCK		Digital input SPI clock
18	SDI		Digital input SPI data in
19	SDO		Digital output SPI data out
20	TM		Digital input connect to digital ground

Table 1 Pin Definition and Function

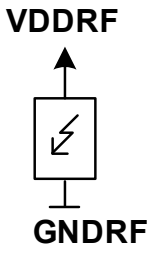
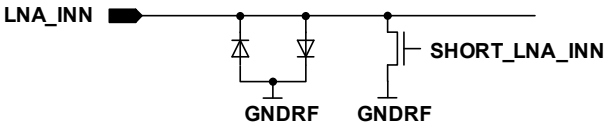
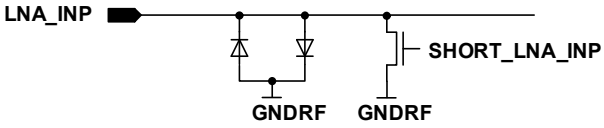
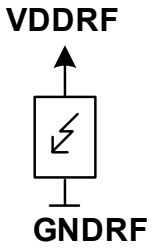
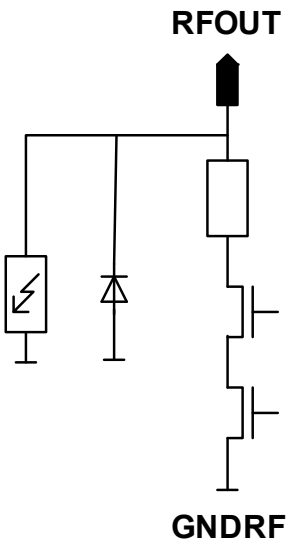
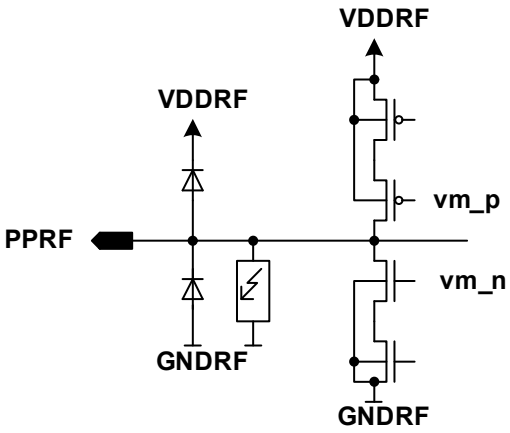
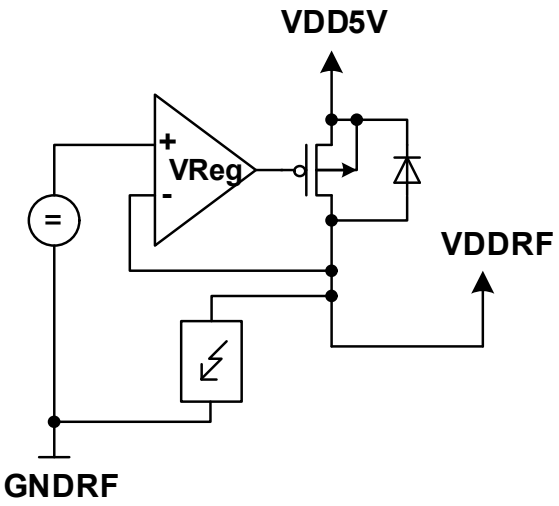
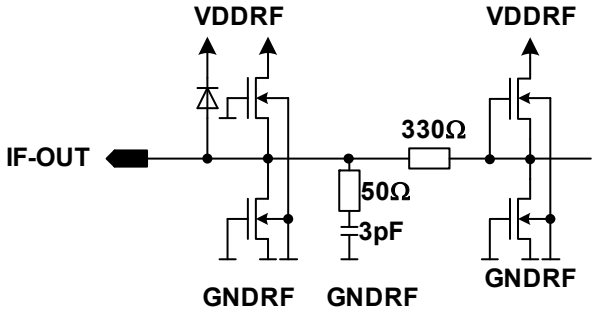
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
21	GNDRF		Analog ground
22	LNA_INN		Analog input - RF input
23	LNA_INP		Analog input +RF input
24	GNDRF		Analog ground
25	RFOUT		Analog output power amplifier output

Table 1 Pin Definition and Function

Pin Nr	Pad Name	Equivalent I/O Schematic	Function
26	PPRF		Digital output always in 3V domain RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: TRISTATE
27	VDDRF		Analog input RF supply
28	IF_OUT		Analog output Mixer output

2 Transceiver Architecture

The TDA5340 transceiver architecture is based on a super-heterodyne/low-IF, single or double down conversion receiver in combination with a highly efficient Class C/E type power amplifier.

A fully integrated Sigma-Delta Fractional-N PLL Synthesizer covers the frequency bands 300-320 MHz, 415-495 MHz, 863-960 MHz with a high frequency resolution, using only one VCO running at around 3.6 GHz. This makes the IC most suitable for Multi-Band/Multi-Channel applications. For Multi-Channel applications a very good channel separation is essential. To achieve the necessary high sensitivity and selectivity a double down conversion super-heterodyne architecture is used. The first IF frequency is located around 10.7 MHz and the second IF frequency around 274 kHz. For both IF frequencies an adjustment-free image frequency rejection feature is realized. In the second IF domain the filtering is done with an on-chip third order bandpass polyphase filter. A multi-stage bandpass limiter completes the RF/IF path of the receiver. For Single-Channel applications with relaxed requirements to selectivity, a single down conversion low-IF scheme can be selected.

A very high efficient Class C/E Power amplifier with output levels of +14 dBm combined with a Gaussian Filter for GFSK and amplitude ramping functions for shaped ASK is implemented. A high resolution power adjustment can be done to trim the output power for highest system power savings. The data can be either shifted out of an on-chip transmit FIFO or directly provided on an input pin.

An RSSI generator delivers a DC signal proportional to the applied input power and is also used as an ASK demodulator. Via an anti-aliasing filter this signal feeds an ADC with 10 bits resolution.The harmonic suppressed limiter output signal feeds a digital FSK demodulator. This block demodulates the FSK data and delivers an AFC signal which controls the divider factor of the PLL synthesizer. A digital receiver, which comprises RSSI peak detectors, a matched data filter, a clock and data recovery, a data slicer, a frame synchronization and a data FIFO, decodes the received ASK or FSK data stream. The recovered data and clock signals are accessible via 2 separate pins. The FIFO data buffer is accessible via the SPI bus interface.The crystal oscillator serves as the reference frequency for the PLL phase detector, the clock signal of the Sigma-Delta modulator and divided by two as the 2nd local oscillator signal. To accelerate the start up time of the crystal oscillator two modes are selectable: a Low Power Mode (with lower precision) and a High Precision Mode.

Features

- Power Amplifier with up to 14 dBm output power
- Sigma Delta PLL with a resolution down to 10.5 Hz
- Receiver with integrated configurable IF-Filter and outstanding sensitivity performance
- On-chip transmit/receive switch
- Two receiver inputs supporting antenna diversity and multiband operation
- 4 pre-programmable configuration sets with self polling and channel scan capabilities
- Autonomous scanning of up to 16 receive channels
- Power ramping and Gaussian filtering of transmit data

2.1 Functional Block Diagram

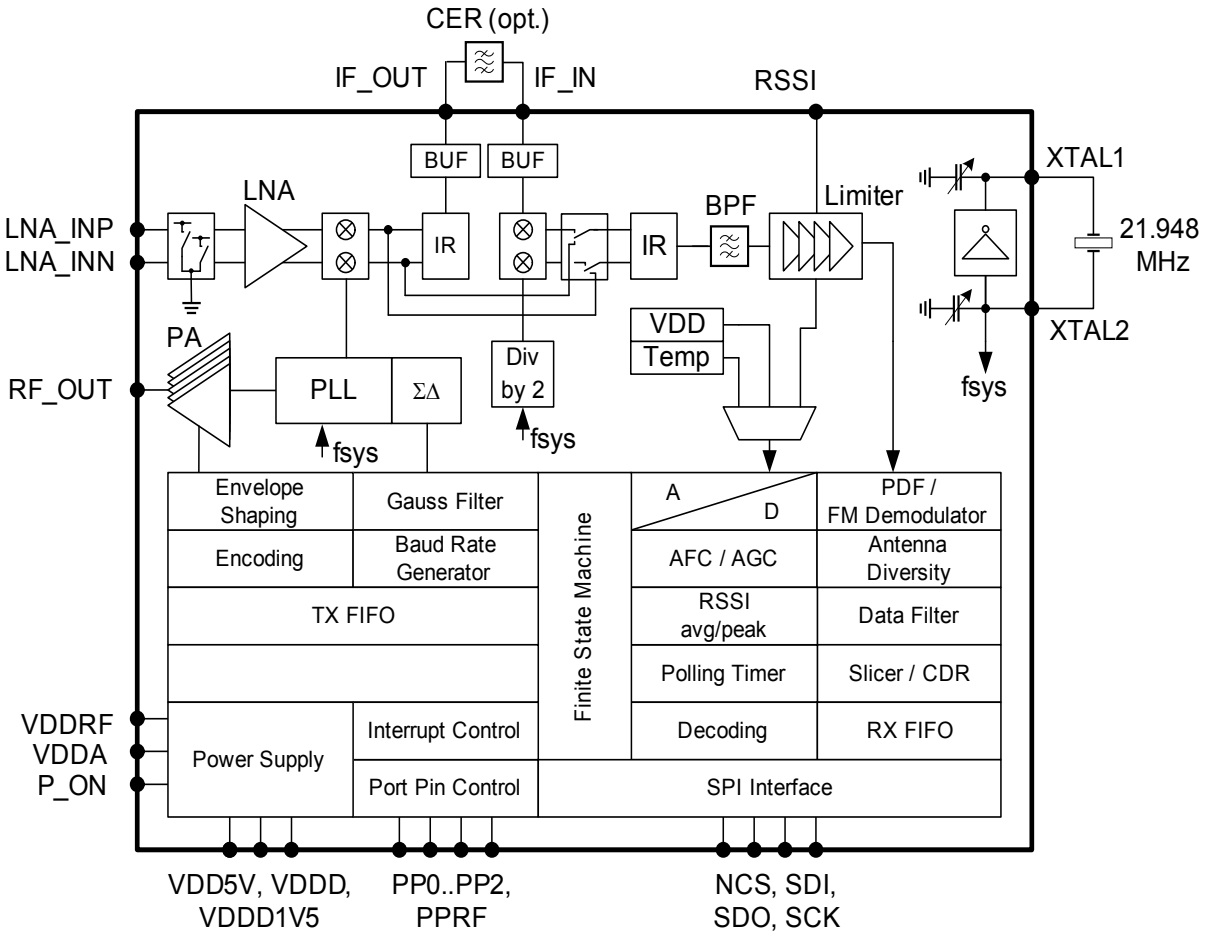


Figure 4 TDA5340 Block Diagram

2.2 Block Overview

The TDA5340 is separated into the following main blocks:

- RF / IF Receiver
- Power Amplifier
- Crystal Oscillator and Clock Divider
- Sigma-Delta Fractional-N PLL Synthesizer
- ASK / FSK Demodulator inc. AFC and AGC
- RSSI Peak Detector
- Digital Baseband Receiver
- Digital Baseband Transmitter
- Power Supply Circuitry
- System Interface
- System Management Unit

3 Operating Modes

The transceiver has three different power saving modes, two receive modes and a transmit mode. The different operating modes are used to adjust the transceiver functionality to the needs of the application. Depending on the

used communication protocols the appropriate power saving mode can be selected. In the table below all different modes are listed and corresponding to the modes the active blocks and current consumptions are shown.

Table 2 Operating Modes

Operating Mode	Transceiver Blocks								typ. Current Consumption
	Dig. Vreg	Ana. Vreg	XTAL	SFR	SPI	PLL	PA	RX	
Power Down	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0.9 µA
Deep Sleep	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	7 µA
Sleep	ON	OFF	ON[1)]	ON	ON	OFF	OFF	OFF	40 µA[2)]
Sleep ADC enabled	ON	ON	ON[1)]	ON	ON	OFF	OFF	OFF	1 mA
Transmit Ready	ON	ON	ON	ON	ON	ON	OFF	OFF	5.8 mA
Transmit Idle	ON	ON	ON	ON	ON	OFF	OFF	OFF	<3 mA
Transmit	ON	ON	ON	ON	ON	ON	ON	OFF	12.5 mA[3)]
Receive	ON	ON	ON	ON	ON	ON	OFF	ON	11.5 mA[4)]

1) selectable between XTAL in high or low precision mode
2) XTAL in low precision mode
3) 10dBm Output power at 434MHz
4) single down conversion Mode (no external CER Filter used)

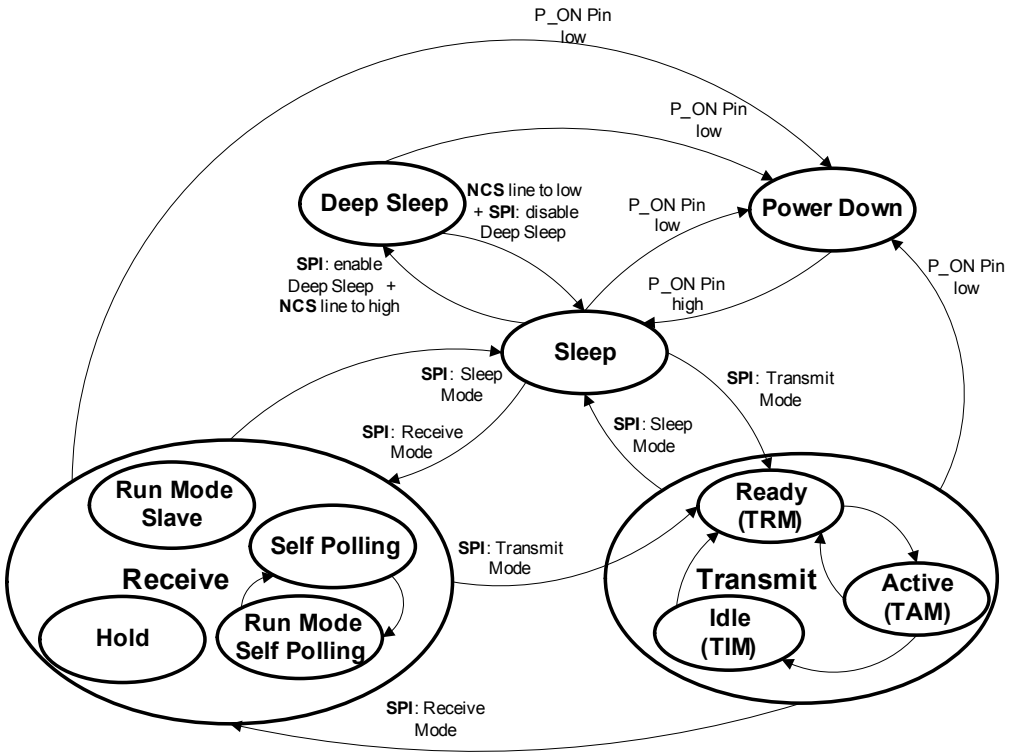


Figure 5 Main State Diagram

3.1 Power Saving Modes

Three different power saving modes are supported by the TDA5340. Depending on the application requirements like startup time and system current consumption the appropriate Power Saving Mode can be selected:

- Power Down Mode (PDM)
- Deep Sleep Mode (DSM)
- Sleep Mode (SM)

To enter the **Power Down Mode (PDM)**, the P_ON Pin must be pulled to low potential. As a result the Special Function Register (SFR) will be set to reset state and all voltage regulators will be switched off. This mode provides the lowest current consumption but also requires the longest time to recover to active modes.

Before entering the **Deep Sleep Mode (DSM)** this mode must be enabled by setting the SFR bit DSLEEPEN in the **Chip Mode Control Register**. To enter the DSM, pin NCS must be pulled to high potential. In the DSM the Crystal Oscillator is switched off but all SFR content is retained. Waking up from DSM is initiated by pulling the NCS pin to low potential again. After the end of the Crystal Oscillator start up time a system ready interrupt is generated (see **"Interrupt Generation Unit" on Page 50**) and the DSLEEPEN bit in the **Chip Mode Control Register** must be cleared to finally leave the DSM. The DSM can be only entered if the Sleep Mode is enabled.

In **Sleep Mode** the Crystal Oscillator is running and the digital domain is active but all analog parts are switched off. The Sleep Mode is fully controlled by the MSEL bit group in the **Chip Mode Control Register**. The SM offers the fastest switching time to active modes but with the expense of higher current consumption.

3.2 Transmit Modes

The Transmit (TX) Mode of the TDA5340 can be entered out of the Sleep and Receive Mode by changing the MSEL bit group in the **Chip Mode Control Register**. In this Mode the transmitter will be enabled and the data will be sent depending on the pre-configured settings.

Transmit (TX) Modes

- TX Ready Mode (TRM)
- TX Idle Mode (TIM)
- TX Active Mode (TAM)
  - TX FIFO Mode (TFM)
  - TX Transparent Mode (TTM)

The state diagram in **Figure 6** shows all possible start and stop combinations of the different transmit modes.

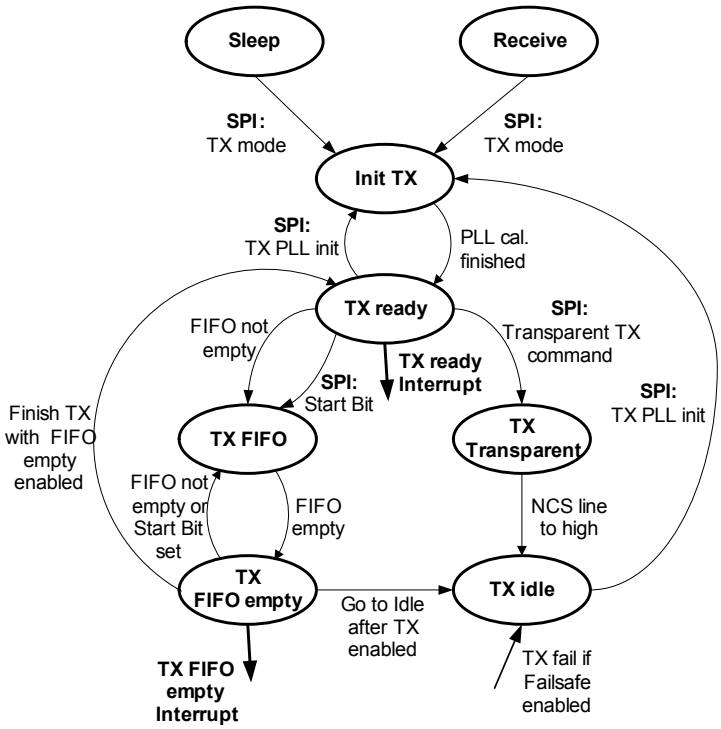


Figure 6 Transmit Modes

To enter the TX Mode the transceiver needs to start first the analog voltage regulators and the PLL. The host controller needs to set the MSEL operating mode bit group in the chip mode control register to enter the **TX Ready Mode.** The entrance of the TRM is indicated by an interrupt on the NINT line which shows the host controller that the transmitter has finished the startup procedure.

The **Transmit Active Mode (TAM)** enables a continuous data transmission where the baseband data are provided by the host controller or from the loaded on-chip transmit FIFO. The TAM must be entered out of the TRM. This can be done via several methods:

- The transparent TX command is entering the **TX Transparent Mode** while base band data must be provided on the SDI line. (see **“TX Transparent Mode” on Page 40**)
- The transceiver is configured in direct transmit mode. This means the Transmit Mode starts right after Transmit Ready Mode as long the TX FIFO is not empty. (see **“TX FIFO Modes” on Page 39**)
- The host controller is using the start bit mode of the transceiver. Within this mode the TFM is entered after enabling the TX start bit in the transmit mode control register (**TX Control Register**).

After transmission of the data frame the TDA5340 either waits for retransmission in the Transmit Ready Mode using the command listed above or enters the **Transmit Idle Mode (TIM)**. Out of the TIM a very fast switch to other modes (e.g. receive) is possible by changing the MSEL bit group in the **Chip Mode Control Register** . It is strongly recommended to leave the TIM state as fast as possible which has to be initiated by the host controller to avoid unnecessary high current consumption.

3.3 Receive Modes

The Receive Modes of the TDA5340 are designed to meet different requirements of the application.

The TDA5340 has three major receive operation modes, which are switched by MSEL bit group in the **Chip Mode Control Register** and the SFR bit HOLD in the **RX Control Register**.

Receive Modes

- Run Mode Slave Receive (RMS)

- Self Polling Mode Receive (SPM)
- Run Mode Self Polling (RMSP)
- Hold Mode (HM)

In RMS the receiver is always active which minimizes the preamble length of the transmit packet. The SPM can be used to perform automatic channel switching and preamble detection. Furthermore the average receive current consumption can be reduced significantly.

The following state diagram in **Figure 7** shows the possible transitions within the Receive Mode.

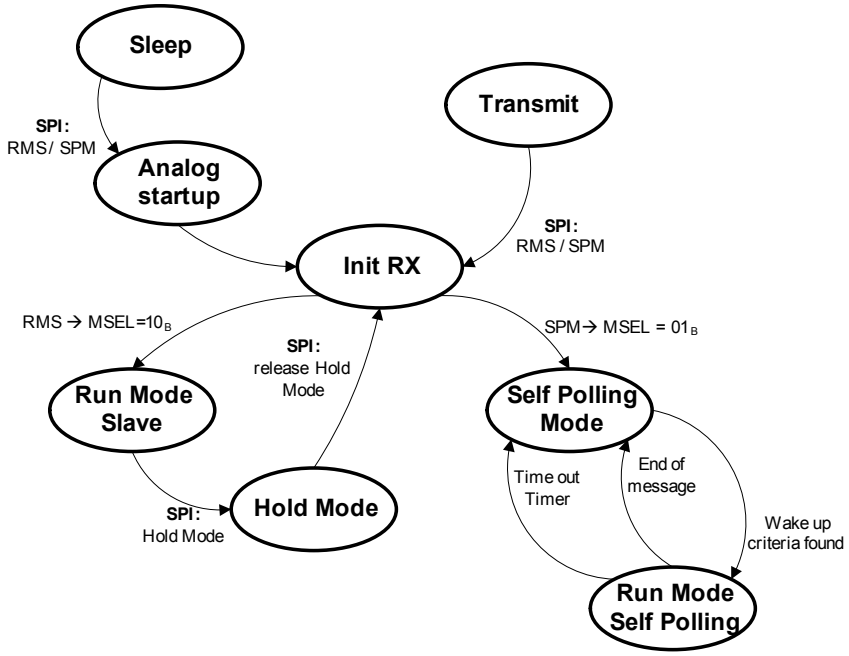


Figure 7 RX Main States

3.3.1 Run Mode Slave Receive (RMS)

In **Run Mode Slave (RMS)** the transceiver is able to continuously receive data which is consequently provided to the host controller. Run Mode Slave is entered by setting the MSEL bit group in the **Chip Mode Control Register**.

The successful detection of a payload, message ID and/or a whole message (End of message) can be signaled to the host micro controller via interrupts. For further details see **“Interrupt Generation Unit” on Page 50**

The configuration may be changed only in Sleep or in Hold Mode before returning to the previously selected operation mode. This is necessary to restart the state machine with defined settings at a defined state. Otherwise the state machine may show an undefined behaviour. Reconfiguration in Hold Mode is faster, because there is no Start-Up sequence.

3.3.2 Hold Mode

The **Hold Mode** is used in RMS to reconfigure the SFR of the device without changing back to Sleep Mode to avoid the time consuming startup procedure. To reconfigure the chip the SFR control bit HOLD in the **RX Control Register** must be set. After reconfiguration in this state the SFR control bit HOLD must be cleared again. After leaving the Hold Mode, the INIT state is entered and the receiver can work with the new settings. Be aware that the time between changing the configuration and re initialization of the chip has to be at least 40us.

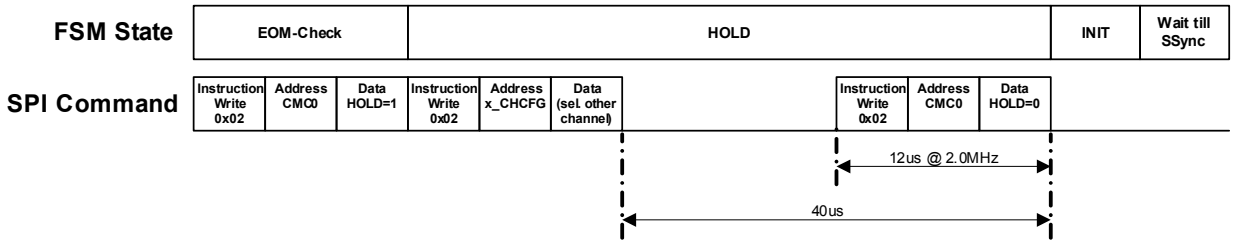


Figure 8 HOLD State Behavior (INITPLLHOLD disabled)

In case of large frequency steps, an additional VAC routine (VCO Automatic Calibration) has to be activated when recovering from Hold Mode (INITPLLHOLD bit in **RX Control Register**). The maximum allowed frequency step in Hold Mode without activation of VAC routine depends on the selected frequency band. The limits are +/- 1 MHz for the 315 MHz band, +/- 1.5 MHz for the 434 MHz band and +/- 3 MHz for the 868/915 MHz band.

When this additional VAC routine is enabled, the TDA5340 starts initialization of the Digital Receiver block after release from Hold Mode and an additional Channel Hop time.

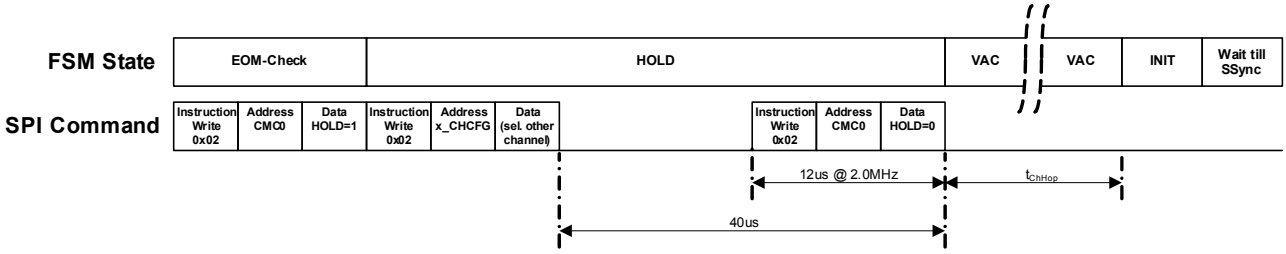


Figure 9 HOLD State Behavior (INITPLLHOLD enabled)

Hold Mode is only available in Run Mode Slave. Configuration changes in Self Polling Mode have to be done by switching to SLEEP Mode and returning to Self Polling Mode after reconfiguration.

3.3.3 Self Polling Mode Receive (SPM)

In **Self Polling Mode (SPM)** the TDA5340 is autonomously toggling between Sleep Mode and receive mode. At that time there is no processing load on the host micro controller. When a wake-up criterion has been found, an interrupt can be generated and the TDA5340 mode will be changed to **Run Mode Self Polling** (RMSP). In RMSP the receiver is searching for the payload data. The mode change back to SPM can be triggered by a successful reception of the payload or by several programmable Time Out Timer (TOTIM) events. Detailed descriptions of payload detection can be found in section **“Frame Synchronization” on Page 95** and for the TOTIM in section **“Time Out Timer (TOTIM)” on Page 62**.

The Polling Timer Unit controls the timing for scanning (On time) and sleeping (Off time, SPM_OFF). Up to four independent configuration sets (A, B, C and D) can automatically be processed, thus enabling scanning from different transmit sources. Additionally, up to 4 different frequency channels within each configuration may be scanned to support Multi-Channel applications. For configuration of On and Off timings see also **“Polling Timer” on Page 60**. So a autonomous scanning of up to 16 different frequency channels is supported.

The successful detection of a wake up criteria, payload, message ID and/or a whole message (End of message) can be signaled to the host micro controller via interrupts. For further details see **“Interrupt Generation Unit” on Page 50**

Automatic Modulation Switching

In Self Polling Mode, the chip is able to automatically change the type of modulation after a wake-up criterion was fulfilled in a received data stream. The type of modulation used in the different operational modes is selected by the SFR control bit MT.

Multi-Channel in Self Polling Mode

As previously mentioned, in Self Polling Mode the TDA5340 allows RF scans on up to four RF channels per configuration, this can be defined in the **Channel Configuration Register**. Channel frequencies are defined in registers **PLL MMD Integer Value Register Channel 1**, **PLL Fractional Division Ratio Register 0 Channel 1**, **PLL Fractional Division Ratio Register 1 Channel 1** and **PLL Fractional Division Ratio Register 2 Channel 1**, where A can be replaced by B, C or D and C1 can be replaced by C2, C3 or C4 to access the different channels and configurations.

Parallel Wake Up Search

While the TDA5340 is in Run Mode Self Polling, further Wake-ups would normally not be detected by the receiver. If the functionality of a parallel Wake-up search during the search for a TSI is desired, this can be activated by the PWUEN bit in **Wake-Up Control Register**. In this case the Wake-up search is not active during a recognized payload and is only active after the first received payload frame. This feature can only be used, when modulation type is the same for SPM and RMSP.

So after a reception of the EOM from the current payload, the parallel WU search can take place in this mode. The WU search will be active after Symbol Sync has been detected.

Self Polling Modes

Four polling modes are available to fit the polling behavior to the expected wake-up patterns and to optimize power consumption in Self Polling Mode.

The following 4 Polling Modes are available and can be configured via 2 bits in the configuration **Self Polling Mode Control Register**:

- Constant On-Off (COO)
- Fast Fall Back to SLEEP (FFB)
  - Ultra Fast Fall Back to SLEEP (UFFB)
- Mixed Mode (MM)
- Permanent Wake-Up Search (PWUS)

A detected wake-up data sequence or an actual value for RSSI or Signal Recognition (a combination of Signal Detector and Noise Detector, see **“Data Filter and Signal Detection” on Page 82**) exceeding a certain adjustable threshold forces the TDA5340 into Run Mode Self Polling.

In all modes the timing resolution is defined by the Reference Timer, which scales the incoming frequency (fsys/64) corresponding to the value, which is defined in the **Self Polling Mode Reference Timer Register**. Changing values of SPMRT helps to fit the final On-Off timing to the calculated ideal timing.

3.3.3.1 Constant On-Off Mode (COO)

In this mode there is a constant On and a constant Off time. Therefore also the resulting master period time is constant.

When **Single-Configuration** is selected then only Configuration A is used. The number of RF channels is defined in the **Channel Configuration Register** (**Single-Channel** or **Multi-Channel** Mode).

Multi-Configuration Mode allows reception of up to 4 different transmit sources or up to 16 RF channels. The corresponding RF channels can be defined in the **Channel Configuration Register**, B_CHCFG, C_CHCFG and D_CHCFG registers. In the case of Multi-Channel or combination of Multi-Channel and Multi-Configuration Mode,

the configured On time is used for each RF channel in a configuration. The diagram below shows possible scenarios.

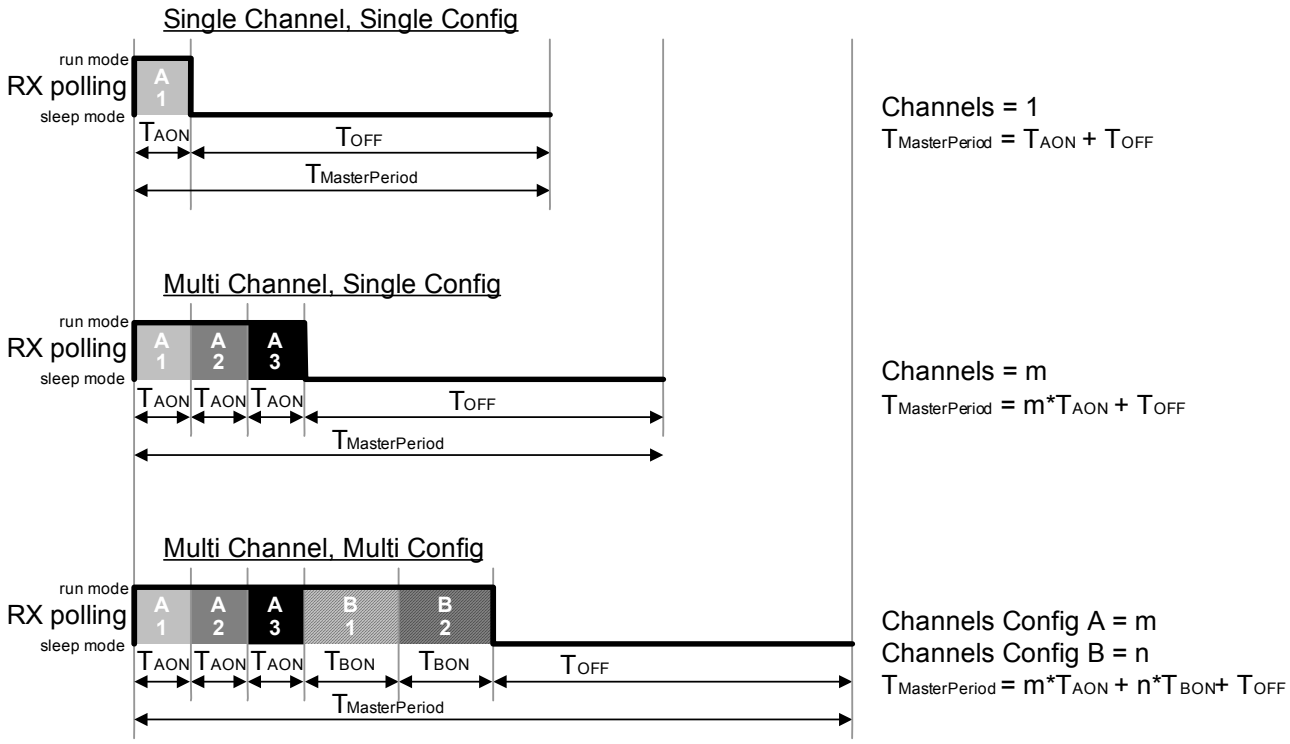


Figure 10 Constant On-Off Time

3.3.3.2 Fast Fall Back to SLEEP (FFB)

This mode is used to switch off the receiver, if there is no RF signal, as quickly as possible to reduce power consumption.

During the search for wake-up data, there is a check for the right data rate, to which the system can be synchronized. If there is no synchronization to the programmed data rate within the so-called Sync Search Time Out (SYSRCTO), the wake-up search for this channel is stopped. If synchronization to the data rate is possible (and not lost again), the TDA5340 waits if the wake-up criterion is fulfilled. If the wake-up criterion is not fulfilled (in worst case, if the last bit of an expected wake-up data pattern is wrong), the wake-up procedure for this channel is stopped, and the TDA5340 tries to synchronize on the next channel, or falls back to sleep. That means that the effective search time and, consequently, the receiver active time is significantly shorter, and power consumption is reduced, when no input signal is present. Calculation of Sync Search Time Out can be found in **“Clock and Data Recovery (CDR)” on Page 88**.

The On and Off time setting is different from the Constant On-Off Time Mode. The entire On time is defined in the **Self Polling Mode On Time Config A Register 0** and **Self Polling Mode On Time Config A Register 1**. Regardless of the numbers of RF channels and whether or not Multi- or Single-Configuration is used, the On time is defined with the Configuration A On-Timer. The deactivation of the receiver can happen at different times, but this event does not influence the timer stage, because the On time is still the same. So the master period is constant. The following scenarios are the same as before, but with Fast Fall Back to SLEEP.

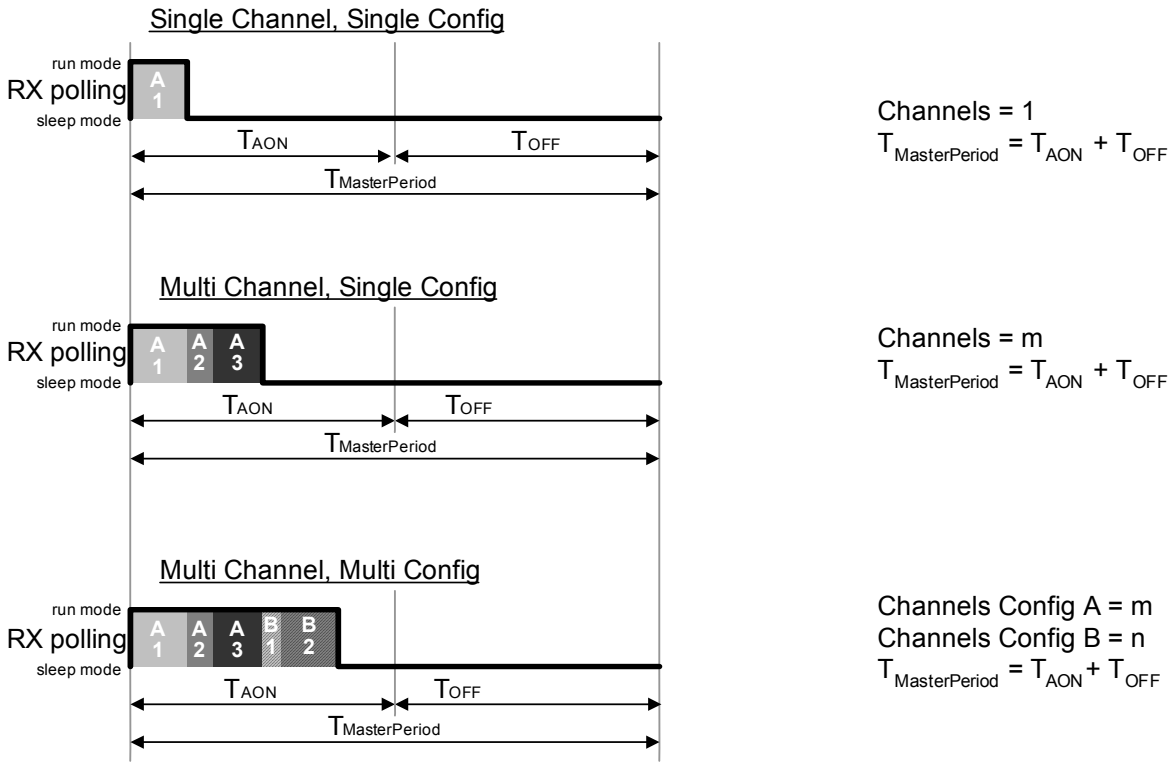


Figure 11 Fast Fall Back to SLEEP

Only the following receive modes (see **"Data Interface" on Page 35**) can be used:

- Packet Oriented FIFO Mode (POF)
- Packet Oriented Transparent Payload Mode (POTP)
- Transparent Mode - Chip Data and Strobe (TMCDS)

Ultra Fast Fall Back to Sleep (UFFB)

The needed time for detecting that no relevant transmission took place can be further reduced by using Ultrafast Fall Back to SLEEP (UFFB). When there was no Wake-up on Level criterion fulfilled in UFFB Mode during the Observation Time (TWULOT, see **"Wake-Up Generator" on Page 90**), then the system goes back to SLEEP (or to next config/channel). This can further reduce the receiver active time, when no data is available. When Wake-up on Level criterion was fulfilled, then the system proceeds with normal FFB functionality (SYSRCTO, optional Wake-up data criterion).

Ultrafast Fall Back to SLEEP is working, when a Wake-up on Data criterion is selected, the UFFBLCOO bit is enabled and FFB or PWUS mode is selected. The UFFB level criterion can be selected in the **Wake-Up Control Register**.

3.3.3.3 Mixed Mode (MM, Const On-Off & Fast Fall Back to SLEEP)

This mode combines Constant-On Time and Fast Fall Back to SLEEP within different configuration sets: Cfg.A: COO; Cfg.B: FFB; Cfg.C: FFB; Cfg.D: FFB

T_{ON} for Configuration A is always calculated according to Const On-Off rules.

T_{ON} for Configuration B, C and D is always calculated according to Fast Fall Back to SLEEP rules.

In Mixed Mode the On time of the first configuration within the FFB group is used. Below there are shown the same scenarios as before, but now for Mixed Mode. Note that Single-Configuration can be set, but is not recommended in Mixed Mode.

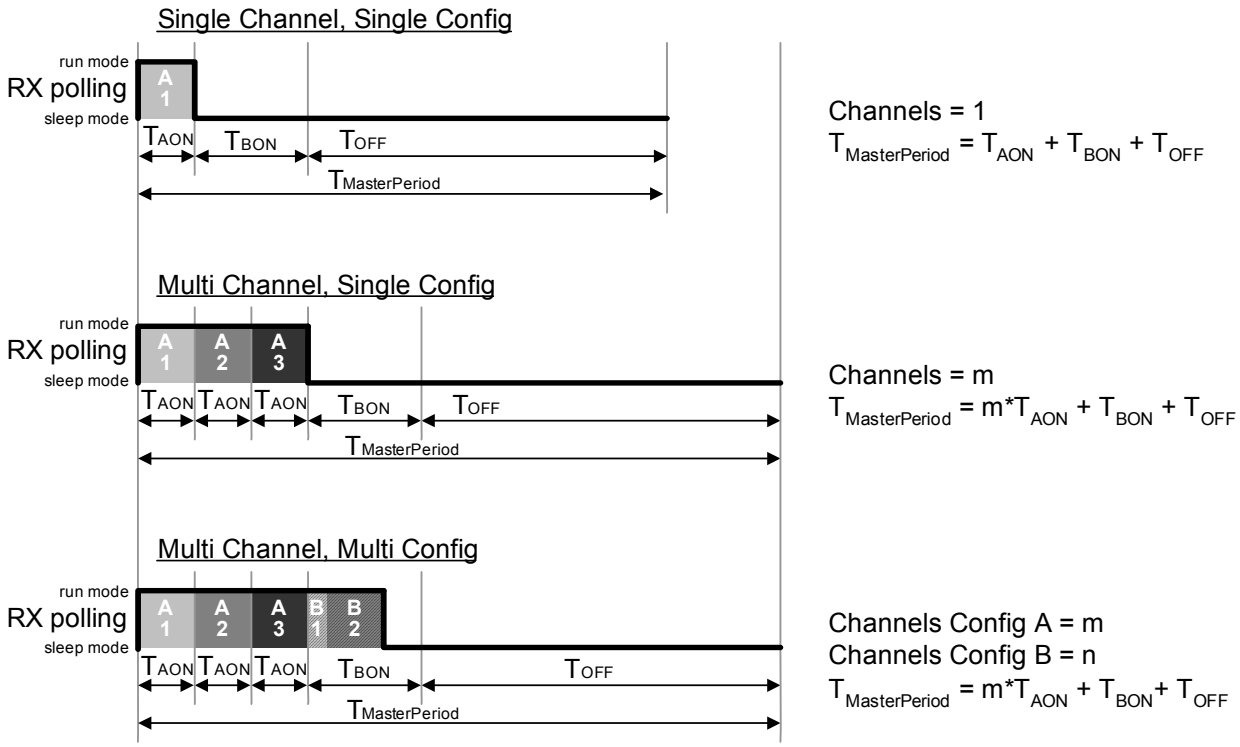


Figure 12 Mixed Mode

Only the following receive modes (see **"Data Interface" on Page 35**) can be used:

- Packet Oriented FIFO Mode (POF)
- Packet Oriented Transparent Payload Mode (POTP)
- Transparent Mode - Chip Data and Strobe (TMCDS)

3.3.3.4 Permanent Wake-Up Search (PWUS)

In this mode the receiver will work in Fast Fall Back Mode, but it will not go back to the SLEEP state after the last channel has been searched. Instead, it will start again from the beginning (Configuration A, RF Channel 1) until the On time has elapsed. The timing calculation can be seen in **Figure 13**. Ultrafast Fall Back to SLEEP functionality can be used as well.

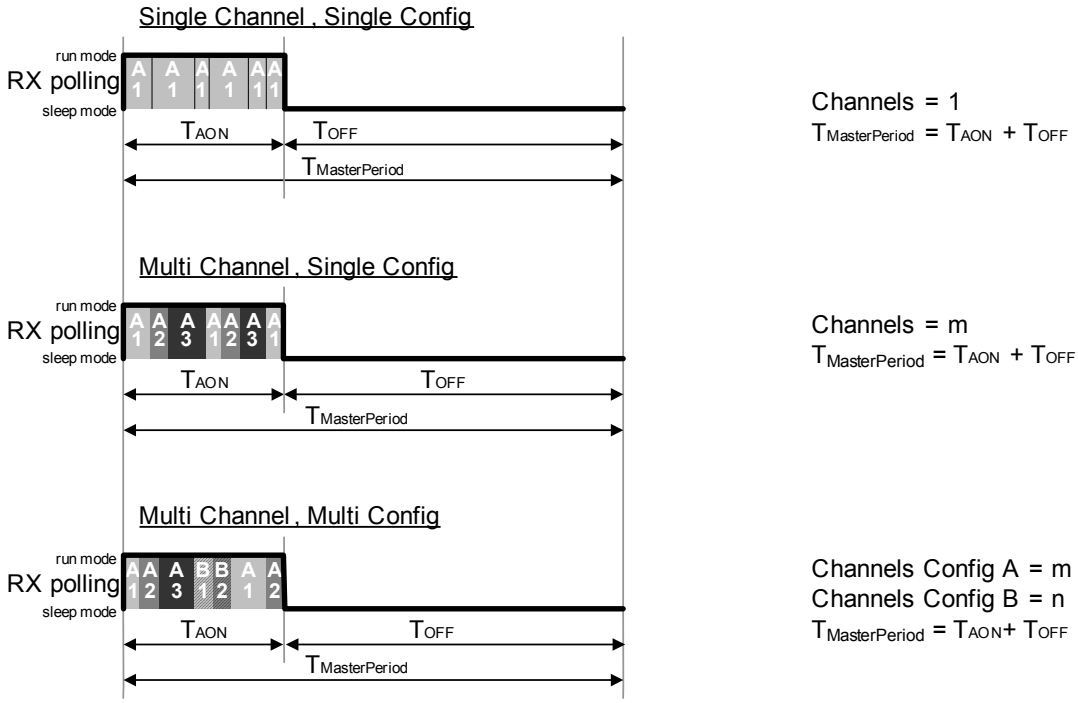


Figure 13 Permanent Wake-Up Search

Only the following receive modes (see **"Data Interface" on Page 35**) can be used:

- Packet Oriented FIFO Mode (POF)
- Packet Oriented Transparent Payload Mode (POTP)
- Transparent Mode - Chip Data and Strobe (TMCDS)

4 System Interface

In most applications, the TDA5340 transceiver IC is attached to an external micro controller. This so-called Application Controller executes a firmware which governs the TDA5340 by reading data from the transceiver when data has been received on the RF channel or write data to the transmit portion if some data needs to be sent. The firmware needs to handle the switching between receive and transmit mode and also the intialization of the transceiver device. The TDA5340 features an easy to use System Interface, which is described in this chapter.

Transparent Mode

The TDA5340 supports two levels of integration. In the most elementary fashion, it provides a rather rudimentary interface.

The incoming RF signal is demodulated and the corresponding data is made available to the Application Controller. Optionally, a chip clock is generated by the TDA5340.

The Application Controller can provide the baseband data to a single input pin which is modulated and amplified via the PLL and Power amplifier.

Since the data signal is always directly the baseband representation of the RF signal, we call this mode the Transparent Mode. The usage of the Transparent Mode will be described in **Chapter 4.3.2** for the receive mode and in **Chapter 4.3.4** for the transmit mode.

Packet Oriented Mode

Alternatively, the TDA5340 features the so-called Packet Oriented Mode which supports the autonomous reception and transmission of data telegrams. The Packet Oriented Mode provides a high-level System Interface which greatly simplifies the integration of the transceiver in data-centric applications. In Packet Oriented Mode, the data interface is based on chunks of synchronous data which are received in packets. In the easiest way, the Application Controller only reacts on the synchronous data it receives. The receiver autonomously handles the line decoding and the deframing of these data, and supports the timed reception of packets. Data is buffered in a receive FIFO and can be read out via the data interface. Further, the receiver provides support for the identification of wake-up signals. Details on the usage of the Packet Oriented Mode of the receiver are given in **Chapter 4.3.1** for the receive mode and in **Chapter 4.3.3** for the transmit portion.

4.1 Interfacing to the TDA5340

The TDA5340 is interfacing with an application by three logical interfaces, see **Figure 14**. The RF/IF interface handles the transmission of RF signals and is responsible for the modulation and demodulation. Its physical implementation has been described in **"RF / IF Receiver" on Page 55**, **"Receiver Baseband" on Page 69**, for the receiver and in **"Transmitter" on Page 58**, **"Transmitter Baseband" on Page 67** for the transmitter. The other two logical interfaces establish the connection to the Application Controller. Note that due to the high level of integration of the transceiver, these interfaces impose minor requirements on the Application Controller, which can be as simple as an 8-bit micro controller operated at low clock rate. As will be shown later, the physical implementation of the data interface depends on whether the transceiver is operating in Packet Oriented or in Transparent Mode. For the sake of clarity, the communication between the TDA5340 and the Application Controller is split into control flow and data flow. This separation leads to an independent definition of the data interface and the control interface, respectively.

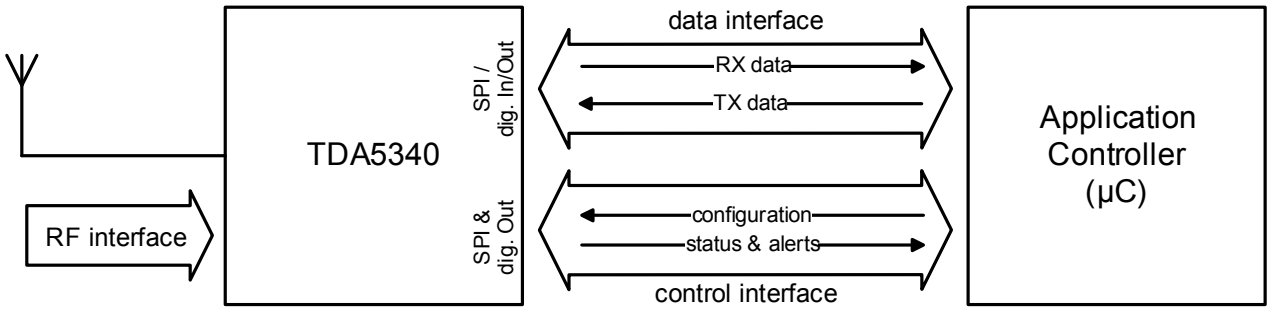


Figure 14 Logical and electrical System Interfaces of the TDA5340

4.2 Control Interface

The control interface is used in order to configure the TDA5340 after start-up or to re-configure it during run-time, as well as to properly react on changes in the status of the transceiver in the Application Controller's firmware. The control interface offers a bi-directional communication link by which

- **configuration data** is sent from the Application Controller to the TDA5340,
- the transceiver provides **status information** (e.g. the status of a data reception) as response to a request it has received from the Application Controller and the
- TDA5340 autonomously **alerts** the Application Controller that a certain, configurable event has occurred (e.g. that a packet has been received successfully, the FIFO buffer needs a reload).

Configuration and status information are sent via the 4-wire SPI interface as described in **"Digital Control (4-wire SPI Bus)" on Page 41**. The configuration data determines the behavior of the transceiver, which comprises

- scheduling the inactive power-saving modes as well as the active receive / transmit modes,

- selecting the properties of the RF/IF interface configuration (e.g. carrier frequency selection, filter settings), configuring the properties of the frames.
- configuring the properties of the frames (e.g. wake-up patterns, Telegram Start Identifier (TSI), and optionally specifying the position, format and content of patterns within packets that stimulate a certain, configurable alerting behavior (Message ID)).

Note that the TDA5340 transceiver IC supports reception of multiple configuration sets on multiple channels in a time-based manner without reconfiguration. Thus, the RF/IF interface as well as the frame format properties support alternative settings, which can be activated autonomously by the transceiver as part of the scheduling process.

In contrast to the high-level interface used for communicating configuration instructions and status information, alerts are emitted by the transceiver on a digital output pin that may trigger external interrupts in the Application Controller. Note that the alerting conditions as well as the polarity of the output pin are configurable, see **"Interrupt Generation Unit" on Page 50**.

4.3 Data Interface

The data interface between the Application Controller and the TDA5340 transceiver IC is used for the transport of the received and transmitted data, see **Figure 14**. The physical implementation as well as the features of the data interface depend on the selected mode of operation.

There are 5 possible receive modes:

- Packet Oriented FIFO Mode (POF)
- Packet Oriented Transparent Payload Mode (POTP)
- Transparent Mode - Chip Data and Strobe (TMCDS)
- Transparent Mode - Matched Filter (TMMF)
- Transparent Mode - Raw Data Slicer (TMRDS)

Access points for these receive modes can be seen in **Figure 58**.

The possible combinations of receive modes and polling mode setup is noted in **Figure 15**.

Self Polling Mode / RX Mode - available signal	Const ON-OFF					Fast Fall Back (UFFB), Mixed, PWUS			
	WU on Level criterion		WU on data criterion			WU on Level criterion		WU on data criterion	
	RSSI	Signal Recognition	Sync	Random, Equal, Pattern		RSSI	Signal Recognition	Sync	Random, Equal, Pattern
POF - FIFO	√	√	√	√		√	√	√	√
POTP - RXD - RXSTR	√	√	√	√		√	√	√	√
TMCDS - CH_DATA - CH_STR	√	√	√	-		√	√	√	-
TMMF - DATA_MATCHFIL	√	-	-	-		-	-	-	-
TMRDS - DATA	√	-	-	-		-	-	-	-

Legend:

√ ... available

- ... not available

Figure 15 Receive Modes

There are 4 possible transmit modes:

- Start Bit FIFO Mode (SBF)
- Direct FIFO Mode (DF)
- Synchronous Transparent Mode (STM)
- Asynchronous Transparent Mode (ASTM)

4.3.1 Packet Oriented Receive Modes

The TDA5340 features the so-called Packet Oriented Mode which supports the autonomous reception of data telegrams. The Packet Oriented Mode provides a high-level System Interface which greatly simplifies the integration of the transceiver in data-centric applications. In Packet Oriented Mode, the data interface is based on chunks of synchronous data which are received in packets. In the easiest way, the Application Controller only reacts on the synchronous data it receives. The receiver autonomously handles the line decoding and the de framing of these data, and supports the timed reception of packets. Data is buffered in a receive FIFO and can be read out via the data interface. Further, the receiver provides support for the identification of wake-up signals.

Packet Oriented FIFO Mode (POF)

In Packet Oriented FIFO Mode, data is transferred via the 4-wire SPI bus. During receive operation, the incoming RF signal is demodulated in the RF/IF interface, the line decoding is performed and the data, of which wake-up frames, data frame headers and optional footers have been stripped off, is stored in the RX FIFO. Then, the received data can be read from the RX FIFO using the “read FIFO” command described in **Chapter 4.5** and **Chapter 4.4**. The data which is read from the RX FIFO is accompanied by information which contains the status of the respective receive operation. Note that the availability of received data packets is communicated via alerts in the control interface.

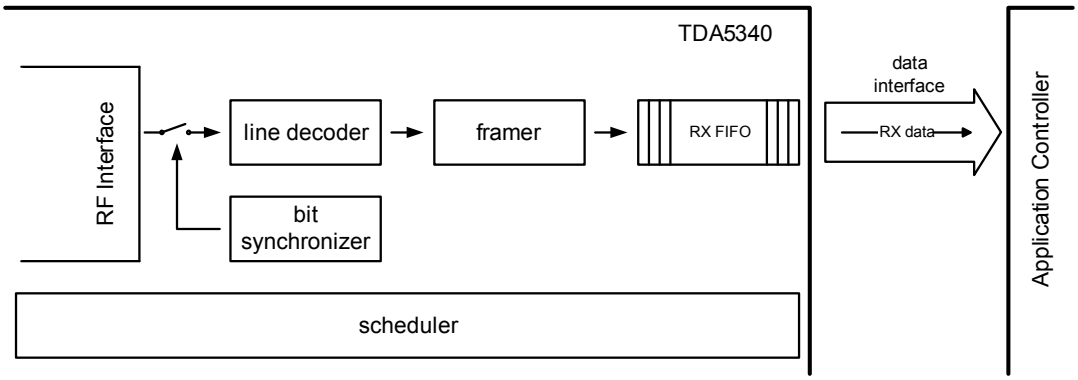


Figure 16 Data interface for the Packet Oriented FIFO Mode

Packet Oriented Transparent Payload Mode (POTP)

Packet Oriented Transparent Payload Mode (POTP) This mode is very similar to POF Mode as data which is going into FIFO is also available via RXD and RXSTR signals (see **Chapter 4.7**).

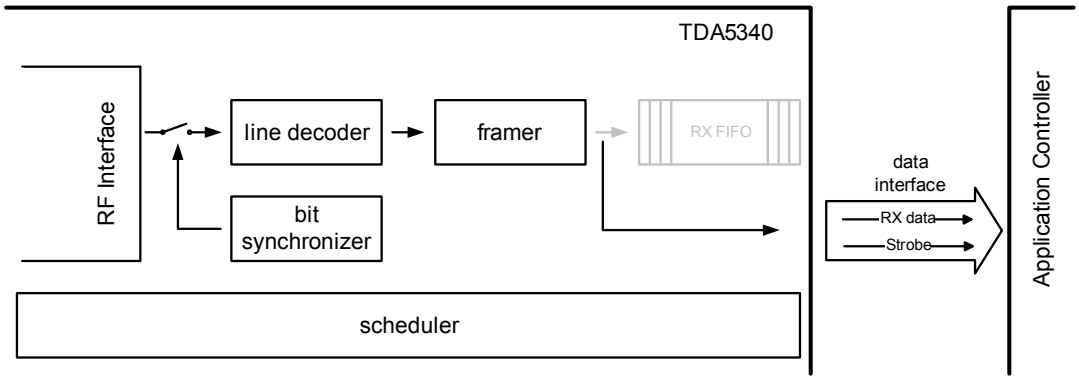


Figure 17 Data interface for the Packet Oriented Transparent Payload Mode

In the TDA5340, there are specific digital output lines (PPx pin) for the Bi-phase decoded data and an appropriate Strobe signal. During inactivity of the receiver, the line is in default mode switched to low. In default mode the

Strobe signal is active high and has a delay of $T_{BIT}/16$ relative to the data bit and a duration of $T_{BIT}/2$. The polarity of the Strobe signal is programmable, this can be done via **PPx Port Configuration Register** .

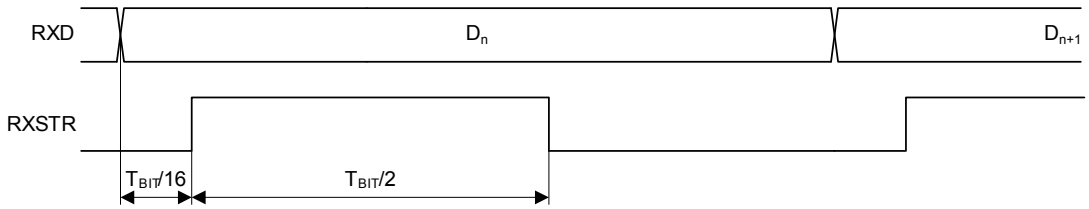


Figure 18 Timing of the Packet Oriented Transparent Payload Mode

4.3.2 Transparent Receive Modes

The receiver's simple plain data interface in this Transparent Mode is shown in **Figure 19**. In this mode, the demodulated data signal is made directly available on the data output pin of the data interface. The demodulated received data of the TDA5340 can be provided without any additional information of the frame structure. The Transparent Mode has two main subgroups which can be distinguished by the usage of the Clock Data Recovery (CDR) block. By using the CDR the TDA5340 provides the baseband data with the recovered encoding data clock.

Transparent Mode - Chip Data and Strobe (TMCDS)

The chip data and chip clock represents the recovered baseband data and clock of the CDR. Note that a sensible chip clock can only be generated if the selected line encoding exhibits a constant chip rate. The chip clock generation can be significantly improved by using a run-in signal of alternating one-zero chips (maximum number of transitions within a data stream).

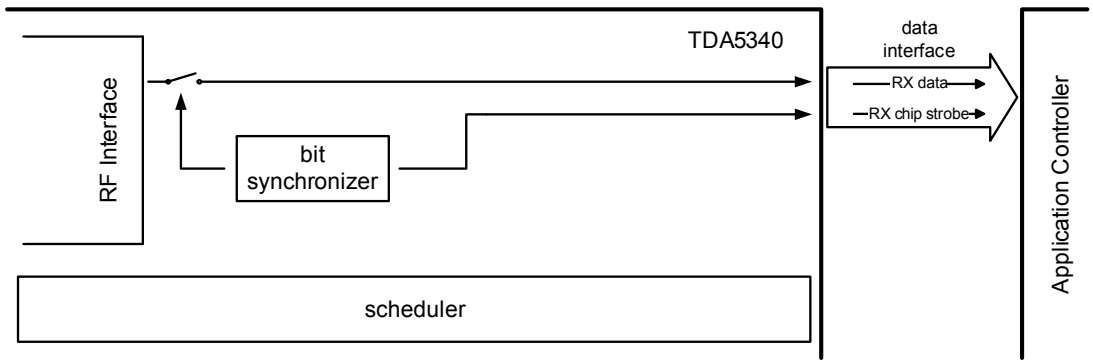


Figure 19 Data interface for the Transparent Mode - Chip Data and Strobe

In the TDA5340, there is a specific digital output line for the chip clock estimate as well as for the data output line, which delivers the encoded chip data. During inactivity of the receiver, the line is in default mode switched to low. The PPx pin provides the estimated chip clock, if CH_STR is selected. Further details are given in **Chapter 4.7**. In default mode the CH_STR signal is active high and has a delay of TCHIP/8 relative to the data chip and a duration of TCHIP/2. The polarity of the CH_STR signal is programmable, this can be done via **PPx Port Configuration Register**.

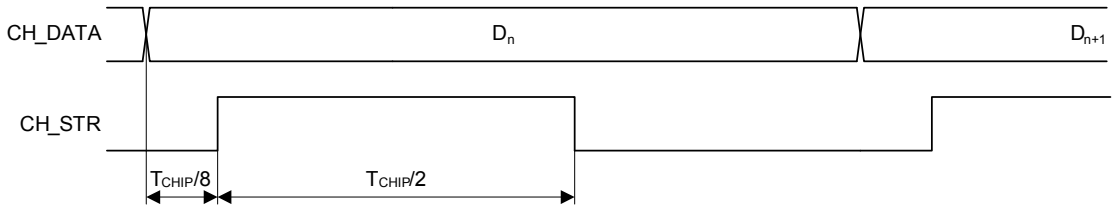


Figure 20 Timing of the Transparent Mode - Chip Data and Strobe

Transparent Mode - Matched Filter (TMMF)

The received data after the Matched Filter (Two-Chip Matched Filter) with an additional SIGN function is provided via the DATA_MATCHFIL signal (PPx pin). In this mode sensitivity measurements with ideal data clock can be performed very simple. For further details see the block diagram in **Figure 58**.

Sensitivity in this transparent mode significantly depends on the implemented clock and data recovery algorithm of the user software in the application controller.

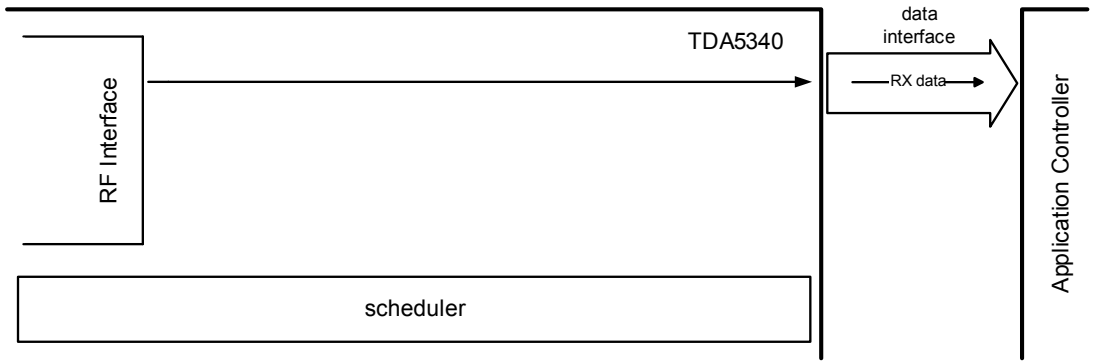


Figure 21 Data interface for the Transparent Modes TMMF / TMRDS

Transparent Mode - Raw Data Slicer (TMRDS)

This mode supports processing of data even without bi-phase encoding by providing the received data via the One-Chip Matched Filter on the DATA signal (PPx pin). See more details in the block diagram in **Figure 58**. Sensitivity in this transparent mode significantly depends on the implemented clock and data recovery algorithm of the user software in the application controller. The data interface can be seen from **Figure 20**.

Self Polling mode is possible as well, but only Constant On-Off Mode and Wakeup on RSSI makes sense. Assume one of the TDA5340 configurations (e.g. Configuration B) is set for external data processing mode. See also example in **Figure 22**. The needed On time (latency through TDA5340) is configured in the corresponding On time registers of the chip. The interrupt for Wake-Up Config B (WUB) is enabled and suitable RSSI thresholds are set. If the RSSI signal is in a valid threshold area, the TDA5340 changes to Run Mode Self Polling and an interrupt can be signaled to the Application Controller. In case the RSSI signal is outside the valid threshold area, the chip stays in Self Polling Mode and the external controller gets no interrupt (as the desired RSSI level is not reached).

It should be mentioned that all Time-out Timers (TOTIMs) should be disabled in the configuration set of the external processing mode as the micro controller takes over the control (see SFR bit group EXTPROC in the **Channel Configuration Register**).

It is recommended to put this external configuration at the end of the On time within the polling cycle (so right before the Off time). This is helpful when using the “EXTTOTIM” command (go to Self Polling Mode, next programmed channel or Configuration A). When the external configuration is the last configuration before the Off time, then the next programmed channel within the polling cycle would be the sequence of the Off time. When data

is available and the RSSI is within a valid threshold area, an interrupt is generated (NINT). So the Application Controller can process the data and decide about valid data.

In case the controller decides that wrong data was sent, the micro controller can send the register command “EXTTOTIM” (see **External Processing Command Register** register). When the micro controller detects valid data, then the controller can send the register command “EXTEOM found” (see **External Processing Command Register**) after completing the data reception.

The functionality described above can also be used for other receive modes (mainly TMMF, TMCDS), where the external micro controller takes on responsibility for further data processing.

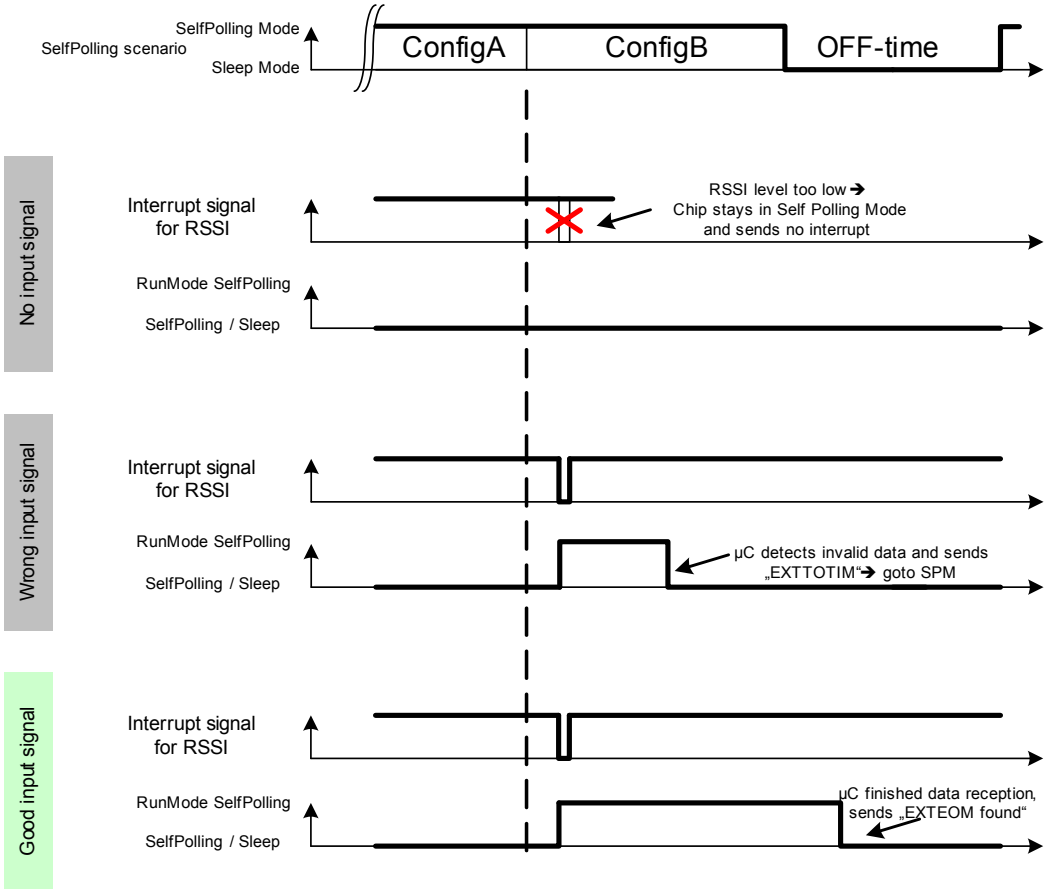


Figure 22 External Data Processing

The SFR bit group EXTPROC in the **Channel Configuration Register** can be activated for each configuration set for an easier handling of external data processing by the Application Controller. Depending on the intended transparent receive mode an activation of this function means:

- Data path in front of Framer Unit is no longer closed (so that no data is going into Framer Unit accidentally)
- Interrupts for FSync, MID and EOM are deactivated internally
- Some/all TOTIM counters are deactivated
- Some/all Wake-up on Data Criteria are disabled
- Wake-up on Signal Recognition is/is not disabled

4.3.3 TX FIFO Modes

The transmit FIFO can be used to reduce the real-time requirements of the host Micro controller. The transmit FIFO can be loaded with a SPI command which is described in **Figure 30**.

We distinguish between Start Bit FIFO Mode (SBF) and Direct FIFO Mode (DF).

Direct FIFO Mode (DF)

The Direct FIFO Mode enables the fastest transition from Init TX state to TX FIFO state. The transmitter will start if a FIFO content is loaded right after the PLL settling time (TX Ready Mode) to shift out the FIFO content with the pre configured output power, modulation scheme, center frequency, data rate and coding. By reloading the TX FIFO the transmission will continue as long the FIFO is not empty. After sending the last Bit /Chip out of the FIFO an interrupt can be generated to signal the host controller that the transmission of the FIFO content has finished.

The TDA5340 either waits for a refill of the TX FIFO in the TX FIFO empty state and sends out the last Bit / Chip of the FIFO content as long as a new FIFO content is loaded.

If the TX Idle transition is enabled the Transceiver will go immediately after the TX empty interrupt into the TX Idle state and waits for a user interaction (SPI access) which can be TX PLL initialization or a change to a other mode.

With the enabled finish transmission with TX FIFO Empty bit (see **TX Control Register**) the transceiver will wait for restart of the transmission in the TX Ready state, the FIFO Empty and TX Ready interrupt flags are set in the **Interrupt Status Register 2**.

Start Bit FIFO Mode (SBF)

If the FIFO is already loaded the transmission start only after setting the TX start bit in the **TX Control Register**. The SBF mode can be used to enable exact timings of the transmitter.

By reloading the TX FIFO the transmission will continue as long as the FIFO is not empty. After sending the last Bit /Chip out of the FIFO a interrupt can be generated to signal the host controller that the transmission of the FIFO content has finished.

The TDA5340 either waits for a refill of the TX FIFO in the TX FIFO Empty state and sends out the last Bit / Chip of the FIFO content as long as the start bit is set again in the **TX Control Register**.

After the TX Empty interrupt the Transceiver will go immediately into the the TX Idle state if the TX idle transition is enabled and waits for a user interaction (SPI access) which can be TX PLL initialization or a change to another mode.

With the enabled finish transmission with FIFO Empty bit the transceiver will wait for restart of the transmission in the TX Ready state, the FIFO Empty and TX Ready interrupt flags are set in the **Interrupt Status Register 2**.

4.3.4 TX Transparent Mode

The transparent mode can be also subdivided into a synchronous and asynchronous transparent mode. In transparent mode the data transmission is started with the transparent TX SPI command (see **Figure 31 “Transparent TX Command” on Page 44**).

Synchronous Transparent Mode

The synchronous transparent mode utilize a the on-chip baud rate generation unit to synchronize the incoming data stream. The baud rate generator can be programmed via a 16 Bit word which is a dividing factor of the Crystal frequency. The baseband data has to be synchronized with the baud rate strobe and provided on the SDI line (Pin 18), during the transmission the NCS line must be low. The TDA5340 can either executes a coding of the input data (coded synchronous transparent mode) or shifts the data provided on the SDI line directly to the modulator (synchronous NRZ mode).

The transmission is terminated by releasing the NCS line to high but the power amplifier is disabled after transmitting of the complete last Bit / Chip. The Picture below shows the produced baseband data by using the Synchronous Transparent Mode.

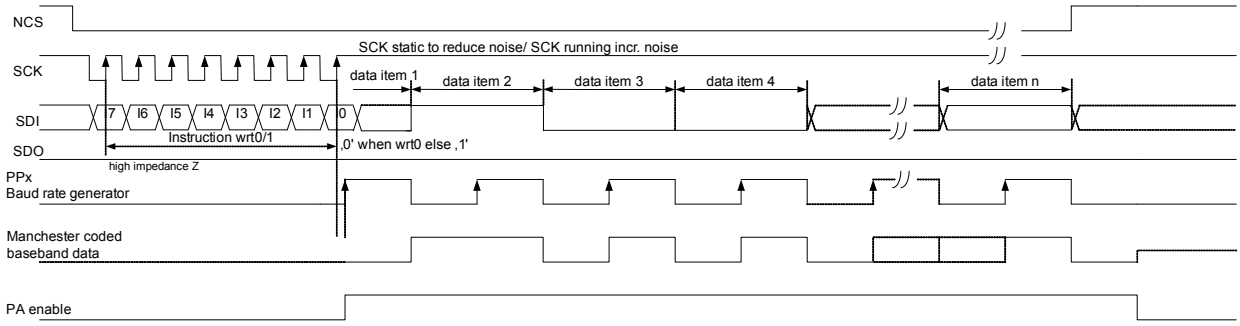


Figure 23 Synchronous Transparent Mode

Asynchronous Transparent Mode

In some applications a change of data rate within one transmission is necessary. In this case the asynchronous transparent mode has to be used. The data which are provided on the SDI line are directly modulated.

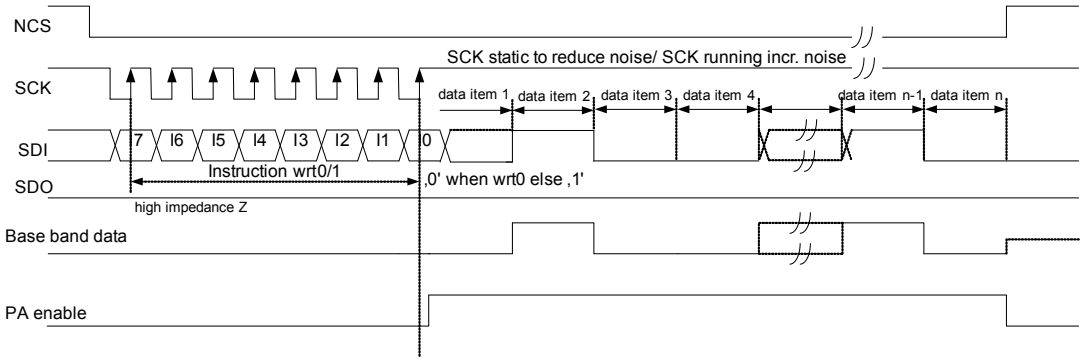


Figure 24 Asynchronous Transparent Mode

Attention: If BT of Gaussian filter is less than 0.5, data edge uncertainties may occur.

4.4 Digital Control (4-wire SPI Bus)

The control interface used for device control and data transmission is a 4-wire SPI interface.

- NCS - select input, active low
- SDI - data input
- SDO - data output
- SCK - clock input: Data bits on SDI are read in at rising SCK edges and written out on SDO at falling SCK edges.

Level Definition:

- logic 0 = low voltage level
- logic 1 = high voltage level

Note: It is possible to send multiple frames while the device is selected. It is also possible to change the access mode while the device is selected by sending a different instruction.

Note: In all bus transfers MSB is sent first, except for the received data read from the FIFO. There the bit order is given as first bit received is first bit transferred via the bus.

Table 3 Instruction Set

Instruction	Description	Instruction Format
WRB	Write to chip in Burst mode	0x01
WR	Write to chip	0x02
RD	Read from chip	0x03
RDF	Read FIFO from chip	0x04
RDB	Read from chip in Burst mode	0x05
WRF	Write FIFO	0x06
WRT0	Write transparent transmit data with starting low data	0x08
WRT1	Write transparent transmit data with starting high data	0x07

Write Command

To write to the device, the SPI master has to select the SPI slave unit first. Therefore, the master must set the NCS line to low. After this, the instruction byte and the address byte are shifted in on SDI and stored in the internal instruction and address register. The following data byte is then stored at this address. After completing the writing operation, either the master sets the NCS line to high or continues with another SPI command. Additionally the received address byte is stored into the **SPI Address Tracer Register** and the received data byte is stored into the **SPI Data Tracer Register**. These two trace registers are readable.Therefore, an external controller is able to check the correct address and data transmission by reading out these two registers after each write instruction. The trace registers are updated at every write instruction, so only the last transmission can be checked by a read out of these two registers.

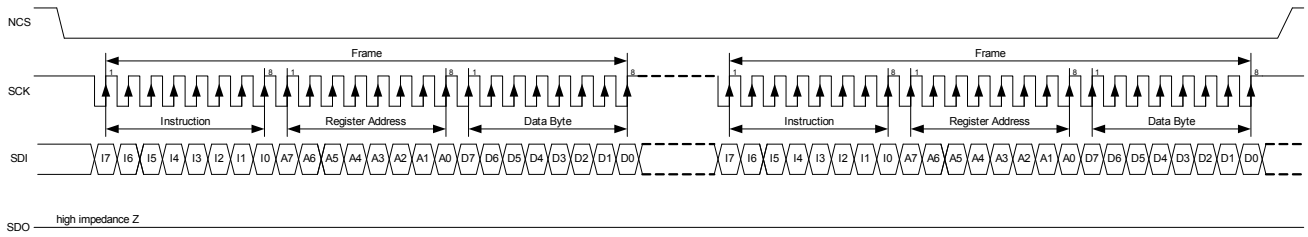


Figure 25 Write Register

Burst Write Command

To write to the device in Burst mode, the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte and the start address byte have been transferred to the SPI slave (MSB first) the successive data bytes will be stored into the automatically addressed registers. To verify the SPI Burst Write transfer, the current address (start address, start address + 1, etc.) is stored in **SPI Address Tracer Register** and the current data field of the frame is stored in **SPI Data Tracer Register**. At the end of the Burst Write frame the latest address as well as the latest data field can be read out to verify the transfer.

Note that some error in one of the intermediate data bytes are not detected by reading **SPI Data Tracer Register**.

Driving the NCS line to high will end the Burst frame.

A single SPI Burst Write command can be applied very efficiently for data transfer either within a register block of configuration dependent registers or within the block of configuration independent registers.

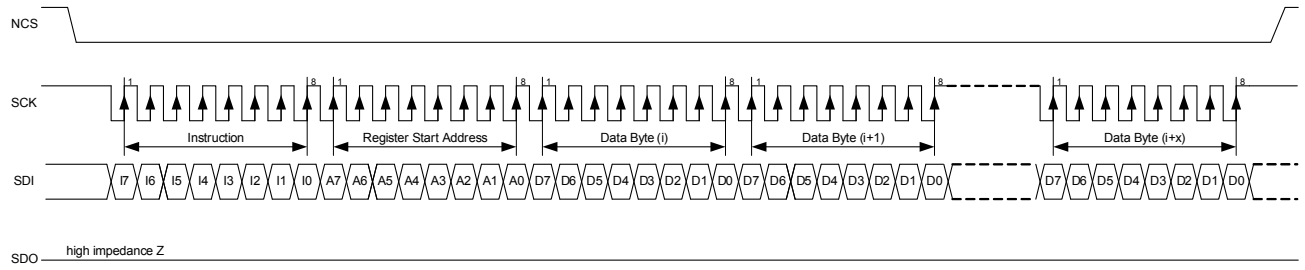


Figure 26 Burst Write Registers

Read Command

To read from the device, the SPI master has to select the SPI slave unit first. Therefore, the master must set the NCS line to low. After this, the instruction byte and the address byte are shifted in on SDI and stored in the internal instruction and address register. The data byte at this address is then shifted out on SDO. After completing the read operation, either the master sets the NCS line to high or continues with another SPI command.

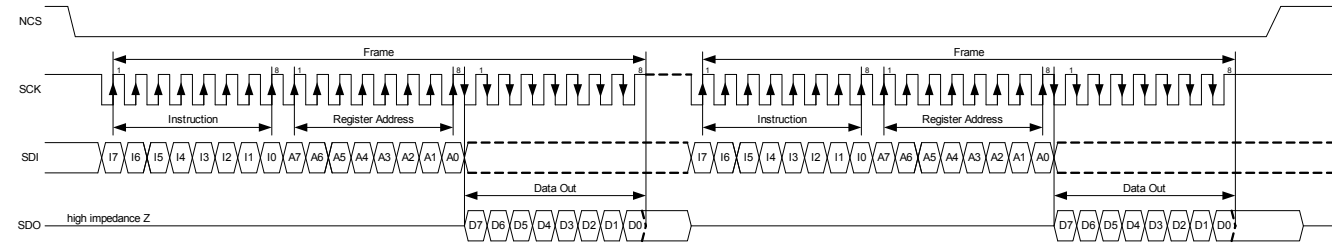


Figure 27 Read Register

Burst Read Command

To read from the device in Burst mode, the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte and the start address byte have been transferred to the SPI slave (MSB first), the slave unit will respond by transferring the register contents beginning from the given start address (MSB first). Driving the NCS line to high will end the Burst frame.

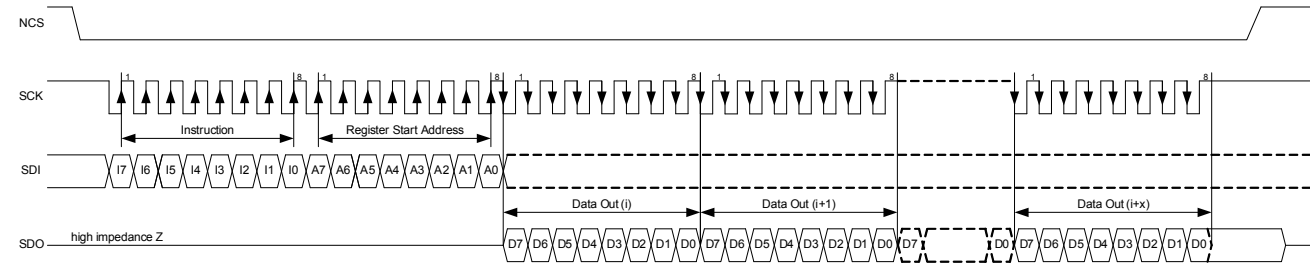


Figure 28 Burst Read Registers

Read FIFO Command

To read the FIFO, the SPI master has to select the SPI slave unit first. Therefore, the master must set the NCS line to low. After this, the instruction byte is shifted in on SDI and stored in the internal instruction register. The data bits of the FIFO are then shifted out on SDO. The following byte is a status word that contains the number of valid bits in the data packet. After completing the read operation, either the master sets the NCS line to high or continues with another SPI command.

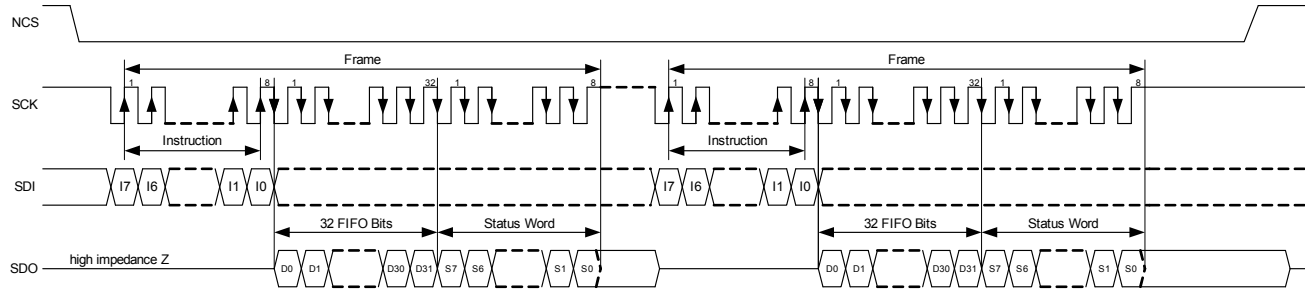


Figure 29 Read FIFO

Write FIFO Command

To write to the TX FIFO the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte (MSB first) the next byte contains the number of data items (chip or bit) minus 1 to be transferred to the FIFO. Therefore 0x00 means a single data item, whereas 0xFF means 256 data items. Successive data bytes contain the data items to be stored into the FIFO. Only the number of data items specified in the 2nd byte of the instruction will be stored into the FIFO. Other bits are skipped. At the end of the access frame the master has to deselect the slave unit by driving the NCS line to high.

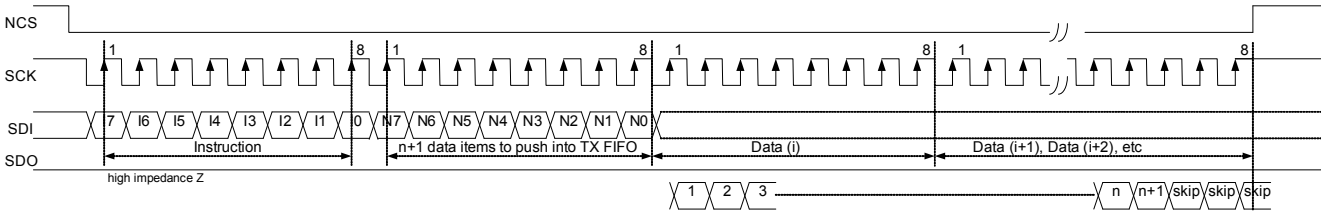


Figure 30 Write TX FIFO

Transparent TX Command

To transfer data items (chip/bit) via SPI in transparent TX mode the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte (MSB first) the SCK should stay static to reduce noise during transmit.

Note that there are 2 versions of the same command available. They differ only in the LSB of the instruction. The intent of this is to pre-set the level of the SDI line to the level of the first TX data item (chip/bit). A new data item is sampled every positive edge of the Baud rate generator strobe.

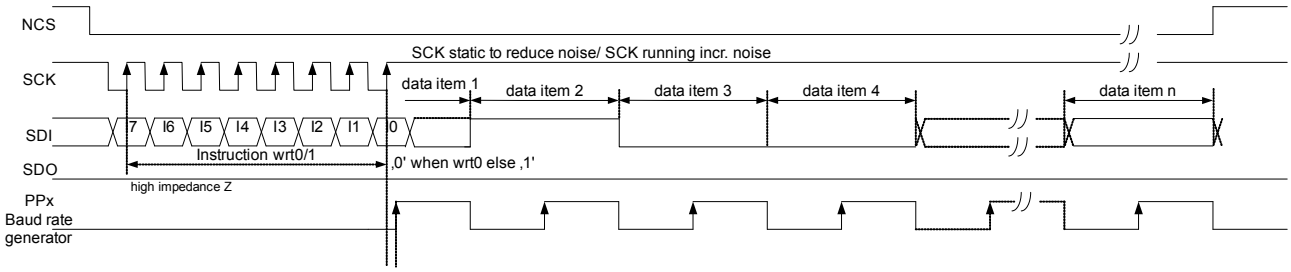


Figure 31 Transparent TX Command

SPI Check Sum

The SPI also includes a safety feature to verify the SPI communication by which the checksum is calculated with an XOR operation from the address and the data when writing SFR registers content. The checksum is in fact an

XOR of the data 8-bitwise after every 8 bits of the SPI write command. The calculated checksum value is automatically written in the **SPI Checksum Register** and can be compared with the expected value. After the **SPI Checksum Register** is read, its value is cleared. In case of an SPI Burst Write and Write FIFO frame, a checksum is calculated from the SPI start address and consecutive data fields.

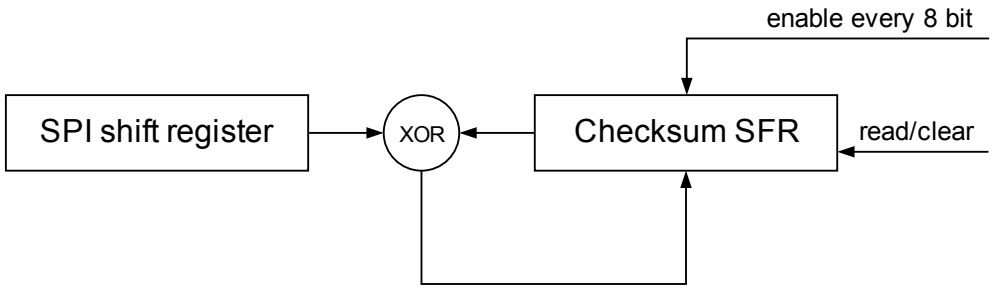


Figure 32 SPI Checksum Generation

4.5 Receive FIFO (RX FIFO)

The Receive FIFO is the storage of the received data frames and is only used in the POF Mode. It is written during data reception. The host micro controller is able to start reading via SPI right after frame sync (interrupt) or in the most common case right after detection of EOM (interrupt). The FIFO can store up to 288 received data bits. If the expected data transmission contains more bits (note that in TSI 8-bit Extended Mode one bit is added in front of the real payload to indicate which of the two TSI pattern has matched), the reading from FIFO can be triggered with the FIFO almost full interrupt to prevent an overrun. The fill level of the FIFO where a FIFO almost full interrupt should be generated can be programmed in the **RX FIFO Almost Full Level Register**.

Architecture

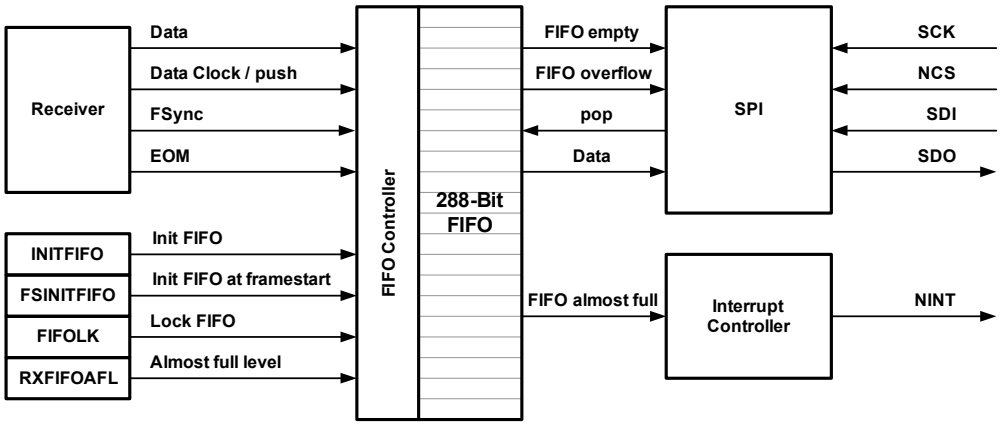


Figure 33 Receive FIFO

The write port is controlled by the Digital Receiver using the push command. Writing data into the FIFO starts with the detection of a Telegram Start Identifier (TSI). The Write Address Pointer is incremented with each data clock signal generated by the Digital Receiver. The read port is controlled by the SPI controller using the pop command. Each bit read from the SPI controller increments the Read Address Pointer. The Read and Write Address Pointers jump from their maximum value (287d) to address zero. Writing to the FIFO stops at EOM or after Sync loss.

FIFO Lock Behavior

The FIFO possesses a lock mechanism that is enabled via the SFR bit FIFOLK in the Receiver Control register (**RX Control Register**). If this mechanism is enabled, the FIFO will enter a FIFO Lock state at the detection of the End of Message (EOM) criterion. During the time that the FIFO is locked, it is not possible to receive additional data in Run Mode Self Polling. This means that it is only possible to detect another wake-up in the Self Polling Mode, but no more data in the Run Mode Self Polling. This will guarantee that only the first complete data packet is stored in the FIFO. Enabling the FIFOLK also locks the digital receiver chain at EOM until release from FIFO lock state.

The FIFO will remain locked unless one of three conditions occurs:

- The remaining contents of the FIFO are completely read out via the SPI
- The SFR control bit FIFOLK is cleared in the **RX Control Register** register
- INITFIFO at Cycle Start is set in the **RX Control Register** and
  - FSM is switched to Run Mode Slave or
  - FSM switches from Self Polling Mode to Run Mode Self Polling

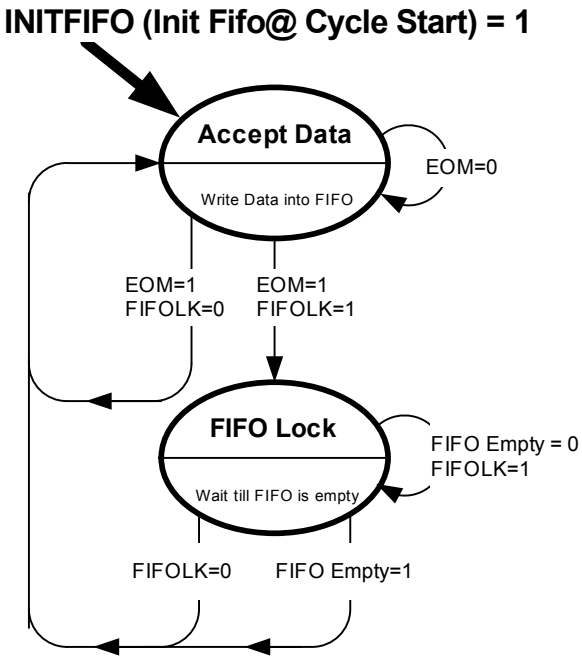


Figure 34 FIFO Lock Behavior

FIFO Status Word

The FIFO Status Word is attached at the end of a FIFO SPI transmission, and shows if there was an overflow, and how many valid data bits were transmitted. The number of valid FIFO bits is indicated at bit positions S0 to S5. S6 of the Status Word is always undefined.

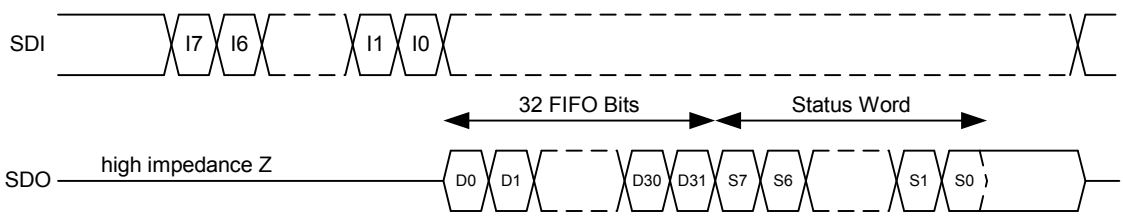


Figure 35 SPI Data FIFO Read

If the Write Address Pointer outruns the Read Address Pointer, an overflow is indicated in the FIFO Overflow Status bit in the FIFO Read Status Word at position S7. All 32 FIFO bits and the bits S5 to S0 of the Status Word are undefined while the Overflow Status bit is set. If a TSI is detected after an overflow, the FIFO Overflow Status bit is cleared and the entire receive FIFO is initialized.

Initialization

Additionally, there are two possibilities to initialize the receive FIFO.

- If the INITFIFO bit is set in the **RX Control Register** (“Init FIFO at Cycle Start”) the entire receive FIFO is always initialized
  - after switching to Run Mode Slave or
  - switching from Self Polling Mode to Run Mode Self Polling.
- If the FSINITFIFO bit in **RX Control Register** is set, the entire receive FIFO is initialized when a TSI is detected and the receive FIFO is not locked (“Init FIFO at Frame Start”).

Last received message length

For application protocols with several payload frames and only a short pause in-between, the micro controller would have to read out the FIFO very fast after detection of an EOM. Thus even slow or overloaded Application Controllers have the possibility now to determine the end of the last message, when reading out the FIFO, while the next payload frame gets already received and payload data is further stored in the FIFO. Therefore the last received message length (e.g. after an EOM event) is stored in **Payload Data Length Register** and the upper two bits of **RF PLL Actual Channel and Configuration Register** at TSI detection of the next message. The upper two bits of **RF PLL Actual Channel and Configuration Register** hold the MSBs, thus a message length of 256 up to 1023 payload bits can be represented. A saturation of the message length at the maximum value of 1023 is realized. Storage at TSI of the next message ensures that even wrong payload data (e.g. if MID is not matching, no EOM will be generated, but payload is kept in FIFO. Or EOM data length criterion is selected only and a sync loss prevents from generating an EOM event) can be identified.

On initialization of the FIFO, the **Payload Data Length Register** and the upper two bits of **RF PLL Actual Channel and Configuration Register** are cleared. The corresponding internal counter is cleared with every TSI detection and initialization of the FIFO.

4.6 Transmit FIFO (TX FIFO)

The Transmit FIFO acts as a data buffer between the baseband data and the host micro controller to reduce the real time requirements and active time of the host controller. The transmit FIFO can only be used combined with the Baud rate generator which generates the output timing of the baseband data.

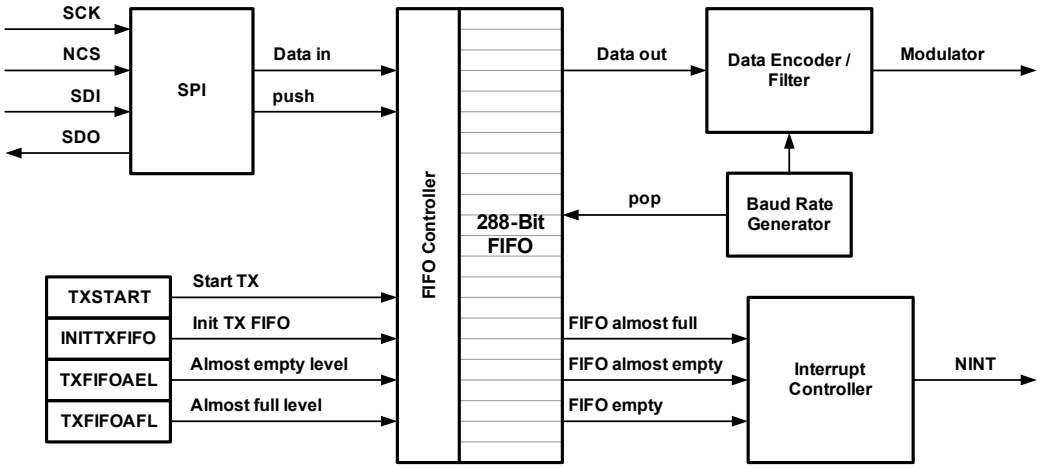


Figure 36 TX FIFO

Fill Level Signalization

There are three types of interrupts which can be enabled and triggered by the TX FIFO.

- FIFO empty (IS2.TXEMPTY)
- FIFO almost empty (IS2.TXAE)
- FIFO almost full (IS2.TXAF)

With the FIFO empty interrupt the host controller can be informed that the transmission has finished and the TDA5340 is now ready to start a new transmission or go to another main state.

For continuous data transmission where the payload data length exceeds the FIFO size the FIFO almost empty interrupt can be used to trigger a refill of the FIFO to keep the transmission ongoing. The trigger level can be programmed with the FIFO almost empty level (**TX FIFO Almost Empty Level Register**) to give flexibility in reaction time to the host controller.

The FIFO almost full interrupt can be utilized to avoid a congestion of the TX FIFO by the host controller. The almost full level can be programmed in a SFR (**TX FIFO Almost Full Level Register**) and represents the distance in bits to the maximum of the FIFO.

FIFO Initialization

The TX FIFO can be initialized by two ways.

- Power Down Mode / RESET
- Programming of SFR register bit TXC.INITTXFIFO

If the TX FIFO is initialized the read and write pointers are set to 0 position of the FIFO. If the initialization of the TX FIFO is done during the transmission in the TX FIFO Mode the FIFO empty interrupt will be generated and the TX FIFO empty state entered.

4.7 General Purpose Output Pins

As long as the P_ON pin is high, all digital output pins operate as described. If the P_ON pin is low, all digital output pins are switched to high impedance mode.

The digital outputs PP0, PP1 are PP2 are fully configurable within the **PP0 and PP1 Configuration Register**, **PP2 and PPRF Configuration Register** and **PPRF_RSSI Configuration Register**, where each of the signals listed below can be routed to any of the three output pins. The default configuration for these three output pins can be seen in **Table 1 “Pin Definition and Function” on Page 15**

The PPRF Pin has mainly the same function as described in the table below but the logic level will be independent of the supply voltage domain always follow the VDDRF voltage. It is also not possible to select the Clock Out Signal for this Pin. In Sleep Mode where all analog supplies are turned off including the VDDRF, this Pin will be set to high Z.

The TDA5340 has also the ability to use the PPRF_RSSI as general purpose output pin (same functionality like PPRF Pin). The general purpose functionality can be enabled by disabling the RSSI buffer in the **RSSI Configuration Register** . The output current driving capability of this pin as general purpose output is limited to 300 µA.

All the Signals listed in **Table 4** can be inverted separately for each Port Pin in the register **PPx Port Configuration Register**.

High Power Pad enable

The PP0, PP1, PP2 and PPRF Pins has the possibility to increase the driving capability from 500µA to 4mA each. If one of the Pins needs to drive for example an external LNA the driving capability on this pin can be increased to supply the external LNA directly with the RX_RUN signal. The driving capability can be increased for each PPX pin separately in the register **PPx Port Configuration Register**. The increase of the driving capability should be just enabled if it is necessary due to fast transients if the pin is not loaded, thus possibly increasing the digital noise in the application.

Table 4 Port Pin Output Selection

Selection	Name	Function
0x0h	CLK_OUT	Clock Out Signal
0x1h	RX_RUN	Receiver enabled
0x2h	NINT	Interrupt Signal
0x3h	ANT_EXTSW1	External Antenna Switch Signal
0x4h	ANT_EXTSW2	External Antenna Switch Signal
0x5h	DATA	Receiver Raw Data Slicer Output
0x6h	DATA_MATCHFIL	Receiver Matched Filter Output
0x7h	not used	
0x8h	CH_DATA	Receiver Data Output of Clock Data Recovery
0x9h	CH_STR	Receiver recovered Data Strobe Output of Clock Data Recovery
0xAh	RXD	Receiver line decoded Data output
0xBh	RXSTR	Receiver Data Strobe of line decoded Data
0xCh	TXSTR	Baud Rate Generator Data Clock
0xDh	not used	
0xEh	not used	
0xFh	Tristate	selected Pin will be Tristate

4.8 Interrupt Generation Unit

The Interrupt functionality of the TDA5340 is the most important unit to signal to the host controller that information is available to collect or some information needs to be provided by the host controller. The Interrupt signal (NINT) is provided on one of the PPX port pins (see **Chapter 4.7**).

The Interrupt Generation Unit handles all interrupts generated by the internal building blocks and sets the NINT signal based on the configuration of the Interrupt Mask registers (**Interrupt Mask Register 0**, **Interrupt Mask Register 1** and **Interrupt Mask Register 2**).

The Interrupt Status registers (**Interrupt Status Register 0**, **Interrupt Status Register 1** and **Interrupt Status Register 2**) are set from the Interrupt Generation Unit, depending on which interrupt occurred independent of the Interrupt Mask registers.

The polarity of the interrupt line can be changed in the **PPx Port Configuration Register** register. Please note that during power up and brownout reset, the polarity of NINT signal is always as described in **“Chip Reset” on Page 54**.

A Reset event has the highest priority. It sets all bits in the Status registers to “1” and sets the interrupt signal to “0”. The first interrupt after the Reset event will clear the Status registers and will set the interrupt signal NINT to “1”, even if this interrupt is masked.

The Interrupt Status register is always cleared after read out via SPI (clear by read).

After Reset the duration of the NINT pulse is fixed to 12µs.

4.8.1 Interrupt Sources

An Interrupt can either signal an internal state reached within the TDA5340 or request data which needs to be transmitted or shows the host controller that a data packed is completely received and ready to fetch in the RX FIFO.

System related Interrupts:

- **Reset Interrupt**
  - The Reset Interrupt occurs either by controlling the P_ON line from the host controller or the internal Brownout detector forces a power up reset event. (see **“Chip Reset” on Page 54**)
  - Not maskable
  - All Interrupt Status registers are set to 0xFFh (**Interrupt Status Register 0**, **Interrupt Status Register 1** and **Interrupt Status Register 2**)
- **System Ready Interrupt**
  - The System Ready Interrupt can be used to signal the host controller the successful mode change from Deep Sleep Mode to Sleep Mode. (see **“Power Saving Modes” on Page 24**)
  - Interrupt Mask: bit 1 (IMSYSRDY) in **Interrupt Mask Register 2**
  - Interrupt Status: bit 1 (SYSRDY) in **Interrupt Status Register 2**

Receiver Interrupts:

- **RX FIFO almost full**
  - This interrupt can be used if the expected length of the received data exceeds the FIFO size (288 Bit).
  - Interrupt Mask: bit 0 (IMRXAF) in **Interrupt Mask Register 2**
  - Interrupt Status: bit 0 (RXAF) in **Interrupt Status Register 2**
- **Wake-up Interrupt**
  - The TDA5340 found a match of the configured Wake-up criteria and will change from Self Polling Mode to Run Mode Self Polling.
  - Status register and Mask registers for each configuration A, B, C and D separately
  - Interrupt Mask: bit 0 (IMWUA) and bit 4 (IMWUB) in **Interrupt Mask Register 0** and bit 0 (IMWUC) and bit 4 (IMWUD) in **Interrupt Mask Register 1**

  - Interrupt Status: bit 0 (WUA) and bit 4 (WUB) in **Interrupt Status Register 0** and bit 0 (WUC) and bit 4 (WUD) in **Interrupt Status Register 1**
- **Frame Sync found**
  - The Frame Synchronization Unit found the configured Telegram Start Identifier (TSI) and will start to write the payload data into the RX FIFO.
  - Status register and Mask registers for each configuration A, B, C and D separately
  - Interrupt Mask: bit 1 (IMFSYNCA) and bit 5 (IMFSYNCB) in **Interrupt Mask Register 0** and bit 1 (IMFSYNCA) and bit 5 (IMFSYNCB) in **Interrupt Mask Register 1**
  - Interrupt Status: bit 1 (FSYNCA) and bit 5 (FSYNCB) in **Interrupt Status Register 0** and bit 1 (FSYNCC) and bit 5 (FSYNCD) in **Interrupt Status Register 1**
- **Message ID found**
  - This Interrupt shows the host controller that a valid message identification was found within the payload data.
  - Status register and Mask registers for each configuration A, B, C and D separately
  - Interrupt Mask: bit 2 (IMMIDFA) and bit 6 (IMMIDFB) in **Interrupt Mask Register 0** and bit 2 (IMMIDFC) and bit 6 (IMMIDFD) in **Interrupt Mask Register 1**
  - Interrupt Status: bit 2 (MIDFA) and bit 6 (MIDFB) in **Interrupt Status Register 0** and bit 2 (MIDFC) and bit 6 (MIDFD) in **Interrupt Status Register 1**
- **End of Message Interrupt**
  - The configured End of Message criteria is fulfilled (data length, loss of SYNC or Code Violation).
  - Status register and Mask registers for each configuration A, B, C and D separately
  - Interrupt Mask: bit 3 (IMEOMA) and bit 7 (IMEOMB) in **Interrupt Mask Register 0** and bit 3 (IMEOMC) and bit 7 (IMEOMD) in **Interrupt Mask Register 1**
  - Interrupt Status: bit 3 (EOMA) and bit 7 (EOMB) in **Interrupt Status Register 0** and bit 3 (EOMC) and bit 7 (EOMD) in **Interrupt Status Register 1**

Transmitter Interrupts

- **TX Error Interrupt**
  - The transmitter portion supports a fail save mechanism which can be signaled to the host controller by this interrupt. Trigger effects for this interrupt are: PLL out of lock and PLL calibration failed.
  - Interrupt Mask: bit 7 (IMTXE) in **Interrupt Mask Register 2**
  - Interrupt Status: bit 7 (TXE) in **Interrupt Status Register 2**
- **TX Ready Interrupt**
  - The PLL calibration is finalized and the transmitter is now ready start the transmission.
  - Interrupt Mask: bit 6 (IMTXR) in **Interrupt Mask Register 2**
  - Interrupt Status: bit 6 (TXR) in **Interrupt Status Register 2**
- **TX Strobe Interrupt**
  - In transparent transmit mode the baud rate generator data request strobe can be either signaled with a 50% duty cycle using the TXSTR signal on a port pin or as a interrupt.
  - The maximum achievable baseband data rate is defined by the interrupt duration (12 µs) which is 80 kBit/s.
  - Interrupt Mask: bit 5 (IMTXR) in **Interrupt Mask Register 2**
  - Interrupt Status: bit 5 (TXR) in **Interrupt Status Register 2**
- **TX FIFO Almost Empty Interrupt**
  - For continuous data transmission where the payload data length exceeds the FIFO size the FIFO almost empty interrupt can be used to trigger a refill of the FIFO to keep the transmission ongoing.
  - Interrupt Mask: bit 3 (IMTXAE) in **Interrupt Mask Register 2**
  - Interrupt Status: bit 3 (TXAE) in **Interrupt Status Register 2**
- **TX FIFO Almost Full Interrupt**
  - The FIFO almost full interrupt can be utilized to avoid a congestion of the TX FIFO by the host controller.
  - Interrupt Mask: bit 4 (IMTXAF) in **Interrupt Mask Register 2**
  - Interrupt Status: bit 4 (TXAF) in **Interrupt Status Register 2**

- **TX FIFO Empty Interrupt**
  - With the FIFO empty interrupt the host controller can be informed that the transmission has finished and the TDA5340 is now ready to start a new transmission or go to another main state.
  - Interrupt Mask: bit 2 (IMTXEMPTY) in **Interrupt Mask Register 2**
  - Interrupt Status: bit 2 (TXEMPTY) in **Interrupt Status Register 2**

4.9 Chip Serial Number

Every device contains a unique, pre programmed 32-bit wide serial number. This number can be read out from **Serial Number Register 0**, **Serial Number Register 1**, **Serial Number Register 2** and **Serial Number Register 3** registers via the SPI interface. The TDA5340 always has SN0.6 set to 1 and SN0.5 set to 1.

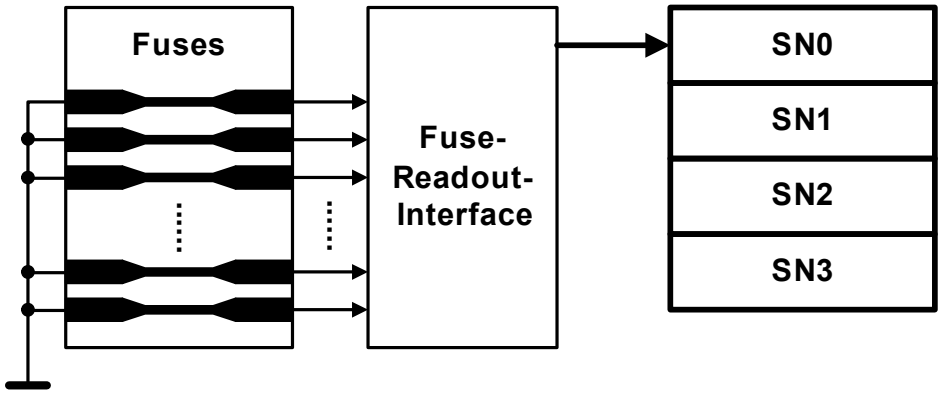
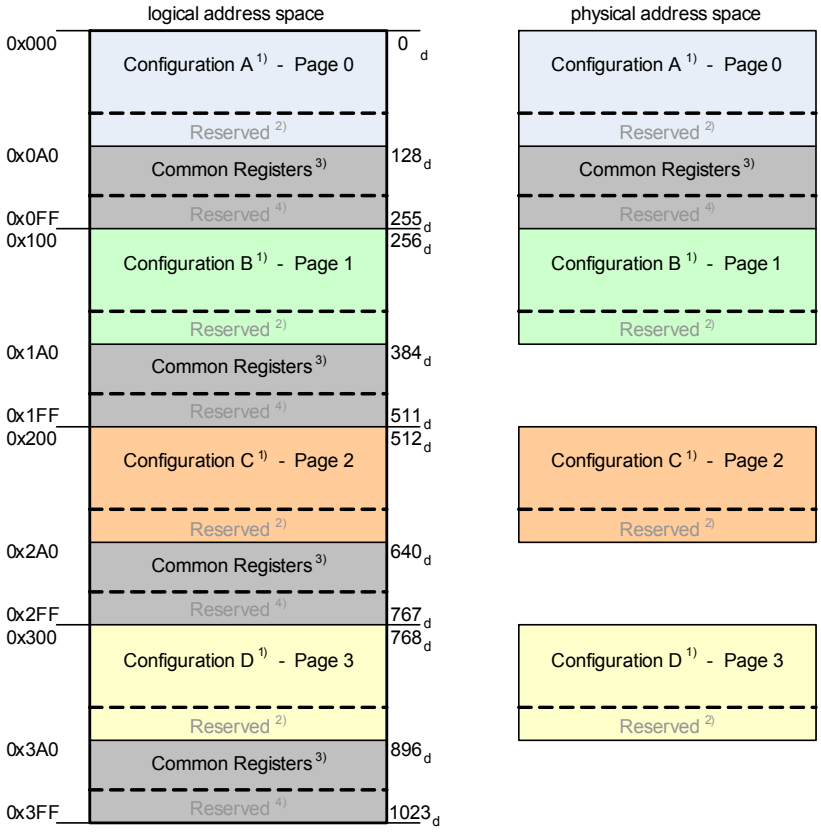


Figure 37 Chip Serial Number

5 Digital Control (SFR Registers)

5.1 SFR Address Paging

An SPI instruction allows a maximum address space of 8 bit. The address space for supporting more than one configuration set is exceeding this 8 bit address room. Therefore a page switch is introduced, which can be applied via the **Special Function Register Page Register** (see Figure 90).



1) Configuration dependent register block (4 protocol specific sets) page switch via SFRPAGE register

2), 4) Reserved – Forbidden area

3) Configuration independent registers (common for all configurations) map (“mirror“) to the same physical address space

Figure 38 SFR Address Paging

5.2 SFR Register List and Detailed SFR Description

The register list is attached in the Appendix at the end of the document.Registers for Configurations B, C and D are equivalent and not shown in detail. All registers with prefix “A_” are related to Configuration A. All these registers are also available for Configuration B, C and D having the prefix “B_”, “C_” and “D_”.

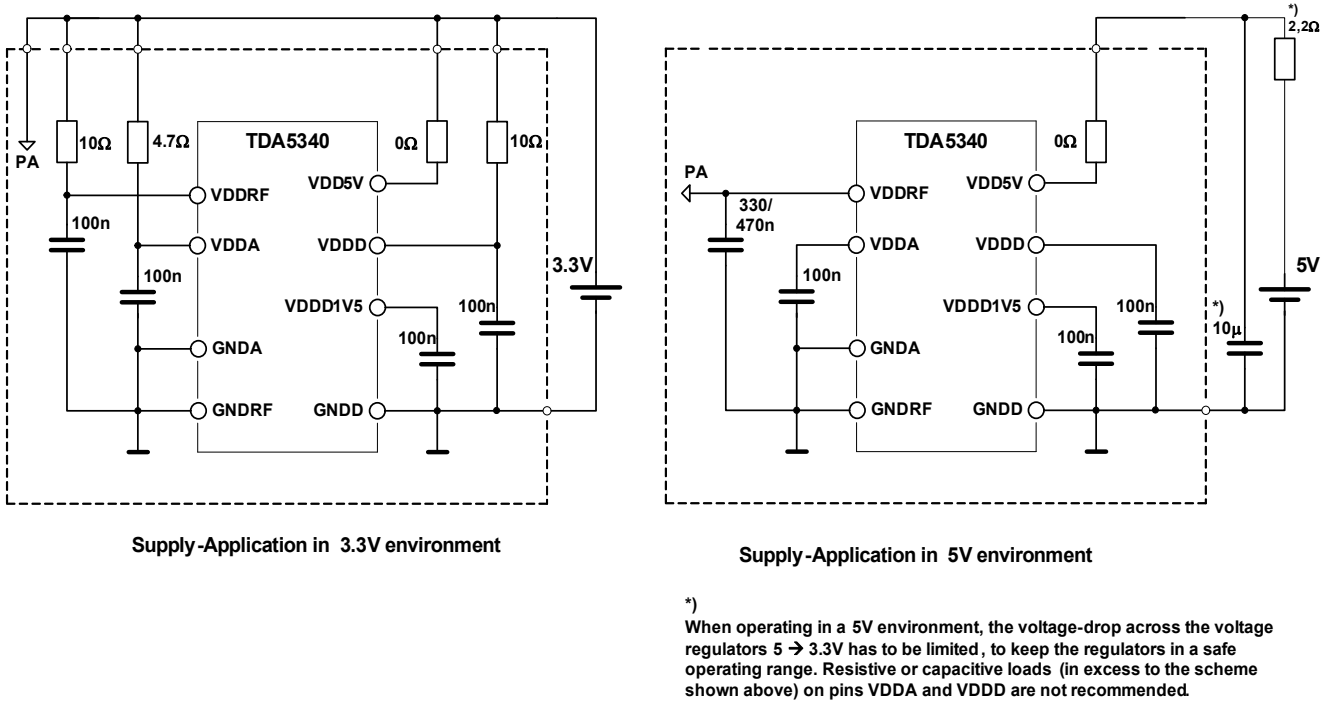
6 Block Description

In this section a detailed description of each building block of the TDA5340 is provided.

6.1 Power Supply Circuitry

The chip may be operated within a 5 Volts or a 3.3 Volts environment.

For operation within a 5 Volts environment (supply voltage range 1), the chip is supplied via the VDD5V pin. In this configuration the digital I/O pads are supplied via VDD5V and the 5 V to 3.3 V voltage regulators supply all internal analog, RF and digital parts (analog/RF section is only active in Run Modes). When operating within a 3.3 Volts environment (supply voltage range 2), the VDD5V, VDDA, VDDD and VDDRF pins must be supplied. The 5 V to 3.3 V voltage regulators are inactive in this configuration. The internal digital core is supplied by an internal 3.3 V to 1.5 V regulator. The regulators for the digital section are controlled by the signal at P_ON (Power On) pin. A low signal at P_ON disables all regulators and set the IC in Power Down Mode. A low to high transition at P_ON enables the regulators for the digital section and initiates a power on reset. The regulator for the analog section is controlled by the Master Control Unit and is active only when the RF section is active. To provide data integrity within the digital units, a brownout detector monitors the digital supply. In case a voltage drop of VDDD below approximately 2.45 V is detected a RESET will be initiated. A typical power supply application for a 3.3 Volts and a 5 Volts environment is shown in the figure below.



Supply-Application in 3.3V environment

Supply-Application in 5V environment

*)
When operating in a 5V environment, the voltage-drop across the voltage regulators 5 → 3.3V has to be limited, to keep the regulators in a safe operating range. Resistive or capacitive loads (in excess to the scheme shown above) on pins VDDA and VDDD are not recommended.

Figure 39 3.3 Volts and 5 Volts Applications

6.2 Chip Reset

Power down and power on are controlled by the P_ON pin. A LOW at this pin keeps the IC in Power Down Mode. All voltage regulators and the internal biasing are switched off. A high transition at P_ON pin activates the appropriate voltage regulators and the internal biasing of the chip. A power up reset is generated at the same time.

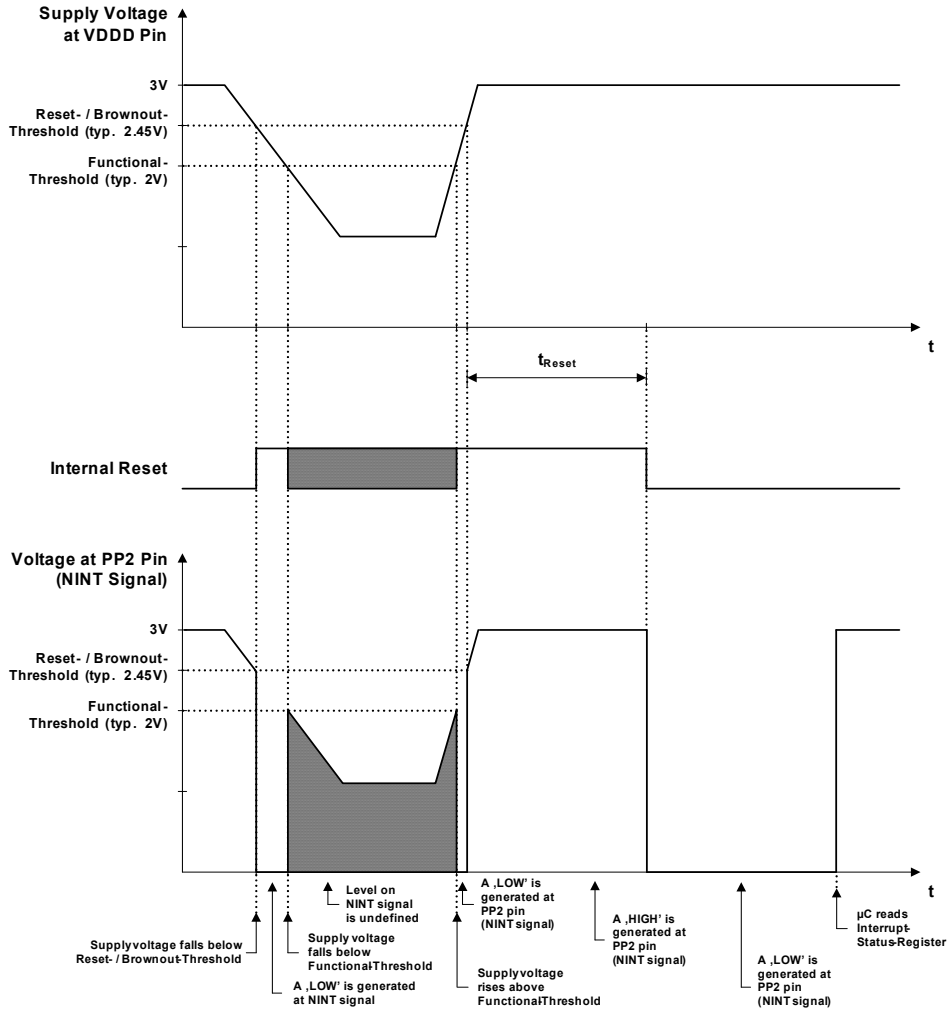


Figure 40 Reset Behavior

Brownout Event

A second source that can trigger a reset is a brownout event. This brownout reset can be enabled and disabled in the **Chip Mode Control Register** by controlling the EN3V3DET bit. Whenever the integrated brownout detector measures a voltage drop below the brownout threshold (approx. 2.45V) on the digital supply, the integrity of the stored data and configuration can no longer be guaranteed; thus a reset is generated. While the supply voltage stays between the brownout and the functional threshold of the chip, the NINT signal is forced to low. When the supply voltage drops below the functional threshold, the levels of all digital output pins are undefined. When the supply voltage raises above the brownout threshold, the IC generates a high pulse at NINT and remains in the reset state for the duration of the reset time. When the IC leaves the reset state, the Interrupt Status registers are set to 0xFF and the NINT signal is forced to low. Now, the IC starts operation in the SLEEP Mode, ready to receive commands via the SPI interface. The NINT signal will go high, when one of the Interrupt Status registers is read for the first time.

6.3 RF / IF Receiver

The receiver path uses a double down conversion super-heterodyne/low-IF architecture, where the first IF frequency is located at 10.7 MHz and the second IF frequency at 274 kHz. For the first IF frequency an adjustment-free image frequency rejection is realized by means of two I/Q-mixers followed by a second order passive polyphase filter centered at 10.7 MHz (PPF). The I/Q-oscillator signals for the first down conversion are delivered

from the PLL synthesizer. The frequency selection in the first IF domain is done by an external CER filter. For low-cost applications, this ceramic filter can be substituted by a simple LC Pi-filter or completely by-passed using the receiver as a single down conversion low-IF scheme with 274 kHz IF frequency. The down conversion to the second IF frequency is done by means of two high-side injected I/Q-mixers together with an on-chip third order bandpass polyphase filter (PPF2 + BPF). The I/Q-oscillator signals for the second down conversion are directly derived by division of two from the crystal oscillator frequency. The bandwidth of the bandpass filter (BPF) can be selected from 50 kHz to 300 kHz in 5 steps (see BPFBWSEL bit group in **IF1 Register**). For a frequency offset of 150 kHz to 120 kHz, the AFC (Automatic Frequency Control) function is mandatory. Activated AFC option might require a longer preamble sequence in the receive data stream.

The receiver enable signal (RX_RUN) can be offered at each of the port pins to control external components. Whenever the receiver is active, the RX_RUN output signal is active. Active high or active low is configured via **PPx Port Configuration Register** .

The frequency relations are calculated with the following formulas:

$$f_{IF1} = 10.7MHz$$
$$f_{IF2} = \frac{f_{IF1}}{39}$$
$$f_{crystal} = f_{IF2} \cdot 80$$
$$f_{LO2} = \frac{f_{crystal}}{2}$$
$$f_{LO1} = f_{crystal} \cdot Dividerfactor \quad (1)$$

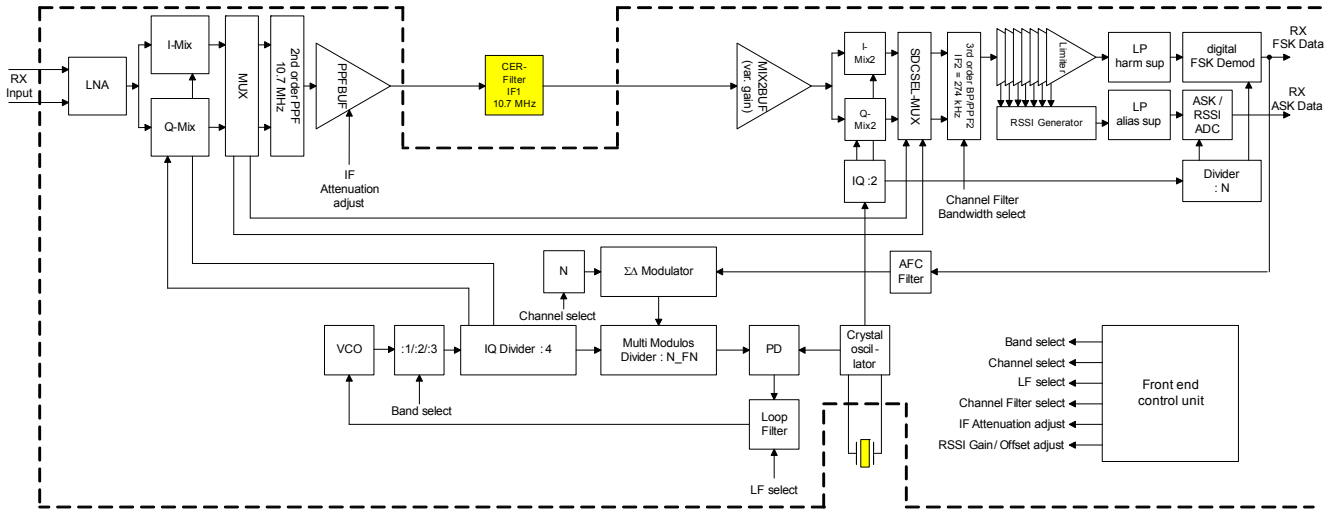


Figure 41 Block Diagram RF Receiver Section

6.3.1 Low Noise Amplifier (LNA)

The LNA of the TDA5340 has a differential input where each input can be used as a single ended input. Both Inputs of the LNA can be grounded separately via internal switches. The LNA optimum input impedance for Noise figure and power matching is set to one single impedance point. The frontend matching can be done either differential or single ended.

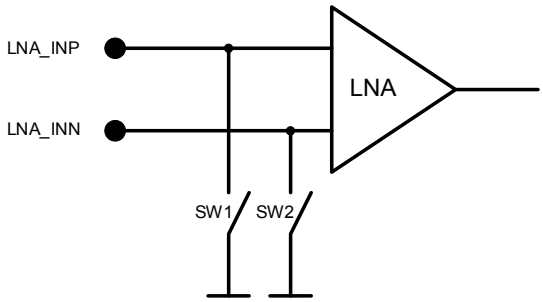


Figure 42 LNA Block Diagram

The independent switchable LNA inputs gives the possibility to match each input to different frequency bands, for example LNA_INP input to 434MHz and LNA_INN to 868MHz. The position of the switches can be defined in all four configurations in the **Antenna Switch Configuration Register** independently.

The optimum NF of the frontend is reached if a differential matching network is applied to the LNA input.

6.3.2 Single/Double Down Conversion

The immunity against strong interference frequencies (so called blockers) is determined by the available filter bandwidth, the filter order and the 3rd order intercept point of the front end stages. For Single-Channel applications with moderate requirements to the selectivity the performance of the on-chip 3rd order bandpass polyphase filter might be sufficient. In this case no external filters are necessary and a single down conversion architecture can be used, which converts the input signal frequency directly to the 2nd IF frequency of 274 kHz.

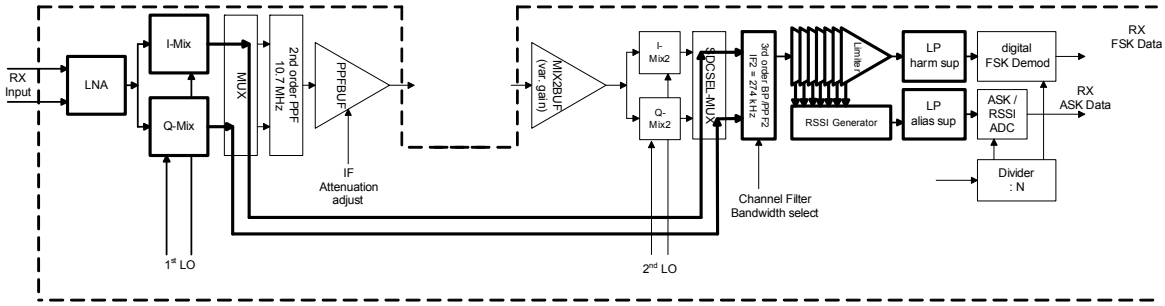


Figure 43 Single Down Conversion (no external filters required)

For Multi-Channel applications or systems which demand higher selectivity the double down conversion scheme with an external CER filter can be selected. The order of such ceramic filter is in a range of 3, so the selectivity is drastically improved and a good channel separation should be guaranteed.

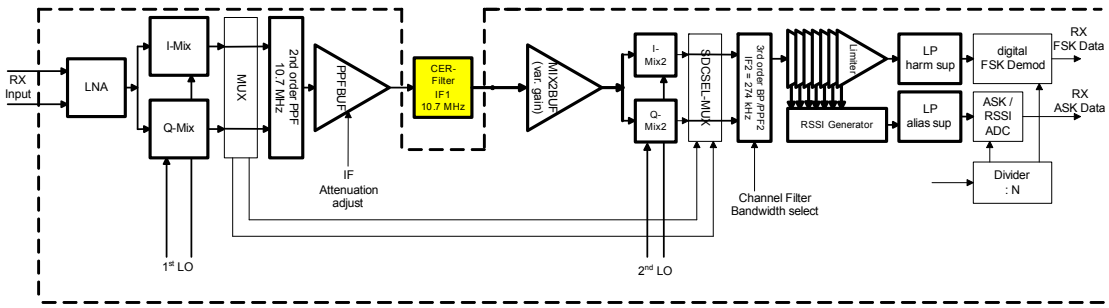


Figure 44 Double Down Conversion

The selection of Single or Double Down Conversion can be done with the SDCSEL bit in the **IF1 Register**. Of course the frequency of the local oscillator needs to be adopted to generate the wanted IF frequency.

6.3.3 Band Pass Filter (BPF)

The fully BPF bandwidth can be programmed via the BPFBWSEL bits in the **IF1 Register** in each configuration. The available bandwidths are:

- 50 kHz
- 80 kHz
- 125 kHz
- 200 kHz
- 300 kHz

The bandpass filter follows the subsequent formula:

$$f_{center} = \sqrt{f_{corner,LOW} \cdot f_{corner,HIGH}} \tag{2}$$

Therefore asymmetric corner frequencies can be observed.

It has to be noted that the analog system bandwidth is not only defined by the BPF alone. The analog system bandwidth is typically lower than the BPF filter bandwidth due to cascading blocks with filter behavior.

The typical analog system bandwidth for different bandpass filter settings are shown in the table below:

Table 5 Analog system bandwidth

BPFBWSEL	BPF bandwidth	BW_{ana}
000_B	50 kHz	50 kHz
001_B	80 kHz	80 kHz
010_B	125 kHz	120 kHz
011_B	200 kHz	180 kHz
100_B	300 kHz	230 kHz

6.4 Transmitter

A highly efficient Class C/E Power amplifier with output levels of +14 dBm combined with a Gaussian Filter for GFSK and amplitude ramping functions for shaped ASK is implemented. A high resolution power adjustment can be done to trim the output power for system power savings. The power adjustment can be also utilized to trim out the production spread of matching components and the PA stage itself. The Sigma Delta PLL is used to generate the necessary local oscillator frequency. The data can be either shifted out of a on-chip transmit FIFO or directly provided on an input pin.

6.4.1 Power Amplifier

The Class C/E Power Amplifier has single ended output (RF_OUT) and is divided into several selectable clusters of amplifier stages (31 stages) which can be combined to achieve the wanted output power in combination with the best efficiency. The achievable output power and efficiency is highly influenced by the load impedance of the matching network.

Power Level Programing

The high power level (POWHIGH) and low power level (POWLOW) of the transmitter can be defined in the **TX Power Configuration Register 0** and **TX Power Configuration Register 1** for each of the four configurations. Of course for FSK modulation schema only the (POWHIGH) level will be used. The resulting output power is a

combination of the matching network impedance, selected power amplifier stages and Duty Cycle Control selection.

The output impedance of the PA depends on the number of PA stages used. The external antenna matching must be done for the impedance related to the highest number of used PA stages, or in other words, for the use-case of highest RF output power. If the desired output power is +13 dBm for instance, the antenna should be matched for the case of all the 31 PA Stages active. Supposed the matching network have been set up for the PA impedance bound to +13 dBm output power (all 31 PA Stages active), it is reasonable to expect some degree of mismatch and efficiency loss by operation in +5 dBm RF power mode.

It has to be kept in mind, by matching to the highest number of PA stages the best efficiency of the PA is reached but also the capability of trimming to higher output power level is lost.

All available PA stages are driven by so called preamplifiers. The current consumption of the preamplifieres is a function of the selected RF frequency and the number of activated stages. The more stages are activated and the higher the frequency the higher the overall current consumption of the preamplifiers.

6.4.2 Duty Cycle Control

The control of Duty Cycle leads to control of the averaged RF output power (by changing the conductive angle of the power amplifier) and contributes to further reduction of the current consumption. It is worth to be noted, that the decreasing conduction angle values lead to decrease of power consumption, but due to the short and high-amplitude current pulses the level of RF harmonics (on n*fcarrier frequencies) tends to rise.

Proper measures (filtering) must be taken to maintain harmonics level rejection.

The duty cycle can be programmed from 25% to 37.5% in 5 steps in the **TX RF Configuration Register**. The higher the selected duty cycle the higher the current consumption and output power.

6.5 Crystal Oscillator and Clock Divider

The crystal oscillator is a Pierce type oscillator. An automatic amplitude regulation circuitry allows the oscillator to operate with minimum current consumption. In SLEEP Mode, where the current consumption should be as low as possible, the load capacitor must be small and the frequency is slightly de tuned, therefore all internal trim capacitors are disconnected. The internal capacitors are controlled by the crystal oscillator calibration **XTAL Coarse Calibration Register** and **XTAL Fine Calibration Register**. With a binary weighted capacitor array the necessary load capacitor can be selected.

Whenever a XTALCALx register value is updated, the selected trim capacitors are automatically connected to the crystal so that the frequency is precise at the specified value. Step size is 1 pF. The SFR control bit XTALHPMS in the **Clock Divider Register 2** can be used to activate the High Precision Mode also during SLEEP Mode.

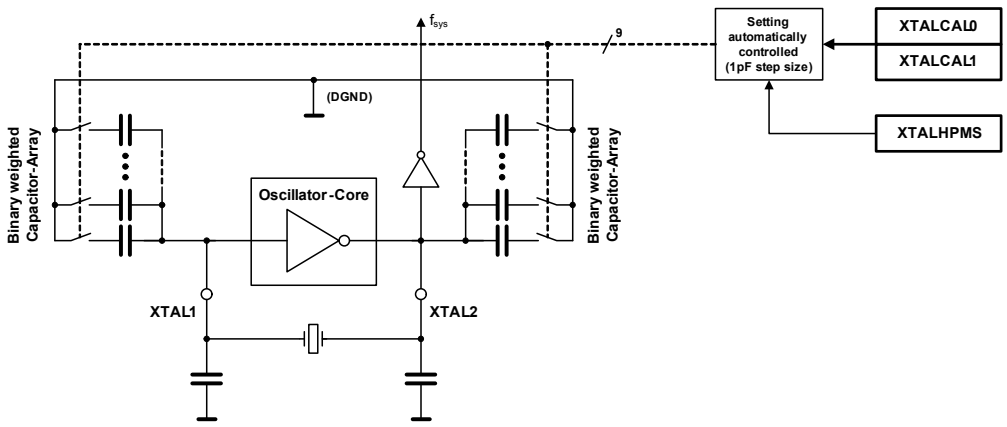


Figure 45 Crystal Oscillator

External Clock Generation Unit

A built in programmable frequency divider can be used to generate an external clock source out of the crystal reference. The 20 bit wide division factor is stored in the **Clock Divider Register 0**, **Clock Divider Register 1** and **Clock Divider Register 2**. The minimum value of the programmable frequency divider is 2. This programmable divider is followed by an additional divider by 2, which generates a 50% duty cycle of the CLK_OUT signal. So the maximum frequency at the CLK_OUT signal is the crystal frequency divided by 4. The minimum CLK_OUT frequency is the crystal frequency divided by 2^{21}.

To save power, this programmable clock signal can be disabled by the SFR control bit CLKOUTEN in **Clock Divider Register 2**. In this case the external clock signal is set to low.

The resulting CLK_OUT frequency can be calculated by:

$$f_{CLKOUT} = \frac{f_{SYS}}{2 \cdot divisionfactor} \quad (3)$$

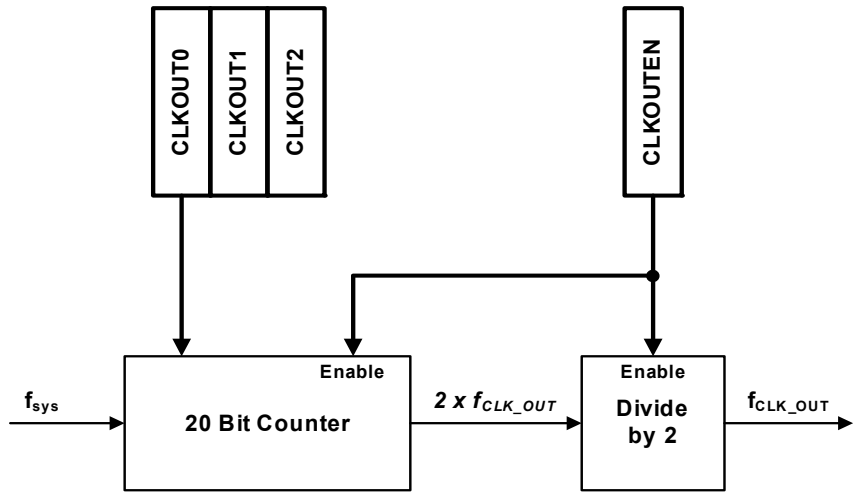


Figure 46 External Clock Generation Unit

The maximum CLK_OUT frequency is limited by the driver capability of the PPx pin and depends on the external load connected to this pin. Please be aware that large loads and/or high clock frequencies at this pin may act as an interfere and reduces performance.

After Reset the PPx pin is activated and the division factor is initialized to 11 (equals f_{CLK_OUT} = 998 kHz).

A clock output frequency higher than 1 MHz is not recommended.

For high sensitivity applications, the use of the external clock generation unit is not recommended.

6.6 Polling Timer

The Polling Timer is used to define the ON and OFF timings of the receiver in Self Polling Mode (SPM) and has three sub-modules.

The **Reference Timer** is used to divide the state machine clock (fsys/64) into the slower clock required for the SPM timers. (see **Self Polling Mode Reference Timer Register**)

The **On-Off Timer** and the **Active Idle Period Timer** are used to generate the polling signal. The entire unit is controlled by the SPM Finite State Machine (FSM). The TDA5340 is able to handle up to four different sets of configurations automatically. However, the examples and figures in this subsection only show up to two configuration sets for the sake of clarity. Related registers are:

- On Time for each configuration: **Self Polling Mode On Time Config A Register 0**, **Self Polling Mode On Time Config A Register 1**, **Self Polling Mode On Time Config B Register 0**, **Self Polling Mode On Time Config B Register 1**, **Self Polling Mode On Time Config C Register 0**, **Self Polling Mode On Time Config C Register 1**, **Self Polling Mode On Time Config D Register 0** and **Self Polling Mode On Time Config D Register 1**
- Off Time: **Self Polling Mode Off Time Register 0** and **Self Polling Mode Off Time Register 1**
- Idle periods: **Self Polling Mode Idle Periods Register**
- Active periods: **Self Polling Mode Control Register**

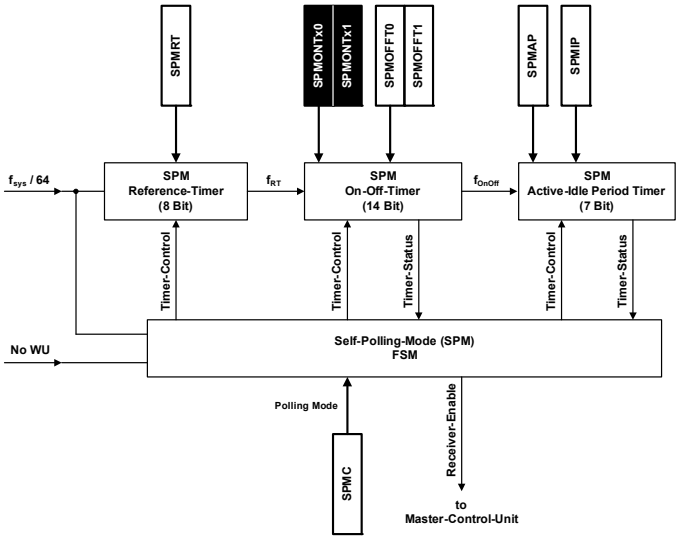


Figure 47 Polling Timer Unit

Calculation of On time:

The On time must be long enough to ensure proper detection of a specified wake-up criterion. Therefore the On time depends on the wake-up pattern, and the wake-up criterion. It has to include transmitter data rate tolerances.

T_{ON} also must include the relevant start-up times. In case of the first channel after T_{OFF}, this is the Receiver Start-Up Time. In case of following channels (RF Receiver is already on, there is only a change of the channel or the configuration), e.g. if Configuration B is used, this is the Channel Hop Latency Time. In addition, it has to be considered that some data bits are required for synchronization and internal latency, see **“RUNIN, Synchronization Search Time and Inter-Frame Time” on Page 103**.

Calculation of Off time:

The longer the Off time, the lower the average power consumption in Self Polling Mode. On the other hand, the Off time has to be short enough that no transmitted wake-up pattern is missed. Therefore the Off time depends mainly on the duration of the expected wake-up pattern.

Active Idle Period Selection

This functionality is used to deactivate some polling periods.

Normally, polling starts again after the $T_{MasterPeriod}$. With this Active Idle Period selection some of the polling periods can be deactivated, independent from the Polling Mode. The active and the idle sequence is set with the **Self Polling Mode Control Register** and the **Self Polling Mode Idle Periods Register** . The values of these registers determine the factor M and N.

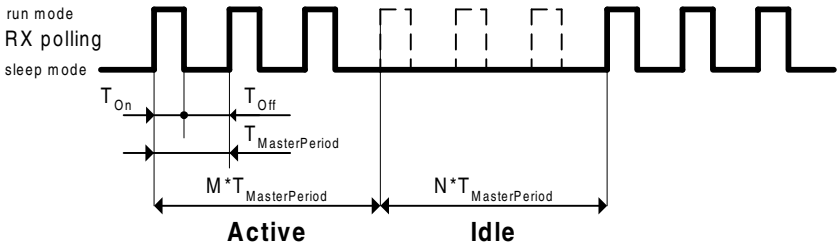


Figure 48 Active Idle Period

6.7 Time Out Timer (TOTIM)

The Time Out Timer unit is used to bring the receiver from Run Mode Self Polling back to Self Polling Mode. The TOTIM can be divided into three main subgroups:

- Timer which are independent of data rate synchronization (**Timeout Timer Register 0** and **Timeout Timer Register 1**)
- Timer are only active if data rate synchronization is lost (**SYNC Timeout Timer Register**)
- Timer are only active if data rate synchronization is present (**TSI Timeout Timer Register** and **EOM Timeout Timer Register**)

The timer will be deactivated by setting the corresponding registers to zero all other values in this registers will activate the timer.

All TOTIM's are initialized after a Wake-up event and a End of Message (EOM) event. The common time base is defined as follows:

$$Timebase = \frac{64 \cdot 512}{f_{SYS}} \tag{4}$$

Independent TOTIM

This timer will be started and will bring back the receiver to Self Polling Mode after expiring without any interaction from internal signal processing.

Data Rate Synchronization Lost (TOTIM_SYNC)

The TOTIM_SYNC is only enabled if the synchronization (SYNC) to the programmed data rate is lost. If the SYNC is found again the timer will be halted at the present value and will continue from this time after loss of SYNC. The SYNC signal will be provided from the Clock and Data Recovery see **Chapter 6.13.13**.

TOTIM with SYNC

There are two timers, TOTIM_TSI (see **TSI Timeout Timer Register**) which is only active between Wake-up and potential Telegram Start Identifier (TSI) and TOTIM_EOM is activated (if enabled) after detection of TSI. This timers are mainly used to avoid receiver activity related to potential interferers which may have the same modulation and data rate as the expected data frame. The register value of TOTIM_EOM has to be multiplied by two and then multiplied with the time base to get the programmed time period. (for details see **EOM Timeout Timer Register**)

In **Figure 49** a detailed description of all TOTIM's can be found.

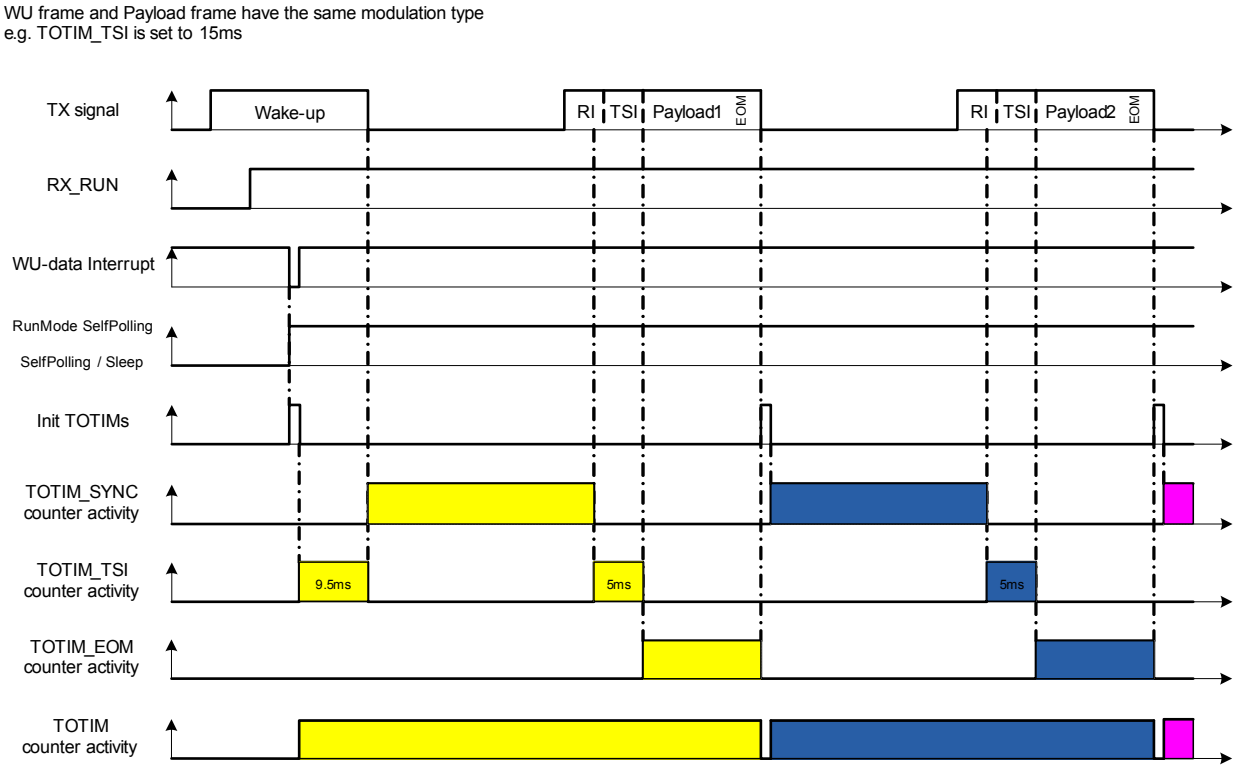


Figure 49 TOTIM Behavior

External Forced TOTIM

Normally the TOTIM event is generated by the TDA5340 itself but in some circumstances the host controller must overrule the internal logic and bring back the receiver to Self Polling Mode immediately. This can be done by a SPI access to **External Processing Command Register** by setting the EXTTOTIM bit to high.

6.8 Baud Rate Generator

The Baud Rate Generator is used to provide a time base for the transmitter baseband. The generated baud rate strobe can be used by the TX FIFO Mode which builds the actual baseband data for the modulation or as an output data request signal in TX Transparent Mode.

The Data Rate frequency can be calculated as follows:

$$DataRate\left[\frac{Bit}{s}\right] = \frac{f_{sys}}{(TXBDRDIV + 1)\cdot 2} \quad (5)$$

Where TXBDRDIV can be set in the **TX Baudrate Divider Register 0** and **TX Baudrate Divider Register 1**. It has to be mentioned that the chip rate is double of the Bit rate if bi-phase encoding is used for NRZ coding the chip rate equals the bit rate.

The data request strobe of the baud rate generation unit can be provided on one of the PPx pins by selecting the TXSTR signal (see **“General Purpose Output Pins” on Page 49**). The transmit baseband data should be provided to the TDA5340 as described in the chapter **“TX Transparent Mode” on Page 40**.

The request strobe can be also signaled to the host controller via a TX Strobe interrupt request of the Interrupt generation unit. (see **“Transmitter Interrupts” on Page 51**) It has to be stated at this point that the maximum

achievable baseband data rate is defined by the interrupt duration (12 µs) which limits this functionality to a data rate of 80 kChips/s.

6.9 Sigma-Delta Fractional-N PLL

The Sigma-Delta Fractional-N PLL is fully integrated on chip. The Voltage Controlled Oscillator (VCO) with on-chip LC-tank runs at approximately 3.6 GHz and is first divided with a band select divider by 1, 2 or 3 (see BANDSEL in **PLL MMD Integer Value Register Channel 1**). Divide by 1 selects the 915 MHz and 868 MHz band, divide by 2 selects the 434 MHz band and divide by 3 selects the 315 MHz band.

In receive mode the I/Q-divider provides an orthogonal local oscillator signal for the first image reject mixer with the necessary high accuracy. In transmit mode a simple divider generates the local oscillator frequency for the power amplifier stage.

The multi-modulus divider determines the channel selection and is controlled by a 3rd order Sigma-Delta Modulator (SDM). A type IV phase detector, a charge pump with programmable current and an on-chip loop filter closes the phase locked loop.

The following formula defines the frequency of the local oscillator for reception.

$$f_{RF} \pm f_{IF} = f_{XOSC} * \left(\left(INT < 5:0 > + \frac{FRAC < 20:0 > + 0.5}{2^{21} - 0.5} \right) \right) \quad (6)$$

The following formula defines the frequency of the local oscillator for transmission.

$$f_{RF} = f_{XOSC} * \left(\left(INT < 5:0 > + \frac{FRAC < 20:0 > + 0.5}{2^{21} - 0.5} \right) \right) \quad (7)$$

Where the INT represents the integer value of the divider which can be programmed in the **PLL MMD Integer Value Register Channel 1** . The FRAC value respectively is the fraction value of the divider and can be configured in the **PLL Fractional Division Ratio Register 0 Channel 1**, **PLL Fractional Division Ratio Register 1 Channel 1** and **PLL Fractional Division Ratio Register 2 Channel 1**.

The same register set exists for each of the 4 channels within the 4 configurations (e.g. 16 times).

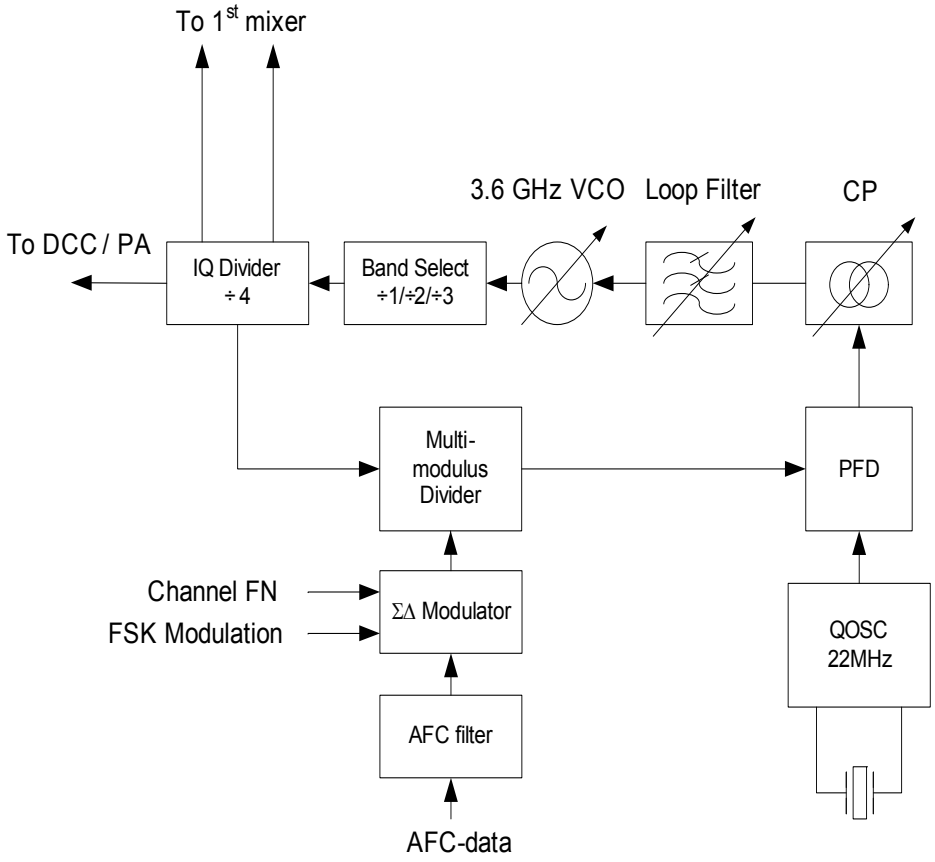


Figure 50 Synthesizer Block Diagram

The following picture shows the PLL frequency range together with the reception and transmission frequency ranges.

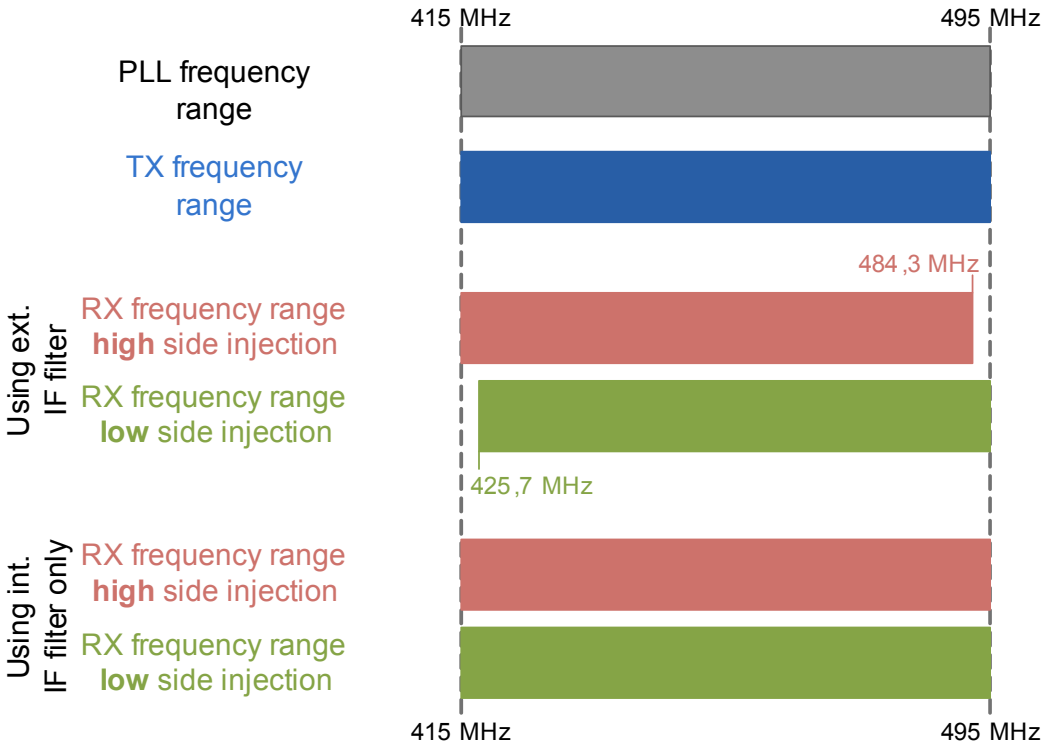


Figure 51 TRX frequency range

6.10 Analog to Digital Converter (ADC)

In front of the AD converter there is a multiplexer so that also temperature and VDDD can be measured.

The default value of the ADC-MUX is RSSI (**ADC Input Selection Register**: 000 for RSSI; 001 for Temperature; 010 for VDDD/2).

After switching ADC-MUX to a value other than RSSI in SLEEP Mode, the internal references are activated and this ADC start-up lasts 100µs. So after this ADC start-up time the readout measurements may begin. The chip stays in this mode until reconfiguration of register ADCINSEL to setting RSSI. However, it is recommended to measure temperature during SLEEP mode (This is also valid for VDDD).

Readout of the 10-bit ADC has to be done via **ADC Result High Byte Register** and **ADC Result Low Byte Register**.

Typical the ADC refresh rate is 3.7 µs. Time duration between two ADC readouts has to be at least 3.7 µs, so this is already achieved due to the maximum SPI rate (16 bit for SPI command and address last 8µs at an SPI rate of 2MBit/s). The EOC bit (end of conversion) in **ADC Result Low Byte Register** indicates a successful conversion additionally. Repetition of the readout measurement for several times is for averaging purpose.

The input voltage of the ADC is in the range of 1 to 2 V. Therefore VDDD/2 (= 1.65 V typical) is used to monitor VDDD.

6.11 Temperature Sensor

The temperature Sensor of the TDA5340 may be utilized to compensate crystal and gain variations due to temperature influences.

The used temperature sensor is generating a voltage proportional to absolute temperature. This voltage is converted into a digital value by the ADC. The function TEMP = function(ADC-value) can be idealized by a straight line.

The accuracy of the temperature sensor is mainly influenced by the used calibration routine. In general it has to be stated that a calibration routine is necessary to achieve an acceptable temperature accuracy. The achievable temperature accuracies are listed below.

- Uncalibrated: The accuracy is low at +/- 23 °C
- 1 point calibration (can be done at any temperature point): A accuracy of +/- 4.5 °C can be achieved.

Temperature Measurement procedure

- Set chip to SLEEP mode
- Set register **ADC Input Selection Register** to “Temperature”
- Wait for at least 100 µs for 1st readout
- Readout ADC via **ADC Result High Byte Register** and **ADC Result Low Byte Register**
- Repeat the readout process 10-times and create average value

Measuring temperature is recommended in Sleep Mode and Transmit Mode only and is fully functional in this modes.

It is not recommended to measure Temperature during Run Mode Slave or Self Polling Mode, as the RF input signal cannot be processed in that case and other side effects will occur.

Temperature or VDDD measurement itself would be working OK in the operating modes Run Mode Slave or Self Polling Mode, but changing the ADC input source to Temperature (or VDDD) does not open the connection to the subsequent Peak Memory filter in the signal chain in these modes.

So during a temperature measurement the PMF gets loaded and the unloading is performed with the selected PMF Decay time, which is several bits usually. After 2 tau (2 * Decay time) the signal went down by 87% (this seems to be OK as first proposal).

This additional "wait" time needs to be kept in mind, before being able to receive data again in Run Mode Slave or Self Polling Mode.

6.12 Transmitter Baseband

The provided transmit modulation schemes of the TDA5340 are:

- OOK or (100% ASK)
- shaped OOK
- ASK
- shaped ASK
- FSK
- GFSK

The transmit modulation schema can be selected in the **TX Configuration Regsiter** by the ASKFSK, ASKSLOPEN and GFSKEN bits. The used modulation schema highly influences the occupied bandwidth of the transmit spectrum and the robustness of the communication link.

ASK has advantages in current consumption of the transmitter but is also more susceptible to interfere signals.

FSK has higher robustness against interferer and also higher sensitivity on the receiver side but this has to be treated with a higher supply current consumption in transmit mode.

In the following description of the modulations we do not differentiate between ASK and OOK because the baseband functionality for both modulation schemes is the same.

6.12.1 ASK/OOK Sloping (shaped ASK/OOK)

The ASK sloping feature is utilized to reduce the spectrum density out of the used channel and can be enabled by using the ASKSLOPEN bit in the **TX Configuration Regsiter** . The sloping is done between the low power level and the high power level (see **“Power Level Programing” on Page 58**) by switching on the internal power

amplifier stages sequentially. The ramping slope can be defined in the ASLDIV in the registers **TX Data Shaping Configuration Register 0** and **TX Data Shaping Configuration Register 2** following the equation below.

$$ASLDIV = \left(\frac{f_{SYS} \cdot SlopeWidth[\%]}{DataRate \cdot (POWHIGH - POWLOW)} \right) - 1 \quad (8)$$

Where f_{SYS} equals to the System frequency which is 21.948717 MHz. The Slope Width is the sloping time given in percentage of the bit duration of the Data Rate. The POWHIGH and POWLOW values are the two power levels used in the ASK modulation. For the Slope width calculation keep in mind, that with BiPhase encoding one Bit consists of two Chips.

The dithering feature is a further mechanism to reduce discrete frequencies within the shaped ASK/OOK frequency spectrum and can be enabled in the **TX Power Configuration Register 1** selected using the SLDITHWD in the **TX Power Configuration Register 0** . The maximum dithering width is defined in following formula.

$$DitherValue = \frac{2^{\text{SLDITHWD}}}{2}$$
$$DitherValue \leq \frac{\text{ASLDIV}}{2} \quad (9)$$

The recommended dithering value is the most closest DitherValue to the ASLDIV/2

6.12.2 FSK and GFSK Modulation

The FSK modulation is done with the Sigma Delta PLL by changing the division factor of the divider. This technique allows a very precise adjustment of the frequency deviation. The wanted frequency deviation can be selected by using a scaling (FDEVSCALE) and a division factor (FDEV) in **TX Frequency Deviation Register**. The calculation of the different register can be found in the equation below.

$$\pm f_{deviation}[Hz] = FDEF \cdot \frac{f_{SYS}}{2^{21}} \cdot 190 \cdot 2^{(FDEVSCALE-6)} \quad (10)$$

As shown in the equation the FDEFSCALE defines the resolution and the maximum achievable frequency deviation. This means the higher the wanted frequency deviation the lower the provided resolution.

Gaussian Filter

With the Gaussian Filter the baseband data can be shaped to reduce the occupied bandwidth of the RF signal.

The functionality can be enabled with the GFSKEN bit in the **TX Configuration Regsiter** register. The resulting gaussian filter division factor GFDIV (**TX Data Shaping Configuration Register 1** and **TX Data Shaping**

Configuration Register 2) out of the required BT can be seen in the equation below, where the division factor is equation is different for bi-phase encoded data and NRZ coded data.

$$GFDIV_{BiPhase} = \frac{f_{SYS}}{DataRate \cdot 2 \cdot 16 \cdot BT} - \tag{11}$$

$$GFDIV_{NRZ} = \frac{f_{SYS}}{DataRate \cdot 16 \cdot BT} - 1 \tag{12}$$

6.13 Receiver Baseband

The IC comprises two separate demodulators for ASK and FSK (see modulation type (MT) bit in register **Channel Configuration Register**).

After combining FSK and ASK data path, a sampling rate adaptation follows to meet an output oversampling between 8 and 16 samples per chip. Finally, an oversampling of 8 samples per chip can be achieved using a fractional sample rate converter (SRC) with linear interpolation

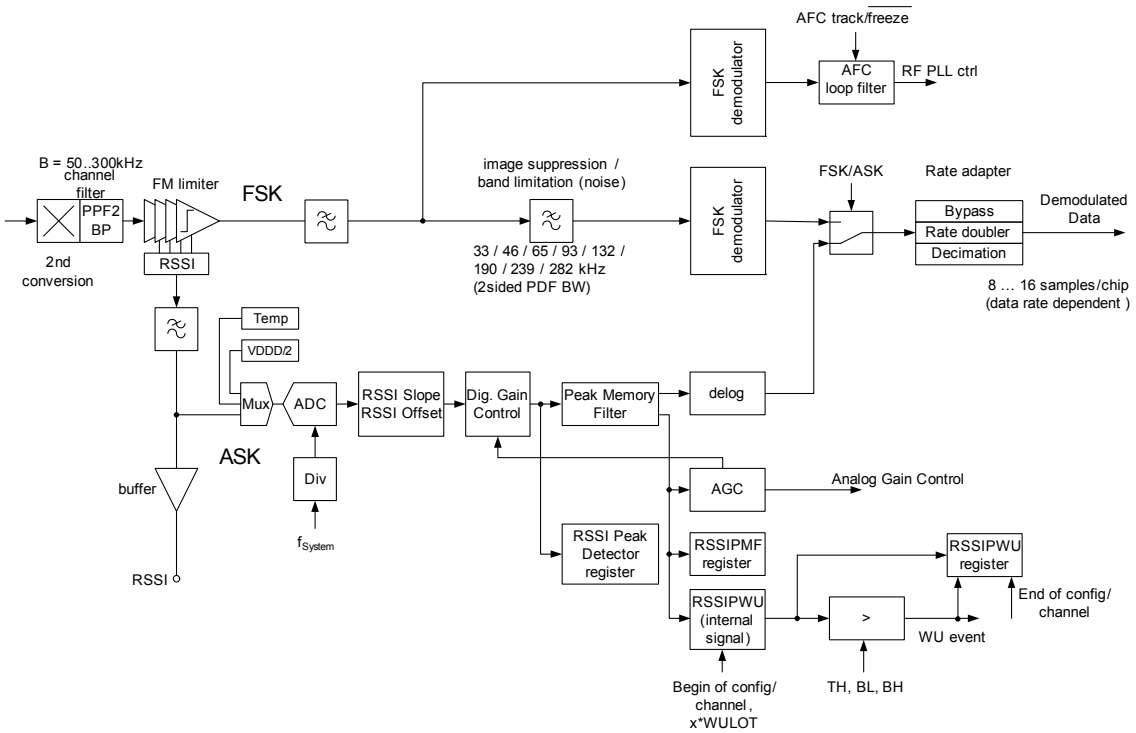


Figure 52 Functional Block Diagram ASK/FSK Demodulator

6.13.1 ASK Demodulator

The RSSI generator delivers a DC signal proportional to the applied input power at a logarithmic scale (dBm) and is also used as an ASK demodulator. Via a programmable anti-aliasing filter (AAFFCSEL bit in **Digital Receiver Configuration Register** register) this signal is converted to the digital domain by means of a 10-bit ADC. For the AM demodulation a signal proportional to the linear power is required. Therefore a conversion from logarithmic scale to linear scale is necessary. This is done in the digital domain by a nonlinear filter together with an exponential function. The analog RSSI signal after the anti-aliasing filter is available at the RSSI pin via a buffer

amplifier. To enable this buffer the SFR control bit RSSIMONEN in register **RSSI Configuration Register** must be set. The anti-aliasing filter can be by-passed for visualization on the RSSI pin (see AAFBYP control bit).

6.13.2 Delog Block & Peak-Memory Filter

The Received Signal Strength Indicator‘s (RSSI) output provides a signal in the logarithmic domain which is converted by the 10 Bit ADC into the digital domain. The Subsequent signal processing is in the linear domain. Therefore it is necessary to delogarithmize the signal, which is accomplished in the „DELOG“ block.

Delogarithmization is a highly nonlinear function which can be seen in **Figure 53**. The limited resolution of the DELOG output causes input signals to be mapped to the minimum possible output level. Therefore signal normalization is needed to shift the signal up into a region of the RSSI curve where a proper input-output mapping in the DELOG block is possible. This signal normalization is achieved by using a **Peak-Memory Filter** (PMF) before de logarithmic (see **Figure 52**).

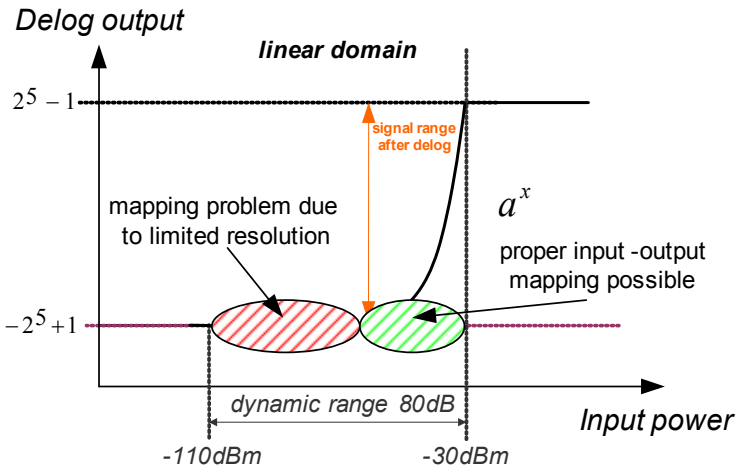


Figure 53 DELOG Function

Basically the task of the PMF is to follow the peaks of the input RSSI signal. To achieve fast settling and to reduce distortion introduced by the signal normalization, the PMF should be setup with a fast attack (PMFUP) coefficient and a slow decay coefficient (PMFDN) (see **Peak Memory Filter Up-Down Factor Register**).

The output from the PMF is used to normalize the digital RSSI signal and is finally shifted and delogarithmized.

In general it can be stated that the faster the Up coefficient and the slower the decay coefficient the better sensitivity performance values can be achieved. But it has also to be stated that the slower the decay coefficient the receiver will have more “memory” to interferes and the interframe time with high power differences will be limited.

The following equation shows the relationship between attack / decay timings and the actual register values.

$$C_{up} = Round\left(\frac{\ln\left(\frac{t_{attack}[Bit]}{DataRate[kBit/s]} \cdot 274\right)}{\ln(2)}\right)$$

$$PMFUP = C_{up} - 1$$

$$C_{down} = \left[Round\left(\frac{\ln\left(\frac{t_{decay}[Bit]}{DataRate[kBit/s]} \cdot 274\right)}{\ln(2)}\right)\right] - C_{up}$$

$$PMFDN = C_{down} - 2 \quad (13)$$

A good starting point is to use an attack time (t_{attack}) of 0.2 bit and a decay time (t_{decay}) of 4 bit.

6.13.3 FSK Demodulator

The limiter output signal, which has a constant amplitude over a wide range of the input signal, feeds the FSK demodulator. There is a configurable lowpass filter in front of the FSK demodulation to suppress the down conversion image (FSK Pre-Demodulation Filter, PDF). This is realized as a 3rd order digital filter. The sampling rate after FSK demodulation is fixed and independent from the target data rate.

6.13.4 Automatic Frequency Control (AFC)

In front of the image suppression filter a second FSK demodulator is used to derive the control signal for the Automatic Frequency Control Unit, which is actually the DC value of the FSK demodulated signal. This makes the AFC loop independent from signal path filtering and allow so a wider frequency capture range of the AFC. The derivation of the AFC control signal is preferably done during the DC free preamble and is then frozen for the rest of the datagram.

Since the digital FSK demodulator determines the exact frequency offset between the received input frequency and the programmed input center frequency of the receiver, this offset can be corrected through the sigma delta control of the PLL. As shown in **Figure 52**, for AFC purposes a parallel demodulation path is implemented. This path does not contain the digital low pass filter (PDF, Pre-Demodulation Filter). The entire IF bandwidth, filtered by the analog bandpass filter only, is processed by the AFC demodulator.

There are two options for the active time of the AFC loop:

- always on
- active for a programmable time relative to a signal identification event (several options can be programmed in SFR).

Start Conditions (AFCSTART in AFC Start/Freeze Configuration Register)

- OFF (AFC Deactivated)
- Direct ON (AFC always on)
- Start on RSSI event
  - AFC will start if RSSI level is above threshold which can be selected in **RSSI Wake-Up Threshold for Channel 1 Register**
- Start on Signal recognition event
  - AFC will start if the Signal recognition condition is fulfilled see **“Data Filter and Signal Detection” on Page 82**programmed

Freeze Conditions (AFCFREEZE in AFC Start/Freeze Configuration Register)

- Stay ON (AFC is always searching)
- Freeze on RSSI event + Delay
  - If the RSSI level is above the configured RSSI threshold in **RSSI Wake-Up Threshold for Channel 1 Register** the AFC will stay at the found frequency after a programmable delay (**AFC/AGC/ADR Freeze Delay Register**)
- Freeze on Signal Recognition event + Delay
  - The AFC will be frozen if the Signal recognition condition is fulfilled and the programmable delay (**AFC/AGC/ADR Freeze Delay Register**) is expired.
- Freeze on Symbol Synchronization (SYNC) + Delay
  - After loss of SYNC the programmable delay time (**AFC/AGC/ADR Freeze Delay Register**) is waited and the AFC frozen
- The TDA5340 provides also the functionality that the host controller can freeze the AFC by the AFCMANF bit in the **External Processing Command Register** register.

Unfreeze Conditions (AFCFREEZE in AFC Start/Freeze Configuration Register)

- no unfreeze
  - once the AFC is frozen on a frequency the receiver will use the discovered frequency offset until the receiver leaves the active mode (RMSP or RMS) or the bit AFC restart at channel change and config change (AFCRESATCC) in **AFC Start/Freeze Configuration Register** is enabled
- Unfreeze on NOT RSSI event
  - If the RSSI level goes below the configured RSSI threshold in **RSSI Wake-Up Threshold for Channel 1 Register** the AFC will unfreeze. A unfreeze will be generated only if the RSSI level is above the threshold and changes below the threshold (negative edge detection)
- Unfreeze on NOT Signal Recognition event
  - The AFC will be unfrozen if the Signal recognition condition is not fulfilled anymore. An unfreeze will be generated only if the Signal recognition condition is fulfilled and changes to loss of Signal recognition (negative edge detection)
- Unfreeze on NOT Symbol Synchronization (SYNC)
  - After loss of SYNC the AFC will be started again. The unfreeze happens only if a SYNC was generated and a transition to loss of SYNC has occurred (negative edge detection)
- The TDA5340 provides also the functionality that the host controller can unfreeze the AFC by the AFCMANUF bit in the **External Processing Command Register**.

The programming of the active time is especially necessary in case the expected frame structure contains a gap (noise) between wake-up and payload in order to avoid the AFC from drifting.

AFC works both for FSK and ASK. In the latter case the AFC loop can be forced to regulates only during ASK data = high. (see AFCBLASK bit in **AFC Start/Freeze Configuration Register**)

For safety reasons it is recommended to use for the same condition for freeze and unfreeze. If the unfreeze condition is on a later stage in the signal processing chain the possibility definitely exists that this event does not occur. For example if the freeze condition is set to RSSI and the unfreeze condition is set to SYNC it may happen that an interferer is freezing the AFC on a wrong frequency and the unfreeze condition of SYNC is never reached.

The maximum frequency offset generated by the AFC can be limited by means of the **AFC Limit Configuration Register** . This limit can be used to avoid the AFC from drifting in the presence of interferers.

The bandwidth (and thus settling time) of the loop is programmed by means of the integrator gain coefficients K1 and K2 (**AFC Integrators Gain Coefficients Register 0** and **AFC Integrators Gain Coefficients Register 1**).

K1 mainly determines the bandwidth. K2 influences the dynamics/damping (overshoot) - smaller K2 means smaller overshoot, but slower dynamics. The bandwidth of the AFC loop is approximately 1.8*K1 (when K1 = K2).

To avoid residual FM, limiting the AFC BW to 1/20 ~ 1/40 of the bit rate is suggested, therefore K1 must be set to approximately 1/40 ~ 1/70 of the bit rate. For most applications K2 can be set equal to K1 (overshoot is then <15%).

When very fast settling is necessary K1 and K2 can be increased up to bit rate/10, however, in this case approximately 1dB sensitivity loss has to be expected due to the AFC counteracting the input FSK signal.

6.13.5 Digital Automatic Gain Control (AGC)

Automatic Gain Control (AGC) is necessary mainly because of the limited dynamic range of the on-chip bandpass filter (BPF). The dynamic range reduces to less than 60dB in case of minimum BPF bandwidth.

AGC is used to cover the following cases:

- ASK demodulation at large input signals
- RSSI reading at large input signals
- Improve IIP3 performance in either FSK or ASK mode

The IF buffer (PPFBUF, see **"Block Diagram RF Receiver Section" on Page 56**) can be fine tuned "manually" by means of 4 bits thus optimizing the overall gain to the application (attenuation of 0dB to -12dB by means of IFATT0 to IFATT15). This buffer allows the production spread of external components to be trimmed or reducing the gain in case of external LNA.

The gain of the 2nd IF path is set to three different values by means of an AGC algorithm. Depending on whether the receiver is used in single down conversion or in double down conversion mode the gain control in the 2nd IF path is either after the 2nd poly-phase network or in front of the 2nd mixer.

The AGC action is illustrated in the RSSI curve below:

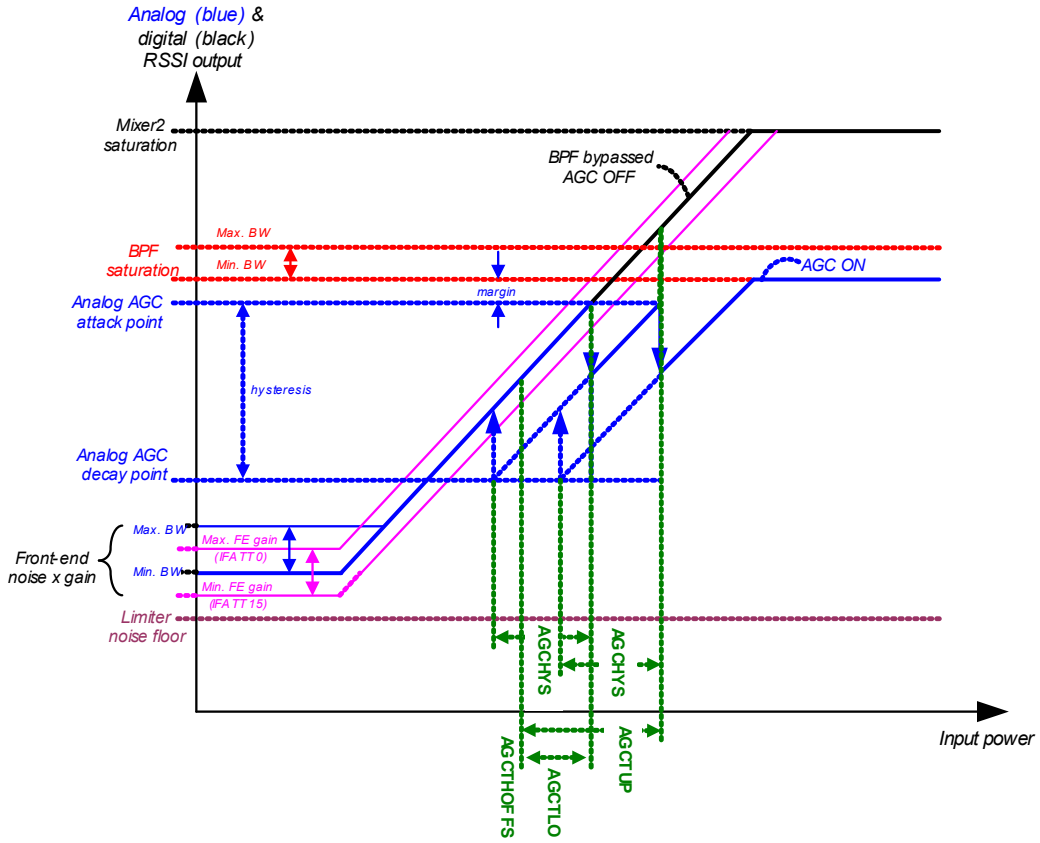


Figure 54 Analog RSSI output curve with AGC action ON (blue) vs. OFF (black)

Digital RSSI, AGC and Delog:

In order to match the analog RSSI signal to the digital RSSI output a correction is necessary. It adds an offset (**RSSI Offset Register**) and modifies the slope (**RSSI Slope Register**) such that standardized AGC levels and an appropriate DELOG table can be applied.

Upon entering the AGC unit the digital RSSI signal is passed through a Peak Memory Filter (PMF). This filter has programmable up and down integration time constants (PMFUP, PMFDN in **Peak Memory Filter Up-Down Factor Register**) to set attack respectively decay time. The integration time for decay time must be significantly longer than the attack time in order to avoid the AGC interfering with the ASK modulation.

The integrator is followed by two digital Schmitt triggers with programmable thresholds (AGCTLO; AGCTUP in **AGC Threshold Register**) - one Schmitt trigger for each of the two attack thresholds (two digital AGC switching points). The hysteresis of the Schmitt triggers is programmable (AGCHYS in **AGC Configuration Register 0**) and sets the decay threshold. The Schmitt triggers control both the analog gain as well as the corresponding (programmable) digital gain correction (AGCDGC in register **AGC Configuration Register 0**).

The difference (“error”) signal in the PMF is actually a normalized version of the modulation. This signal is then used as input for the DELOG table.

The following condition of the thresholds needs to be fulfilled:

$$AGCOFFS + 1.6 \cdot AGCTLO < 102.4$$
$$AGCOFFS + 25.6 + 1.6 \cdot AGCTUP < 102.4 \quad (14)$$

AGC threshold programming

The SFR description for the AGC thresholds are in dBs. The first value to set is the AGC threshold offset (AGCTHOFFS) in register **AGC Configuration Register 1**.

This value is the offset relative to 0 input (no noise, no signal), which for the default setting of gain, and assuming typical insertion loss of matching network and ceramic filter, can be extrapolated to be approximately -143dBm.

In this case the default setting of the AGCTHOFFS of 63.9dB corresponds to an input power of approximately -79dBm (= -143dBm + 63.9dB).

The low (digital) AGC threshold is then -79 + 12.8dB (default AGCTLO) = -66dBm and the upper (digital) AGC threshold is -79 + 25.6 (default AGCTUP) = -53dBm.

Therefore a margin of about 6dB is indicated before a degradation of the linearity of the 2nd IF can be observed when using the 50kHz BPF or even about 16dB when using the 300kHz BPF.

The input power level at which the AGC switches back to maximum gain is -66dBm - 21.3dB (default AGCHYS) = -87dBm. This provides enough margin against the minimum sensitivity.

When AGC is activated, RSSI is untrimmed, IFATT <= 5.6dB and the same RSSI offset should be applied for all bandpass filter settings, then the settings in **Table 6** can be applied, where a small reduction of the RSSI input range can be observed.

Table 6 AGC Setting 1

AGC Threshold Hysteresis = 21.3 dB					
AGC Digital RSSI Gain Correction = 15.5 dB					
BPF	**RSSI Offset Compensation[1)]**	**AGC Threshold Offset**	**AGC Threshold Low**	**AGC Threshold Up**	**RSSI Input Range Reduction**
300 kHz	32	63.9 dB	8	4	5 dB
200 kHz	32	63.9 dB	6	2	5 dB
125 kHz	32	63.9 dB	5	0	5 dB
80 kHz	32	51.1 dB	11	6	2.8 dB
50 kHz	32	51.1 dB	9	5	0 dB

1) This value needs to be used for calculating the register values

For the full RSSI input range, the values in **Table 7** can be applied.

Table 7 AGC Setting 2

AGC Threshold Hysteresis = 21.3 dB				
AGC Digital RSSI Gain Correction = 15.5 dB				
BPF	**RSSI Offset Compensation[1)]**	**AGC Threshold Offset**	**AGC Threshold Low**	**AGC Threshold Up**
300 kHz	-18	63.9 dB	5	1
200 kHz	-18	51.1 dB	11	7
125 kHz	-18	51.1 dB	10	5
80 kHz	4	51.1 dB	9	5
50 kHz	32	51.1 dB	9	5

1) This value needs to be used for calculating the register values

Attack and Decay coefficients of Peak memory filter (PMF-UP & PMF-DOWN):

The settling time of the loop is determined by means of the integrator gain coefficients PMFUP and PMFDN in **Peak Memory Filter Up-Down Factor Register**, which need to be calculated from the wanted attack and decay times.

The ADC is running at a fixed sampling frequency of 274kHz. Therefore the integrator is integrating with PMFUP*274k per second, i.e. time constant is 1/(PMFUP*274k). The attack times are typically 16 times faster than the decay times.

Typical calculation of the coefficients by means of an example:

PMFUP = 2^-round (ln(AttTime / BitRate * 274kHz) / ln(2))

PMFDN = 2^-round (ln(DecTime / BitRate * 274kHz) / ln(2)) / PMFUP

where AttTime, DecTime = attack, decay time in number of bits

Example:

BitRate = 2kbps

AttTime = 0.1 bits

=> PMFUP = 2^-round (ln(0.1bit/2kbps*274kHz)/ln(2)) = 2^-round(3.8) = 2^-4

DecTime = 2 bits

=> PMFDN = 2^-round (ln(2bit/2kbps*274kHz)/ln(2))/PMFUP = 2^-round(8.1)/2^-4 = 2^-4

Note: In case of ASK with large modulation index the attack time (PMFUP) can be up to a factor 2 slower due to the fact that the ASK signal has a duty cycle of 50% - during the ASK low duration the integrator is actually slightly discharged due to the decay set by PMFDN.

The AGC start and freeze times are programmable. The same conditions can be used as in the corresponding AFC section above. They will however, be programmed in separate SFR registers.

6.13.6 RSSI Peak Detector

The IC possesses several digital RSSI peak level detectors. The RSSI level is averaged over 4 samples before it is fed to any of the peak detectors. This prevents the evaluated peak values to be dominated by single noise peaks. To be able to measure the RSSI it is very important to select the RSSI signal as input signal for the A/D converter in the **ADC Input Selection Register**.

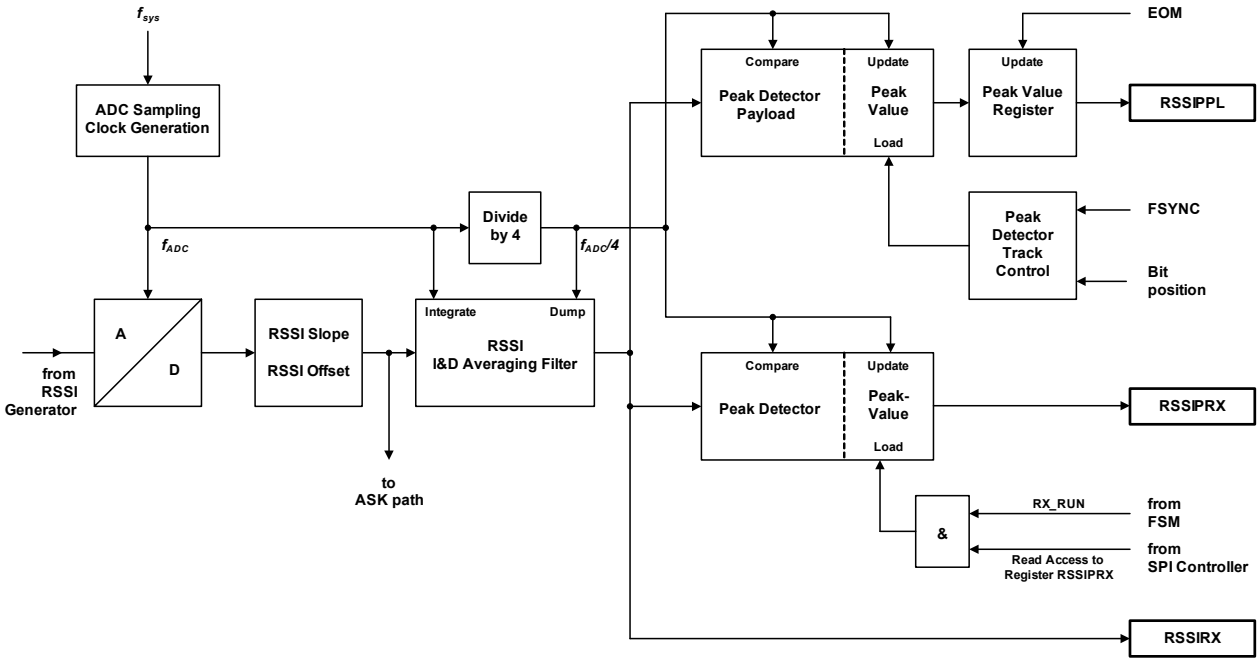


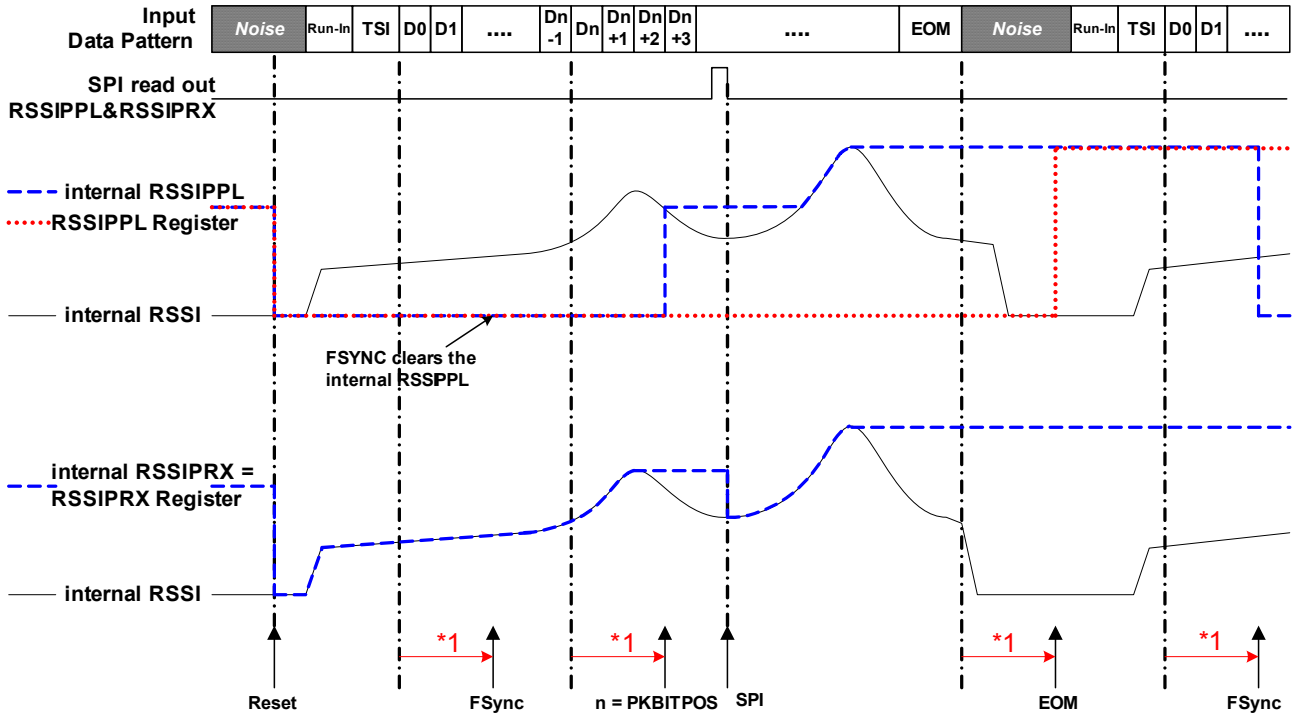
Figure 55 Peak Detector Unit

Peak Detector Payload is used to measure the input signal power of a received and accepted data telegram. It is read via **RSSI Payload Peak Detector Readout Register**. Observation of the RSSI signal starts at the detection of a TSI (FSYNC) and ends with the detection of EOM. The internal RSSIPPL value is cleared after FSYNC. The evaluated RSSI peak level RSSIPPL is transferred to the RSSIPPL register at EOM. Starting the observation of the RSSI level can be delayed by a selectable number of data bits and is controlled by the **RSSI Peak Detector Bit Position Register**. A latency in the generation of FSYNC and EOM of approx. 2..3 bits in relation to the contents of the Peak Detector must be considered. Within the boundaries described, the register RSSIPPL always contains the peak value of the last completely received data telegram. The register RSSIPPL is reset to 0 at power up reset only.

Peak Detector is used to measure RSSI independent of a data transfer and to digitally trim RSSI. It is read via **RSSI Peak Detector Readout Register**. Observation of the RSSI signal is active whenever the RX_RUN signal is high. The **RSSI Peak Detector Readout Register** is refreshed and the Peak Detector is reset after every read access to **RSSI Peak Detector Readout Register**. It may be required to read **RSSI Peak Detector Readout Register** twice to obtain the required result. This is because, for example, during a trim procedure in which the input signal power is reduced, after reading **RSSI Peak Detector Readout Register**, the peak detector will still hold the higher RSSI level. After reading **RSSI Peak Detector Readout Register** the lower RSSI level is loaded into the Peak Detector and can be read by reading **RSSI Peak Detector Readout Register** again. When the RX_RUN signal is inactive, a read access has no influence to the peak detector value. The register RSSIPRX is reset to 0 at power up reset.

Peak Detector Wake-Up **Wakeup Peak Detector Readout Register** is used to measure the input signal power during Wake-Up search. The internal signal RSSIPWU gets initialized to 0 at start of the first observation time window at the beginning of each configuration/channel. The peak value of this signal is tracked during Wake-Up search. In case of a Wake-Up, the actual peak value is written in the **Wakeup Peak Detector Readout Register**.

Even in case no Wake-Up occurred, actual peak value is written in the **Wakeup Peak Detector Readout Register** at the end of the actual configuration/channel of the Self Polling period. So if no Wake-Up occurred, then the **Wakeup Peak Detector Readout Register** contains the peak value of the last configuration/channel of the Self Polling period, even in a Multi-Configuration/Multi-Channel setup. This functionality can be used to track RSSI during unsuccessful Wake-Up search due to no input signal or due to blocking RSSI detection. For further details please refer to **"Wake-Up Generator" on Page 90**.



*1 Computation Delay due to filtering and signal calculation.

Figure 56 Peak Detector Behavior

Recommended Digital RSSI Trimming Procedure

- Download configuration file (Run Mode Slave; **RSSI Slope Register**, **RSSI Offset Register** set to default, i.e. RSSISLOPE=1, RSSIOFFS=0)
- Turn off AGC (AGCSTART=0) and set gain to AGCGAIN=0
- Apply PIN1 = -85 dBm RF input signal read **RSSI Peak Detector Readout Register** eleven times (minimum 10 ms in-between readings), use average of last ten readings (always), store as RSSIM1
- Apply PIN2 = -65 dBm RF input signal read **RSSI Peak Detector Readout Register** eleven times (minimum 10 ms in-between readings), use average of last ten readings (always), store as RSSIM2Calculate measured RSSI slope SLOPEM=(RSSIM2-RSSIM1)/(PIN2-PIN1)
- Adjust **RSSI Slope Register** for required RSSI slope SLOPER as follows: RSSISLOPE=SLOPER/SLOPEM
- Adjust **RSSI Offset Register** for required value RSSIR2 at PIN2 as follows: RSSIOFFS=(RSSIR2-RSSIM2)+(SLOPEM-SLOPER)*PIN2
- The new values for RSSISLOPE and RSSIOFFS have to be added to the configuration!

Notes:

1. The upper RF input level must stay well below the saturation level of the receiver (see **Chapter 6.13.5**)
2. The lower RF input level must stay well above the noise level of the receiver
3. If IF Attenuation is trimmed, this has to be done before trimming of RSSI

4. If RSSI needs to be trimmed in a higher input power range the AGCGAIN must be set accordingly

6.13.7 Antenna Diversity based on RSSI (ADR)

The ADR is a build in state machine within the TDA5340 which can select one of two antennas by using the RSSI as decision criteria. The selection of the antenna can be done either by using an external antenna switch or by utilize the build in RX/TX switch as an antenna switch between RFINN and RFINP. This would mean that the two differnetial inputs of the LNA are used as sepparate single ended LNA inputs for both antennas.

Due to the fact that the ADR is using the RSSI as decision base, the functionality is mainly useful for constant envelope modulation schemes (i.e. FSK or GFSK).

ADR principle

The antenna selection behavior of the ADR is divided into 3 different areas of the RSSI curve and can be adjusted by several thresholds and hysteresis registers.

- Search
- Switch
- Stay

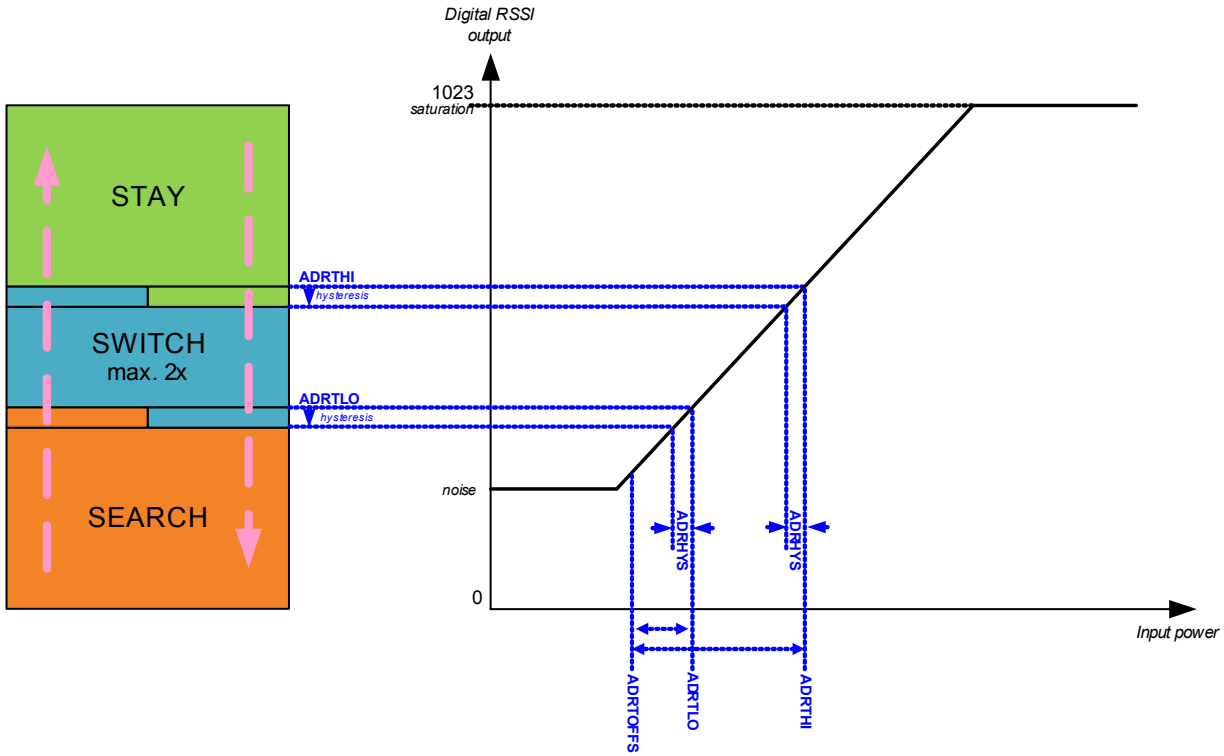


Figure 57 ADR principle

ADR Search State

If the actual RSSI voltage on both antenna inputs is below the **ADR Threshold Register 1** the internal state machine will switch between both antennas periodically. The period can be defined by the **ADR Timeout Configuration Register 0** and **ADR Timeout Configuration Register 2**.

ADR Switch State

The state machine will enter the switch state if the RSSI level of one of the antennas is above the lower threshold level (**ADR Threshold Register 1**) and below the higher threshold level. After entering the switch state the state machine changes to the other antenna and will check the signal level strength. The receiver will now remain on the antenna with the higher RSSI value. In the switch state the state machine starts the switch timer which can be programed in the **ADR Timeout Configuration Register 1** and **ADR Timeout Configuration Register 2**. This timer is used to periodically change to the opposite antenna. This mechanism enables the detection of a stronger signal on the other antenna within the switch state.

If the Signal strength on both antennas will fall below the lower threshold minus the hysteresis the receiver will go back to the search mode.

ADR Stay State

To enter the stay state the actual signal strength of one antenna needs to be above the higher threshold level (**ADR Threshold Register 1**). After reaching the stay state the receiver will remain on this antenna as long as the RSSI is above the higher threshold level minus the hysteresis.

If the signal level falls below the lower bound the state machine will change the antenna and moves to the switch state.

ADR Calculations

The lower threshold can be calculated as follows:

$$ADRTH_{LOW}[dBm] = Base[dBm] + ADRTLO \cdot 3.2 + Offset[dBm] \tag{15}$$

For calculation of the threshold high the equation below can be used:

$$ADRTH_{HIGH}[dBm] = Base[dBm] + 12.5[dBm] + ADRTHI \cdot 3.2 + Offset[dBm] \tag{16}$$

Where the Base is usually taken with -140 dBm and the ADRTLO, ADRTHI and Offset can be selected via SFR registers.

The timers of the search and switch state are using a common time base which can be calculated as follows:

$$t_{ADR\_Base} = \frac{320}{f_{sys}} = \frac{320}{21.948717 \cdot 10^6\, Hz} = 14.579\,\mu s \tag{17}$$

The equation below defines the timer for the search state:

$$t_{search} = t_{ADR\_Base} \cdot \mathrm{ADRTSEARCH} \tag{18}$$

The timer of the switch state can be calculated using the equation below:

As a general rule of thumb the search time should be 2 times the used baseband data rate.

$$t_{switch} = t_{ADR\_Base} \cdot \mathrm{ADRTSWITCH} \tag{19}$$

The ADRTSWITCH and ADRTSEARCH parameters can be selected in the **ADR Timeout Configuration Register 0**, **ADR Timeout Configuration Register 1** and **ADR Timeout Configuration Register 2**

6.13.7.1 ADR activation

There are two options for the active time of the ADR state machine:

- 1. always on
- 2. active for a programmable time relative to a signal identification event (several options can be programmed in SFR).

Start Conditions (ADR START in ADR Start/Freeze Configuration Register)

- OFF (ADR Deactivated)
- Direct ON (ADR always on)
- Start on RSSI event --> not recommended
  - ADR will start if RSSI level is above threshold which can be selected in **RSSI Wake-Up Threshold for Channel 1 Register**
- Start on Signal recognition event
  - ADR will start if the Signal recognition condition is fulfilled see **“Data Filter and Signal Detection” on Page 82**

Freeze Conditions (ADRFREEZE in ADR Start/Freeze Configuration Register)

- Stay ON (ADR is always searching)
- Freeze on RSSI event + Delay
  - If the RSSI level is above the configured RSSI threshold in **RSSI Wake-Up Threshold for Channel 1 Register** the ADR will stay at the found antenna after a programmable delay (**AFC/AGC/ADR Freeze Delay Register**)
- Freeze on Signal Recognition event + Delay
  - The ADR will be frozen if the Signal recognition condition is fulfilled and the programmable delay (**AFC/AGC/ADR Freeze Delay Register**) is expired.
- Freeze on Symbol Synchronization (SYNC) + Delay
  - After loss of SYNC the programmable delay time (**AFC/AGC/ADR Freeze Delay Register**) is waited and the ADR is frozen
- The TDA5340 provides also the functionality that the host controller can freeze the ADR by the ADRMANF bit in the **External Processing Command Register** register.

Unfreeze Conditions (ADRFREEZE in ADR Start/Freeze Configuration Register)

- no unfreeze
  - once the ADR is frozen on a frequency the receiver will use the discovered antenna until the receiver leaves the active mode (RMSP or RMS)
- Unfreeze on NOT RSSI event
  - If the RSSI level goes below the configured RSSI threshold in **RSSI Wake-Up Threshold for Channel 1 Register** the ADR will unfreeze. An unfreeze will be generated only if the RSSI level is above the threshold and changes below the threshold (negative edge detection)
- Unfreeze on NOT Signal Recognition event
  - The ADR will be unfrozen if the Signal recognition condition is not fulfilled anymore. An unfreeze will be generated only if the Signal recognition condition is fulfilled and changes to loss of Signal recognition (negative edge detection)
- Unfreeze on NOT Symbol Synchronization (SYNC)
  - After loss of SYNC the ADR will be started again. The unfreeze happens only if a SYNC was generated and a transition to loss of SYNC has occurred (negative edge detection)
- The TDA5340 provides also the functionality that the host controller can unfreeze the ADR by the ADRMANUF bit in the **External Processing Command Register**.

The programming of the active time is especially necessary in case the expected frame structure contains a gap (noise) between wake-up and payload in order to avoid the ADR from switching.

For safety reasons it is recommended to use the same condition for freeze and unfreeze. If the unfreeze condition is on a later stage in the signal processing chain the possibility that this event does not occur definitely exists. For example if the freeze condition is set to RSSI and the unfreeze condition is set SYNC it may happen that an interferer is freezing the ADR on a wrong frequency and the unfreeze condition of SYNC is never reached.

6.13.8 Digital Baseband (DBB) Receiver

The digital baseband receiver comprises a matched data filter, a clock and data recovery, a data slicer, a line decoder, a wake-up generator, a frame synchronization and a data FIFO. The recovered data and clock signals are accessible via 2 separate pins. The FIFO data buffer is accessible via the SPI bus interface.

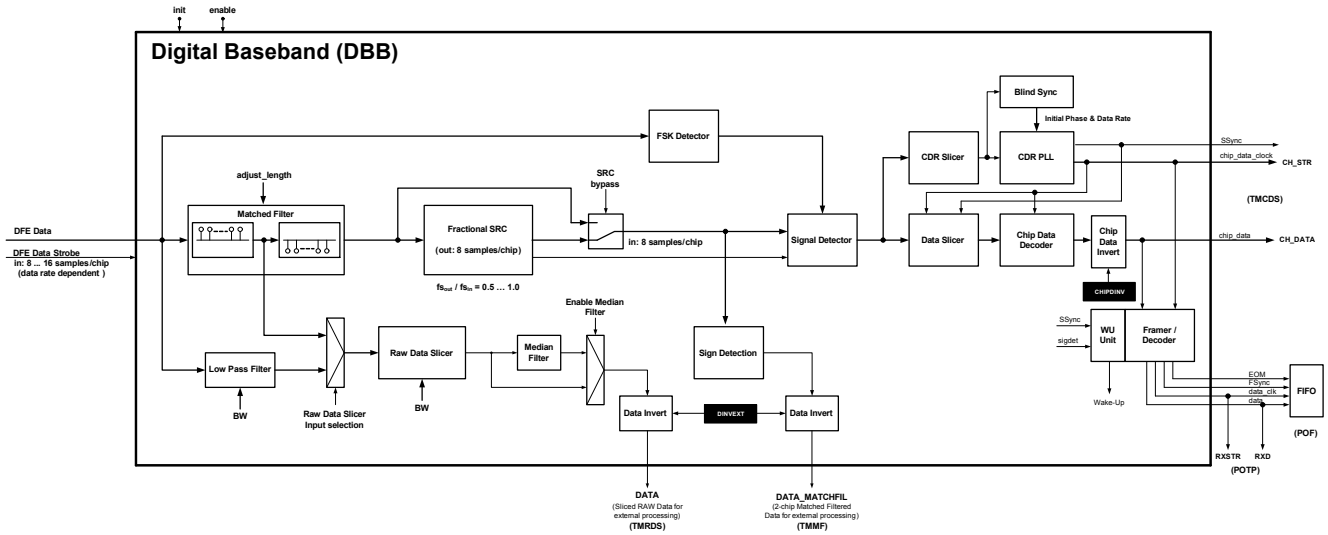


Figure 58 Functional Block Diagram Digital Baseband Receiver

6.13.9 Data Filter and Signal Detection

The data filter is a matched filter (MF). The frequency response of a matched filter has ideally the same shape as the power spectral density (PSD) of the originally transmitted signal, therefore the signal-to-noise ratio (SNR) at the output of the matched filter becomes maximum. The input sampling rate of the baseband receiver has to be between 8 and 16 samples per chip. The oversampling factor within this range is depending on the data rate. The MF has to be adjusted accordingly to this oversampling. After the MF a fractional sample rate converter (SRC) is applied using linear interpolation. Depending on the data rate decimation is adjusted within the range 1...2. Finally, at the output of the fractional SRC the sampling rate is adjusted to 8 samples per chip for further processing.

To distinguish whether the incoming signal is really a signal or only noise adequate detectors for ASK and FSK are built in.

Signal and Noise Detector

The Signal Detector decides between acceptable and unacceptable data (e.g. noise). This decision is taken by comparing the signal power of the actually received data (**Signal Power Readout Register**) with a configurable threshold level (registers **Signal Detector Threshold Level Register - Wakeup** and **Signal Detector Threshold Level Register - Run Mode**), which must be evaluated. In case the actual signal power is above the threshold, acceptable data has been detected.

To decide in case of FSK whether there is a data signal or simply noise at the output of the rate adapter, there is a Noise Detector implemented. The principle is based on a power measurement of the demodulated signal. The

current noise power is stored in the **Noise Power Readout Register** and is updated at every SPI controller access. The Noise Detector is useful if data signal is transmitted with small FSK deviations. In case the current noise power (**Noise Power Readout Register**) is below the configurable threshold (register **FSK Noise Detector Threshold Register**), a data signal has been detected.

The Signal Recognition mode must be configured based on whether ASK or FSK modulation is used. Signal Recognition can be a combination of Signal Detector and Noise Detector:

- Signal Detector (=Squelch) only (related registers:**Signal Detector Threshold Level Register - Wakeup** and **Signal Detector Threshold Level Register - Run Mode** and **Signal Power Readout Register**). This mode is generally used for ASK.
- Noise Detector only (related registers: **FSK Noise Detector Threshold Register** and **Noise Power Readout Register**).
- Signal and Noise Detector simultaneously.
- Signal and Noise Detector simultaneously, but the FSK noise detect signal is valid only if the **Signal Detector Threshold Low Level Register** threshold is exceeded. This is the recommended FSK mode, if minimum FSK deviation is not sufficient to use Signal Detector only.

Signal Recognition can also be used as Wake-up on Level criterion (see **“Wake-Up Generator” on Page 90**).

Figure 59 shows the system characteristics to consider in choosing the best Signal Detector level. On the one hand, a higher SIGDET threshold level must be set for achieving good FAR (False Alarm Rate) performance, but then the MER/BER (Message Error Rate/Bit Error Rate) performance will decrease. On the other hand, the MER/BER performance can be increased by setting smaller SIGDET threshold levels but then the FAR performance will worsen.

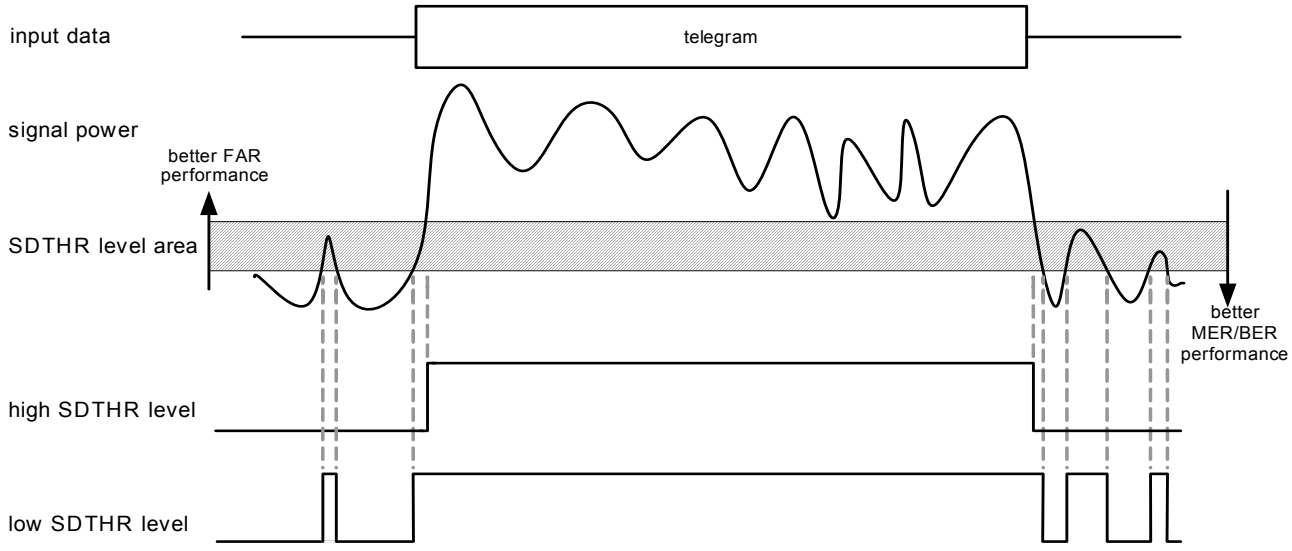


Figure 59 Signal Detector Threshold Level

Quick Procedure to Determine Signal and Noise Detector Thresholds

Preparation:

A setup is required with original RF hardware as in the final application. The values of **Signal Power Readout Register** and **Noise Power Readout Register** can be read via the final application.A complete configuration file using right modulation, data rate and Run Mode Slave, must be prepared and downloaded to the TDA5340.

Signal Detector Threshold for ASK

Take 500 readings of **Signal Power Readout Register** (50 are also possible, but this leads to less accurate results) with no RF input signal applied (=noise only). Calculate average and Standard Deviation. Signal Detector Threshold is average plus 2 times the Standard Deviation. To load the **Signal Detector Threshold Level Register - Wakeup** and **Signal Detector Threshold Level Register - Run Mode** register the calculated value must be rounded and converted to hexadecimals. For a final application, the Signal Detector Threshold should be varied to optimize the false alarm rate and the sensitivity.

Signal Detector Thresholds for FSK

Do 500 readings of **Signal Power Readout Register** with no RF input signal applied (=noise only). Calculate average and Standard Deviation. Signal Detector Threshold is average plus 2 times the Standard Deviation. Of course this value has to be rounded and converted to hexadecimal. For a final application the Signal Detector Threshold should be varied to optimize the false alarm rate and the sensitivity.Verification if Squelch only is possible. Apply a bit pattern (e.g. PRBS9) with correct data rate at about -80 dBm input signal power and minimum FSK deviation to the RF input. Do 500 (50) readings of **Signal Power Readout Register**, calculate average minus three times the Standard Deviation. This value should be higher than the calculated Signal Detector Threshold calculated above. If this is not the case, Signal Detector AND Noise Detector must be used.

Noise Detector Threshold

Do 500 readings of **Noise Power Readout Register** with no RF input signal applied (=noise only). Calculate average and Standard Deviation. Noise Detector Threshold is average minus the Standard Deviation. Round this value and convert it to hexadecimal. For a final application, the Noise Detector Threshold should be varied to optimize false alarm rate and sensitivity.

Signal Detector Low Threshold

The Signal Detector Low Threshold is always required in combination with the Noise Detector. Set register bit SDLORE to 1 in register **Signal Detector Configuration Register**. Apply a bit pattern (e.g. PRBS9) at correct data rate at about -80 dBm input signal power and minimum FSK deviation to the RF input. Do 500 (50) readings of **Signal Power Readout Register**, calculate average. Change bit group SDLORSEL in **Signal Detector Threshold Level Register - Wakeup** till average is smaller than 50d (0x32). **Signal Detector Threshold Low Level Register** = 0.8 * (average - 3 * Standard Deviation). Set register SDLORE back to 0. The last setting of bit group SDLORSEL must also be used for configuration!

6.13.10 Data Slicer

The output signal of the matched filter within the internal data processing path is in the range of +x to -x (x is the maximum value of the internal bit width). If Code Violations within a Manchester encoded bit stream have to be detected, the data slicer has to recover the underlying chip stream instead of the bit stream. In this case zero values at the matched filter output lead to an additional slicing threshold and an implicit sensitivity loss. To provide the full reachable sensitivity for applications which do not need the symbols S (space) and M (mark), the data slicer has three different operating modes:

- Chip mode (Code Violations are allowed)
- Bit mode (without Code Violations)
- NRZ mode

The chip mode introduces an implicit sensitivity loss compared to the bit mode, because a zero-crossing in the 2-chip matched filter signal must be detectable. This is only possible when an additional slicing level is introduced in the data slicer. The data slicer internally maps a positive value to a 1 and a negative value to a -1. Everything inside the zero thresholds (zero-tube) becomes a 0. After that, the decoding to the chip-level representation is done by mapping the -1 to a “0” chip and the 1 to a “1” chip. A zero out of the data slicer is decoded to chip-level by referencing to the previous chip value.

In bit mode the data slicer has only one threshold (zero) to distinguish between the two levels of the matched filter output. The data slicer internally maps a positive value to a 1 and a negative value to a -1. After that, the selected line decoding is applied.

Data Slicer Chip mode:

- Code violations detectable (TSI, or EOM) Performance loss compared to bit mode
- Activation via setting register **Slicer Configuration Register** to a value of
  - 0x90 (Chip Mode EOM-CV: For patterns with code violation in data packet and optimized for activated EOM code violation criterion and optional data length criterion.)
  - 0x94 (Chip Mode EOM-Data length: For patterns with code violations in data packet and optimized for activated EOM data length criterion only.)
  - 0xD5 (Chip Mode Transparent: When Framer is not used, but CH_DATA and CH_STR are used for external processing.)

Data Slicer Bit Mode

- No code violations detectable
- Full performance
- In case of Bi-phase mark and Bi-phase space an additional bit must be sent to ensure correct decoding of the last bit
- Activation via setting **Slicer Configuration Register** to a value of 0x75

In Data Slicer Bit mode an even number of TSI chips needs to be used.

When Data Slicer Bit mode is selected, then the last chip of RUNIN must be different from first chip of TSI (e.g. Runin-bit sequence 000000 and TSI bit sequence 0xx...xxx is OK). Otherwise the TSI will not be detected correctly.

On using Data Slicer Bit Mode, the Wake-up criteria Random Bits Detection and Pattern Detection cannot be applied.

When using Data Slicer Bit Mode, the Wake-up criterion Equal Bits Detection cannot be applied in case the transmitted Manchester/Bi-phase coded bit stream used for the Wake-up decision contains a sequence of at least two equal chips.

Data Slicer NRZ Mode

- longer RUNIN pattern required, prefered alternating Zeros and Ones
- Activation via setting **Slicer Configuration Register** to a value of 0x8C

A line decoder decodes the incoming data chips according to the encoding scheme (see **“Decoding/Encoding Modes” on Page 105**).

Slicer Level Saturation

The magnitude of the Matched Data Filter output defines the decision level of the Data Slicer. A huge input step at the matched filter input can lead to drift of the slicing level and therefore to bit errors. Such an input step can happen in FSK by applying a high frequency offsets (100kHz) with low deviations (1kHz). The calculation of the saturation value in the **Slicing Level Saturation Register** is described in the Register value calculation application note.

6.13.11 Raw Data Slicer - DATA Output

The Raw Data Slicer is used to provide data for external processing with the host controller on one of the port pins. The input of the Raw Data Slicer can be selected from two different sources as can be seen in **Figure 58**

The proper input to the Slicer should be selected by following conditions:

- One Chip Matched Filter output
  - NRZ Data
  - external CDR with correlation over a long preamble sequence (32Bit)
- Low Pass Data Filter
  - NRZ Data

– Data detection is done by evaluation of bit boundaries and edge detection

6.13.11.1 DC Offset Cancellation / Settling time

The input signal provided by the Low Pass Filter or the One Chip Matched Filter is not DC free. A DC Offset is introduced by a frequency offset in case of FSK and due to the Delog function in ASK case. The DC offset must be compensated to slice the data correctly. The DC cancellation is realized as a bandwidth adjustable low pass filter in front of the Raw Data Slicer.

The corner frequency of the DC offset cancellation low pass filter can be calculated as follows.

$$f_g = \frac{SampleRate \cdot BW_{SEL} \cdot BW_{SCA} \cdot DR[Bit/s]}{8} \quad (20)$$

Where the Sampling Rate is in between 8 and 16 which is defined from the system clock (f_{sys}) to Data rate (DR) ratio.

The figure below shows the output data of the One Chip Matched Data Filter and the DATA Output in comparison to the input data by changing the low pass filter corner frequency. As can be seen that the accuracy of the output edges are influenced by the low pass filter corner frequency.

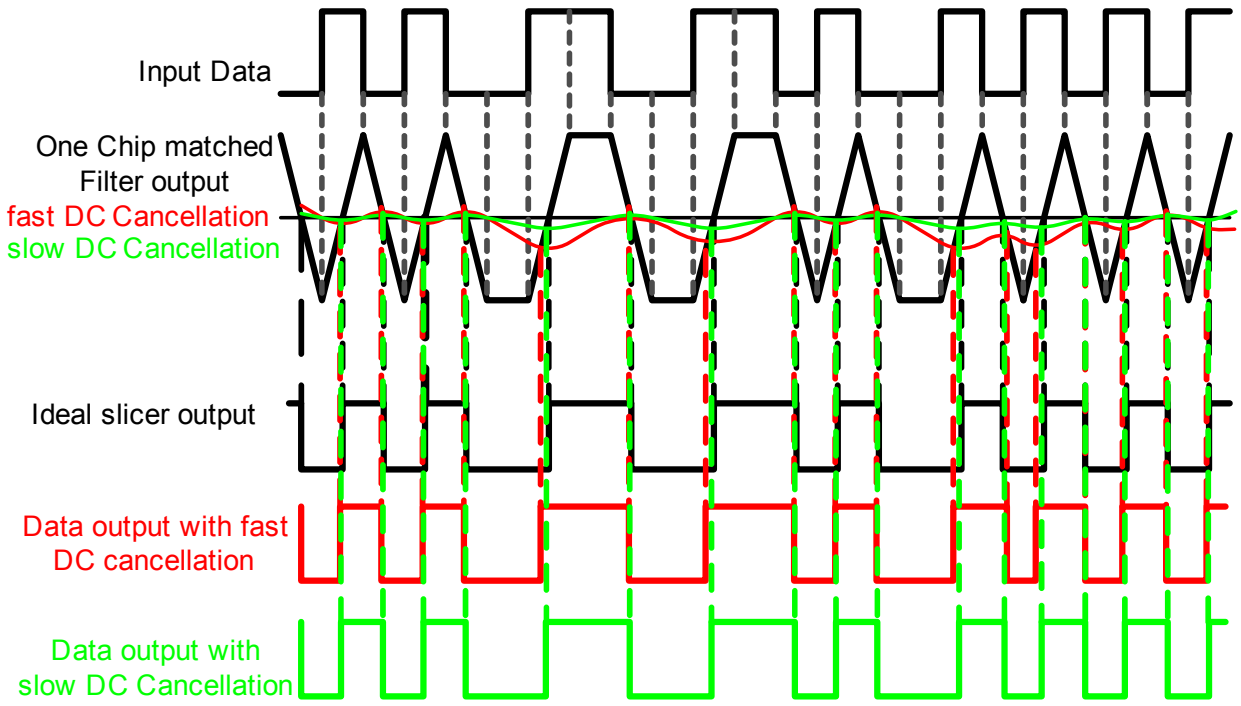


Figure 60 DATA Output / DC Offset Cancellation

For ASK and FSK modulation different approaches needs to be applied for the DC offset cancellation unit.

DC Offset Cancelation for FSK

The actual bandwidth of the DC offset cancellation can be selected within two areas. The two areas are necessary to achieve a fast settling in combination with a stable slicing value during the received data frame. The areas are separated by a programmable threshold in the **Externel Data Slicer BW Switching Threshold Register 0** and **Externel Data Slicer BW Switching Threshold Register 1**.

If the actual calculated DC offset is far away from the data signal a fast adjustment of the DC value can be achieved by using first a high filter bandwidth in order to achieve a fast settling. After reaching the desired DC offset the bandwidth can be reduced which provides a very stable slicing threshold.

Within the **External Data Slicer Configuration Register 1** the wide bandwidth with fast settling can be defined and the **External Data Slicer Configuration Register 0** provides the functionality to set the tighter bandwidth with a very stable slicing threshold.

DC Offset Cancelation for ASK

In ASK the bandwidth within both areas should be set to the same value due to the fact that in ASK are no huge DC offsets are expected.

6.13.11.2 Median Filter

The Median Filter can be enabled with the MEDFEN bit within the **External Data Slicer Configuration Register 2** and will be used to bridge single samples at the output of the One Chip Matched Filter and Low Pass Filter to avoid glitches on the output of the slicer.

6.13.12 Matched Filter Output - DATA Matched Filter

The Matched Filter has an inherent DC cancellation with a very fast settling time which can be applied only to a bi-phase encoded input data stream. Due to the nature of the Matched Filter the output has an edge delay which is depending of the input data sequence. Therefore an edge detection with a chip / bit duration measurement can not be applied to this output. The figure below shows the output data of the Matched Data Filter and the output of the DATA Matched Filter in comparison to the input data.

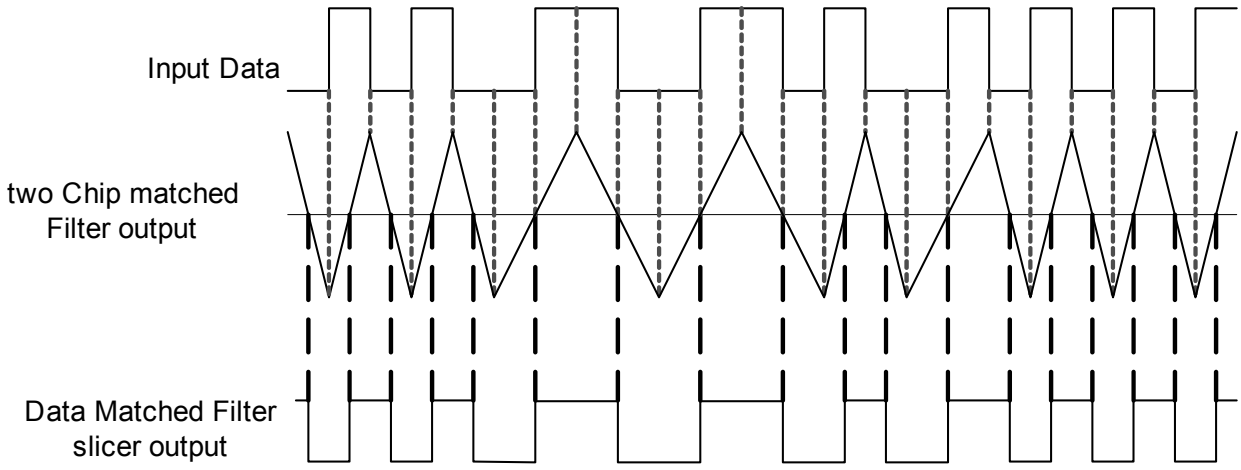


Figure 61 DATA Matched Filter Output

As shown in **Figure 61** the DATA Matched Filter output is a sign operation of the Matched Filter output this will lead to a systematic jitter which can be up to 50% of the chip duration.

6.13.13 Clock and Data Recovery (CDR)

An all-digital PLL (ADPLL) recovers the data clock from the incoming data stream. The second main function is the generation of a signal indicating symbol synchronization. Synchronization on the incoming data stream generally occurs within the first 4 bits of a telegram.

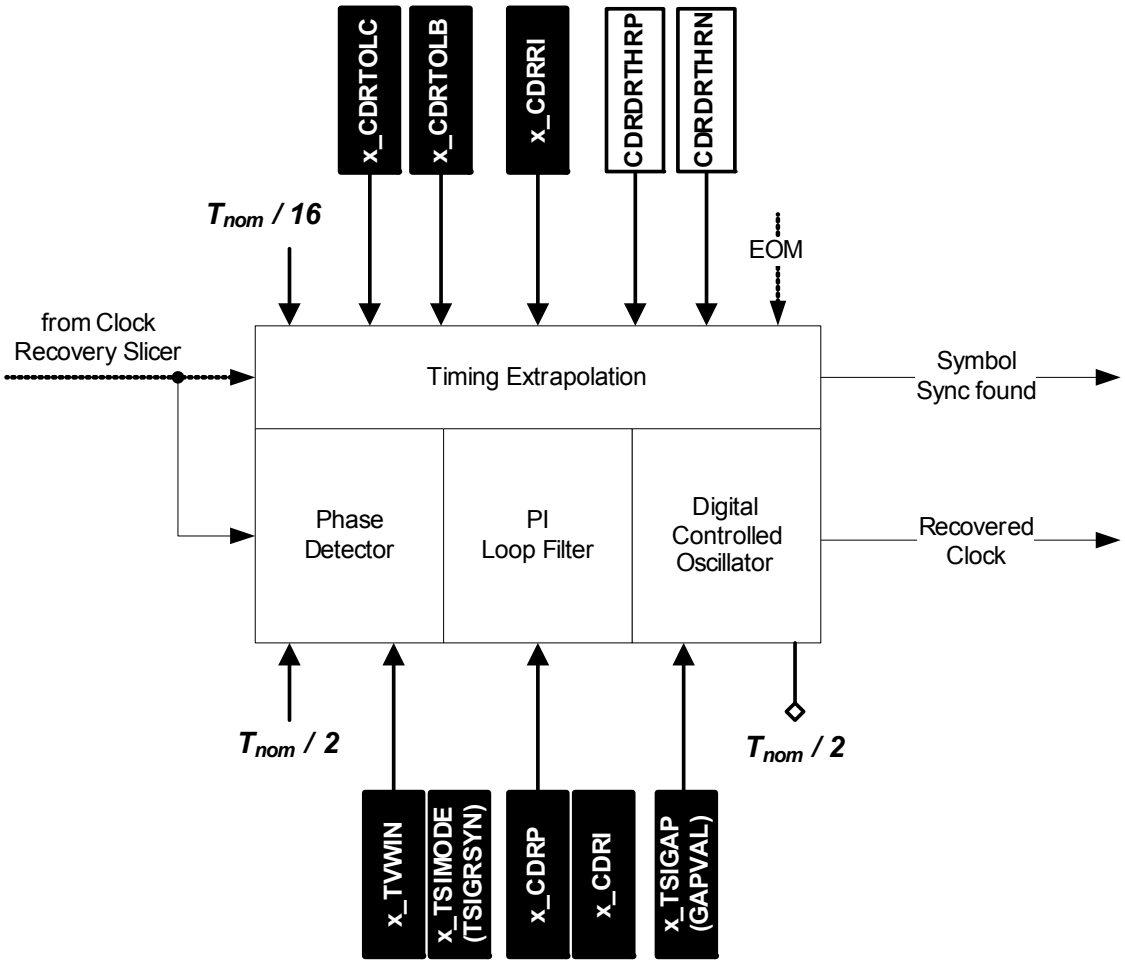


Figure 62 Clock Recovery (ADPLL)

Clock Recovery is implemented as standard ADPLL PI regulator with Timing Extrapolation Unit for fast settling.

In the unlocked state, the Timing Extrapolation Unit calculates the frequency offset for the incoming data stream. If the defined number of Bi-phase encoded bits are detected (the RUNIN length (RUNLEN) can be set in the **CDR Configuration Register 0**), the I-part and the PLL oscillator will be set and the PLL will be locked.

When RUNLEN is set to small values, then the I-part is less accurate (residual error) and can lead to a longer needed PLL settling time and worse performance in the first following bits. Therefore the selected default value is a good compromise between fast symbol synchronization and accuracy/performance.

Duty cycle and data rate acceptance limits are adjustable via registers. After locking, the clock must be stable and must follow the reference input. Therefore, a rapid settling procedure (Timing Extrapolation Unit) and a slow PLL are implemented.

If the PLL is locked, the reference signal from the Clock Recovery Slicer is used in the phase detector block to compute the actual error. The error is used in the PI loop filter to set the digital controlled oscillator running frequency. For the P, I and Timing Extrapolation Unit settings, the default values for the **Clock and Data Recovery P Configuration Register** and **Clock and Data Recovery Configuration Register** are recommended.

The PLL will be unlocked, if a code violation of more than the defined length is detected, which is set in the A_TVWIN control register. Another criterion for PLL re synchronization is an End Of Message (EOM) signalled by the Framer block.

The CDR PLL oscillator generates the chip clock frequency which is equal to 2 time the data rate.

Settling Time (RUNIN length)

The ideal RUNIN pattern is a series of either Manchester 1's or Manchester 0's. This pattern includes the highest number of edges that can be used for synchronization. In this case, the number of physically sent RUNIN bits is 4.

The number of RUNIN bits specified in **CDR Configuration Register 0** should always be set to three. This setting defines the duration of the internal synchronization. Because of internal processing delays, the pattern length that must be reserved for RUNIN is longer.

Code/Timing Violation Window (TVWIN)

The PLL unlocks if the reference signal is lost for more than the time defined in the **Timing Violation Window Register** . During the TSI Gap (see TSI Gap Mode in **"Frame Synchronization" on Page 95**), the PLL and the TVWIN are frozen.

TVWIN time is the time during which the Digital Baseband Receiver should stay locked without any incoming signal edges detected. The time resolution is $T_{Bit}/16$.

Duty Cycle Variation

Ideally, the input signal to the Clock and Data Recovery (CDR) would have a chip width of 8 samples and a bit width of 16 samples and the CDR would not lock onto any input that violates this. However, due to variations in the duty cycle this stringent assumption for the pulse widths will in general not be true. Therefore it is necessary to loosen this requirement by using tolerance windows.

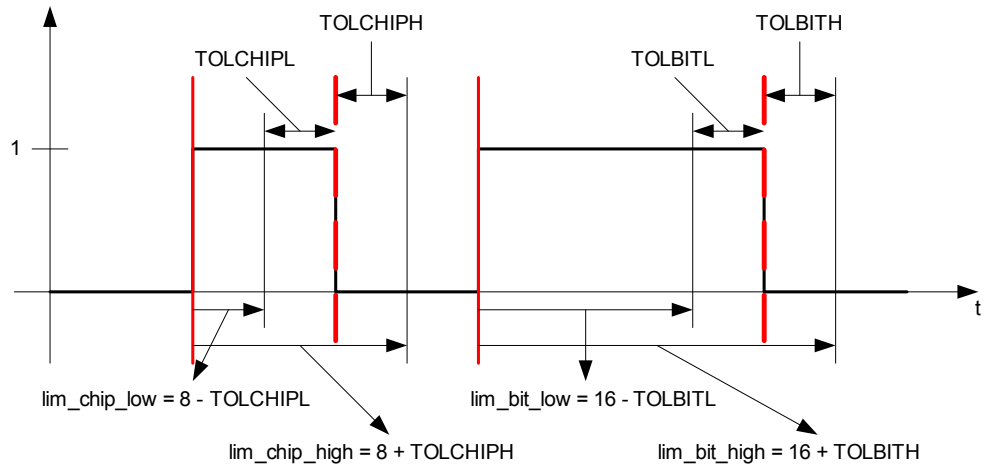


Figure 63 Definition of Tolerance Windows for the CDR

The **CDR Configuration Register 1** with TOLCHIP for the chip width tolerance and with TOLBIT for the bit width tolerance - that can be used to tighten or loosen the windows around the ideal pulse widths. As it can easily be seen from **Figure 63**, tighter windows will result in more stringent requirements for the input data to have a 50% duty cycle and bigger windows will allow the duty cycle to vary more. **Figure 63** also depicts the meaning of the bits in the **CDR Configuration Register 1**.

Data Rate Acceptance Limitation

The Clock and Data Recovery is able to accept data rate errors of more than +/-15% with a certain loss of performance. There exist Multi-Configuration applications where the data rate of both configurations are within this

range. So the adjacent data rates of these configurations are disturbing each other. The limitation of the data rate acceptance can be activated in this case.

The clock and data recovery (CDR) regenerates the clock based on the input data delivered from the clock recovery (CR) slicer. Symbol synchronization (cdr_lock) is achieved when a specified number of chips (can be set via RUNLEN bit of the **CDR Configuration Register 0**) has a valid pulse width. In parallel the preset value correlator estimates a preset value for the clock recovery PLL so that a shorter settling time is achieved. This preset value is also proportional to the data rate and is therefore used in the data rate acceptance limitation block. If the preset value is outside a certain range (positive and negative threshold configurable via **CDR Data Rate Acceptance Positive Threshold Register** and **CDR Data Rate Acceptance Negative Threshold Register**), the CDR does not go into lock and no symbol synchronization is generated.

For each configuration there exists one bit (DRLIMEN bit of **CDR Configuration Register 1**) to switch the data rate acceptance limitation functionality on or off. Data rate acceptance limitation is disabled by default. All configurations share the same threshold registers, the default thresholds are set so that almost all packets with a data rate error of +/-10% and larger are rejected.

The following statements summarize some important aspects that need to be kept in mind when using the described functionality:

- The output of the estimator must be described on statistical terms - this means that it can not be guaranteed that all packets with a certain data rate outside the allowed range will be rejected
- The quality of the estimated data rate value is mainly influenced by the setting of the signal and noise detectors
- Reducing the RUNIN length in **CDR Configuration Register 0** reduces the quality of the data rate estimation, resulting in a degradation of the performance of the data rate acceptance limitation block
- The same threshold can be used for FSK and ASK
- If the thresholds are too small it may happen that also packets with a valid data rate are rejected

6.13.14 Wake-Up Generator

A wake-up generation unit is used only in the Self Polling Mode for the detection of a predefined wake-up criterion in the received pattern. There are two groups of configurable wake-up criteria:

- Wake-up on Level criteria
- Wake-up on Data criteria

The search for the wake-up data criterion is started if data chip synchronization has occurred within the predefined number of symbols, otherwise the wake-up search is aborted. Several different wake-up patterns, like random bit, equal bit, bit pattern or bit synchronization, are programmable.

Additional level criterion fulfilment for RSSI or Signal Recognition can lead to a fast wake-up and to a change to Run Mode Self Polling. Whenever one of these Wake-up Level criteria is enabled and exceeds a programmable threshold, a wake-up has been detected.

The Wake-up Level criterion can be used very effectively in combination with the Ultrafast Fall Back to SLEEP Mode (see **“Ultra Fast Fall Back to Sleep (UFFB)” on Page 31**) for further decreasing the needed active time of the autonomous receive mode. A configurable observation time for Wake-up on Level can be set in the **Wake-up on Level Observation Time Register**.

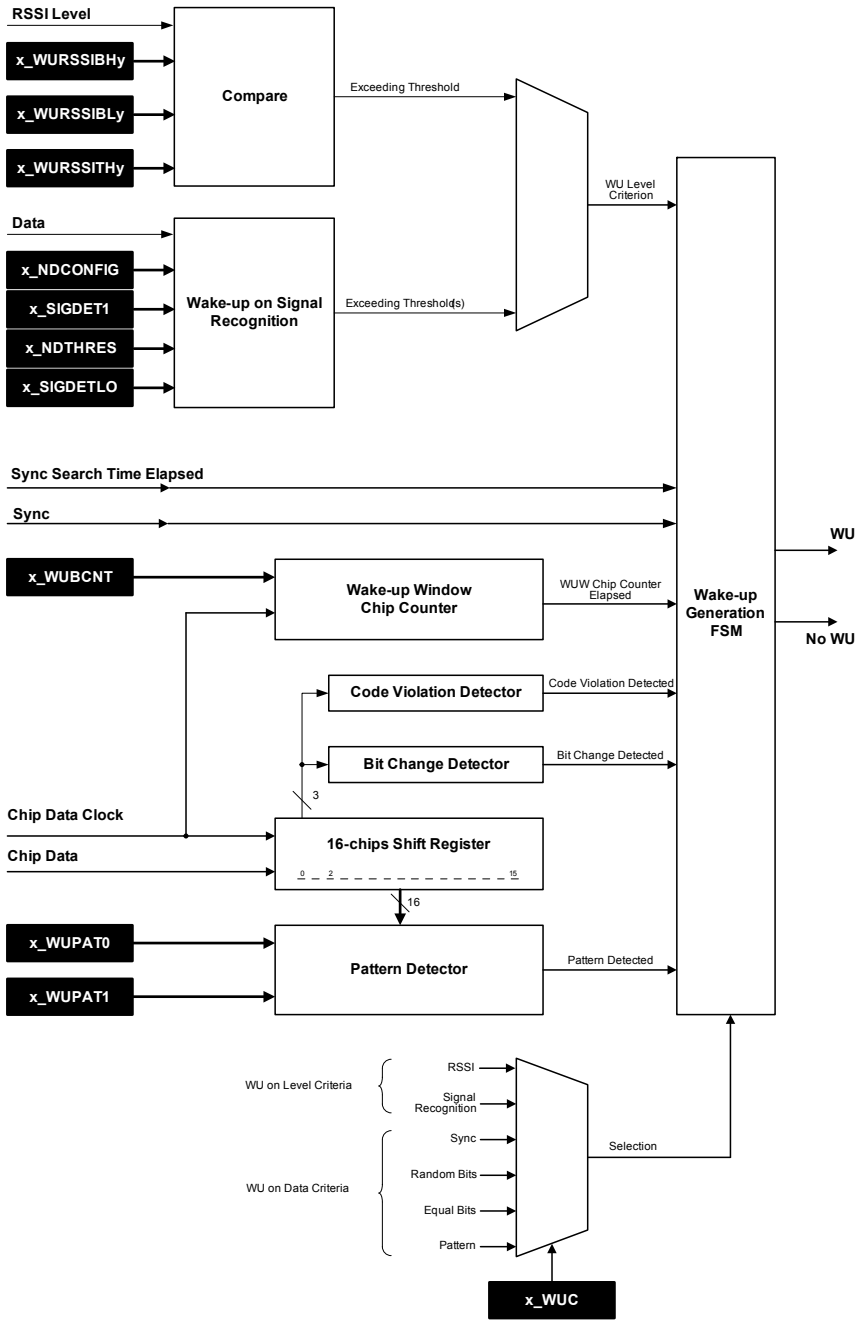


Figure 64 Wake-Up Generation Unit

6.13.14.1 Wake-Up on RSSI

The threshold **RSSI Wake-Up Threshold for Channel 1 Register** is used to decide whether the actual signal is a wanted signal or just noise. Any kind of interfering RSSI level can be blocked by using an RSSI blocking window. This window is determined by the thresholds **RSSI Wake-Up Blocking Level Low Channel 1 Register** and **RSSI Wake-Up Blocking Level High Channel 1 Register**, where 1 represents the actual RF channel (1 to 4). These two thresholds can be evaluated during normal operation of the application to handle the actual interferer environment.

The blocking window can be disabled by setting **RSSI Wake-Up Blocking Level Low Channel 1 Register** to the minimum value and **RSSI Wake-Up Blocking Level High Channel 1 Register** to the maximum value.

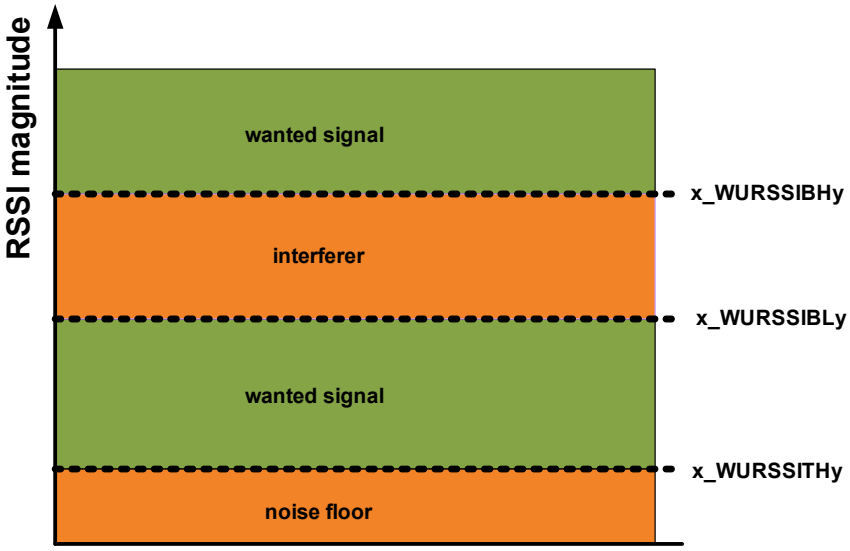


Figure 65 RSSI Blocking Thresholds

The necessary ON time for Wake-Up on RSSI can be calculated as follows:

$$t_{ON} = t_{RXstartup} + t_{WULOT} \quad (21)$$

The Wake-Up level observation time (t_{WULOT}) can be set in the **Wake-up on Level Observation Time Register** register and represents a division factor of the system time base (T_{SYS}). The WULOT time for Wake-Up on RSSI is mainly influenced by the coefficient of the peak memory filter (**Peak Memory Filter Up-Down Factor Register**). Slower up coefficient means also longer settling time of the RSSIPMF signal.

6.13.14.2 Threshold evaluation procedure

A statistical noise floor evaluation using read register **RSSI Peak Memory Filter Readout Register** (RMS operation) leads to the threshold **RSSI Wake-Up Threshold for Channel 1 Register**. The interferer thresholds **RSSI Wake-Up Blocking Level Low Channel 1 Register** and **RSSI Wake-Up Blocking Level High Channel 1 Register** are disabled when they are set to their default values.

For evaluation of the interferer thresholds, either use **RSSI Peak Memory Filter Readout Register** for RMS operation or during SPM and WU (Wake-Up) on RSSI use **Wakeup Peak Detector Readout Register** to statistically evaluate the interferer band. Finally the thresholds **RSSI Wake-Up Blocking Level Low Channel 1 Register** and **RSSI Wake-Up Blocking Level High Channel 1 Register** can be set. Wake-Up on RSSI can also be applied as additional criterion when already using a Wake-Up on Data criterion in Constant On-Off (COO) Mode.

NOTE: If e.g. an interferer ends/starts too close after/to the beginning/end of the observation time, then a decision level error can arise. This is due to the filter dynamics (settling time). Further, for interferer thresholds evaluation in SPM this changes interferer statistics. Several interferer measurements are recommended to suppress this, what makes sense anyway for a better distribution.

6.13.14.3 Wake-Up on Signal Recognition

Instead of the previously mentioned RSSI criterion, the Signal Recognition criterion (see **"Data Filter and Signal Detection" on Page 82**) can be applied for Wake-Up search. So the **Signal Detector Threshold Level Register - Wakeup**, **Signal Detector Threshold Low Level Register** and **FSK Noise Detector Threshold Register** threshold registers can be used.The observation time has to be specified in the register **Wake-up on Level Observation Time Register**. This observation time has to contain the delay in the signal path (12.5 µs + 2.25*Tbit)

and the duration for the comparison of the Signal Recognition criterion.The number of consecutive valid Signal Recognition samples/levels is compared vs. a threshold defined in **Signal Recognition Threshold Register**. This threshold has an influence on the false alarm rate. So **Signal Recognition Threshold Register** defines the minimum needed consecutive T/16 samples of the Signal Recognition output to be at high level for a positive Wake-Up event generation.

6.13.14.4 Wake-Up on Data Criterion

All SFRs configuring the Wake-up Generation Unit support the Multi-Configuration capability. The search for a wake-up data criterion is started if symbol synchronization is given within a certain duration (see **“Clock and Data Recovery (CDR)” on Page 88**); otherwise the wake-up search is aborted. During the observation period, the wake-up data search is aborted immediately if symbol synchronization is lost. If this is not the case, the wake-up search will last for the number of chips/bits defined in the register **Wake-Up Bit or Chip Count Register**.

The Wake-up Window (WUW) Chip/Bit Counter counts the number of received chips/bits and compares this number vs. the number of chips/bits defined in the register **Wake-Up Bit or Chip Count Register**.

The Code Violation Detector checks the incoming chip data stream for being Bi-Phase coded. A Code Violation is given if four consecutive chips are ’One’ or ’Zero’.

The Bit Change Detector checks the incoming Bi-phase coded bit data stream for changes from 'Zero' to 'One' or 'One' to 'Zero'.

The Pattern Detector searches for a pattern with 16 chips/bits length within the Wake-up Window. The pattern is configurable via the **Wake-Up Pattern Register 0** and **Wake-Up Pattern Register 1**.

The selection of 1 out of 4 wake-up data criteria is done via the **Wake-Up Control Register**.

The following table shows the different Wake-Up criteria in combination with the baseband modes.

Table 8 Wake-Up Criteria / Baseband Mode

Base Band Mode	Wake-Up Criteria			
	Pattern Detection / Bit Mode	**Pattern Detection / Chip Mode**	**Random Bit Detection**	**Equal Bit Detection**
Normal Mode	OK, abort Wake-Up search at Code Violation (CV)	OK	OK, abort Wake-Up search at CV	OK, abort Wake-Up search at CV
NRZ Mode	OK, abort Wake-Up search at 4 equal chips	OK	“3 out of 6 Detection” - abort Wake-Up search at 4 equal chips	“alternating Bit detection”
Bit Slicer Mode	not supported	OK	OK, abort Wake-Up search at 4 equal chips	OK, abort Wake-Up search at 3 equal chips

Pattern Detection

The incoming signal must match a dedicated pattern of up to 8 bits or 16 chips in Wake-Up Pattern Chip Mode. When the WUW chip counter elapses, the search is stopped. The higher the setting of **Wake-Up Bit or Chip Count Register** the longer it is possible to search for the wake-up pattern. The minimum for the **Wake-Up Bit or Chip Count Register** is 0x11! The pattern detection is stopped either when WUW elapses or when symbol synchronization is lost.The Wake-Up pattern can be extended from 16 chips to 16 bits on activation of WUPMSEL bit (Wake-Up Pattern Bit Mode) in the **Wake-Up Control Register**. In this Bit Mode no Code Violations (CV) are allowed and thus Pattern Detection is aborted, when a CV is detected.

Equal Bit Detection

Wake-up condition is fulfilled if all received bits inside of WUW are either 0 or 1. **Wake-Up Bit or Chip Count Register** holds the number of required equal bits. The higher the setting of **Wake-Up Bit or Chip Count Register** the lower the number of wrong wake-ups.

Equal bits detection is stopped if a bit change or a CV has been detected, or symbol synchronization is lost.

Random Bits Detection

Wake-up condition is fulfilled if there is no code violation inside of WUW. WUBCNT holds the number of required Bi-phase coded bits. The higher the setting of **Wake-Up Bit or Chip Count Register**, the lower the number of wrong wake-ups.

Random bits detection is stopped if a code violation has been detected, or symbol synchronization is lost.

Valid Data Rate Detection

Wake-up condition is fulfilled if symbol synchronization is possible inside of Sync Search Time out (see **“RUNIN, Synchronization Search Time and Inter-Frame Time” on Page 103**). WUBCNT is not used. This is the weakest wake-up data criterion, and should be avoided.

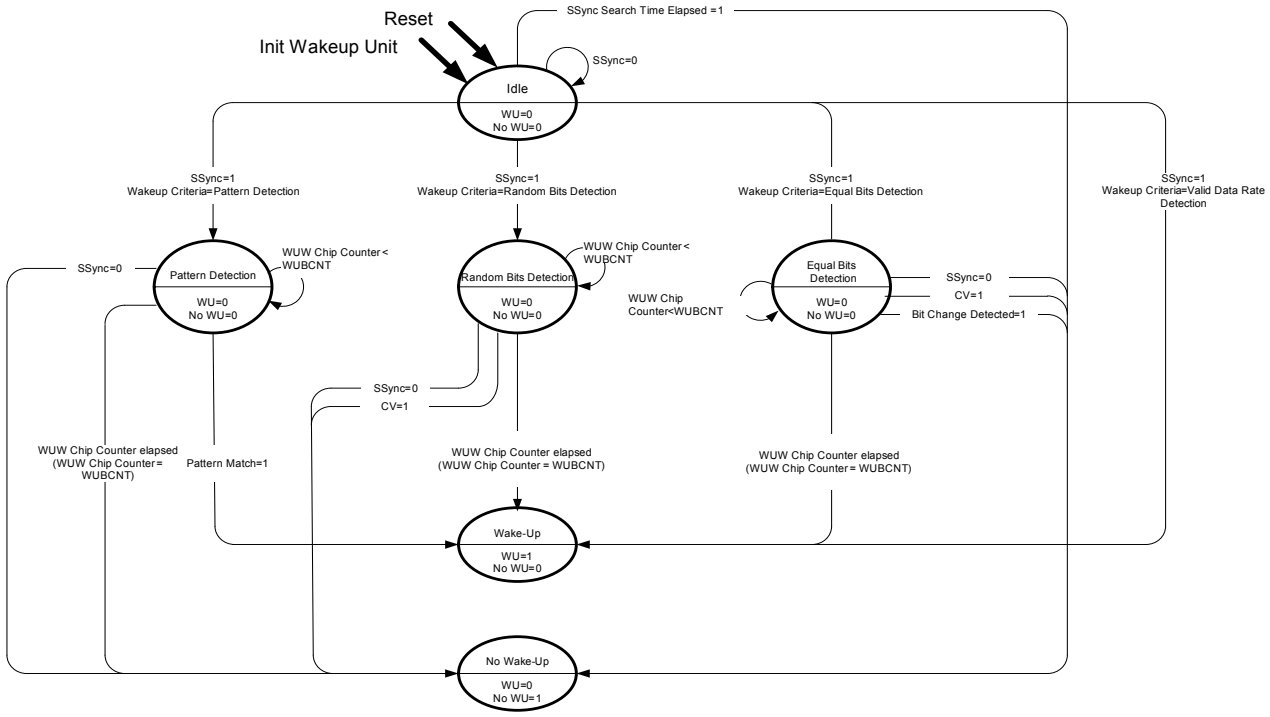


Figure 66 Wake-Up Data Criteria Search

6.13.15 Frame Synchronization

The Frame Synchronization Unit (Framer) synchronizes to a specific pattern to identify the exact start of a payload data frame within the data stream. This pattern is called Telegram Start Identifier (TSI).There are different TSI modes selectable via the configuration in register **TSI Detection Mode Register**:

- 16-Bit TSI Mode, supporting a TSI length of up to 16 bits or 32 chips
- 8-Bit Parallel TSI Mode, supporting two independent TSI pattern of up to 8 bits length each. Different payload length is possible for these two TSI pattern.
- 8-Bit Extended TSI Mode, identical to 8-Bit Parallel TSI Mode, but identifies which pattern matches by adding a single bit at the beginning of the data frame
- 8-Bit TSI Gap Mode, supporting two independent TSI pattern separated by a discontinuity

All SFRs configuring the Frame Synchronization Unit support the Multi-Configuration capability (Config A, B, C and D). The Framer starts working in Run Mode Slave after Symbol Sync found and in Self Polling Mode after wake-up found and searches for a frame until TSI is found or synchronization is lost. The input of the Framer is a sequence of Bi-phase encoded data (chips) or NRZ data. Basically the Framer consists of two identical correlators of 16 chips in length. It allows a Telegram Start Identifier (TSI) to be composed of Bi-phase encoded “Zeros” and “Ones”. The active length of each of the 16 chips correlators is defined independently in the **TSI Length Register A** and **TSI Length Register B**. The pattern to match is defined as a sequence of chips/bits in the **TSI Pattern Data Reference A Register 0**, **TSI Pattern Data Reference A Register 1**, **TSI Pattern Data Reference B Register 0** and **TSI Pattern Data Reference B Register 1**. Note that the RUNIN length shown in the figures below is the maximum needed RUNIN with the length of 8 chips. Further details on the needed RUNIN time of the receiver can be seen in **“RUNIN, Synchronization Search Time and Inter-Frame Time” on Page 103**.

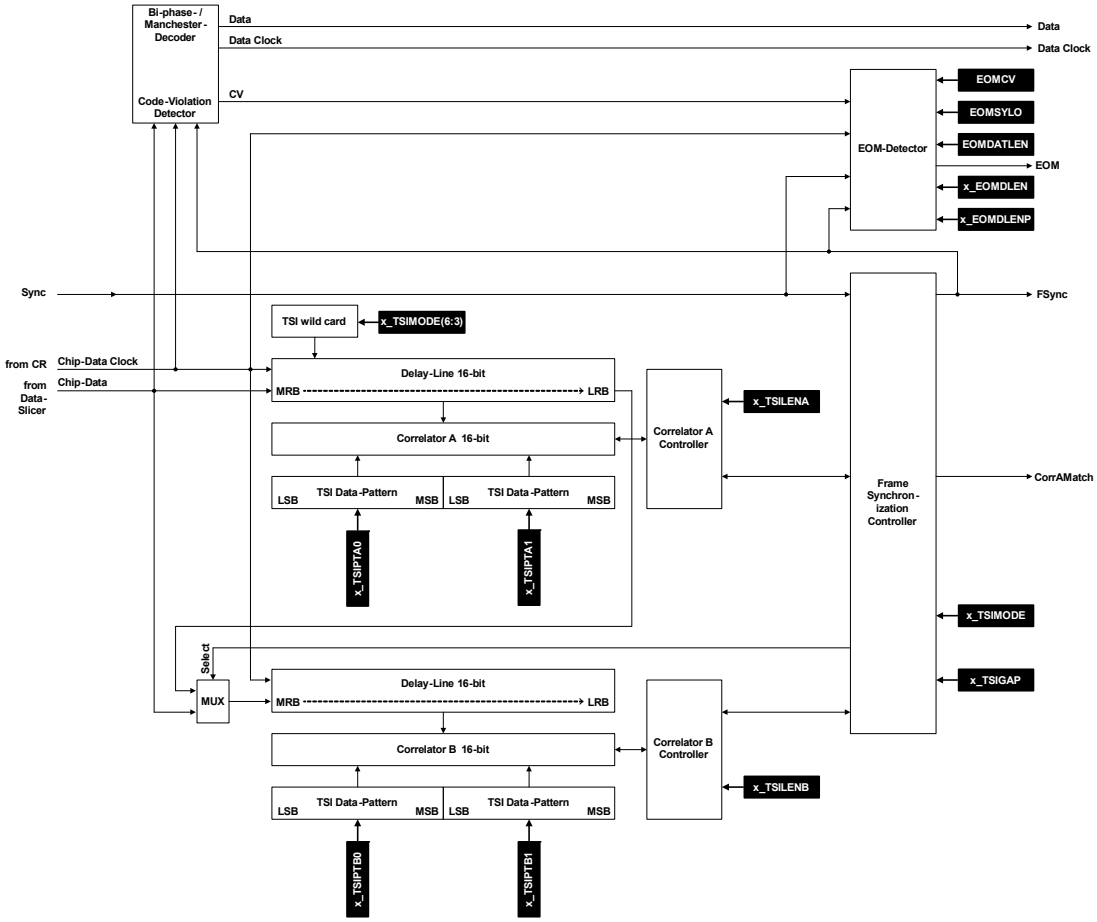


Figure 67 Frame Synchronization Unit

The two independent correlators can be configured in the **TSI Detection Mode Register** to work in one of the following four TSI modes:

16-Bit Mode: As a single correlator of up to 32 chips

The length of the **TSI Length Register A** must be set to 16d whenever **TSI Length Register B** is higher than 0.

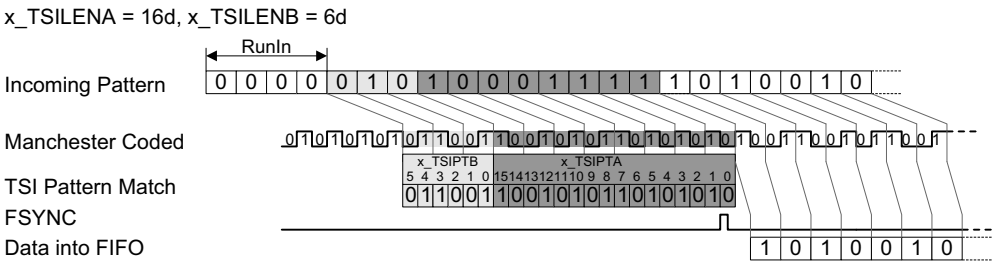


Figure 68 16-Bit TSI Mode

8-Bit Parallel Mode: As two correlators of up to 16 chips length each working simultaneously in parallel

In the following example, TSI Pattern B matches first and generates an FSYNC. The lengths of both TSI Patterns are now independent from each other. The payload length for these two TSI Pattern may be different.

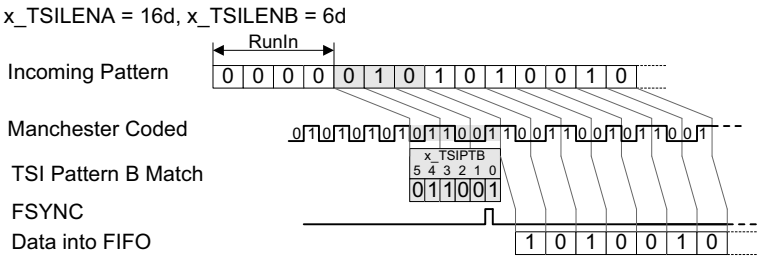


Figure 69 8-Bit Parallel TSI Mode

8-Bit Extended Mode: As two correlators of up to 16 chips length each working simultaneously in parallel, with matching information insertion

This bit is inserted at the beginning of the payload. “0” is inserted, when correlator A has matched and “1” when correlator B has matched. The payload length for these two TSI Pattern may be different.

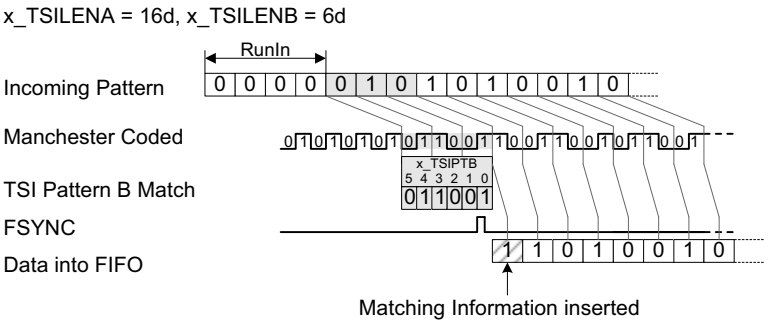


Figure 70 8-Bit Extended TSI Mode

8-Bit Gap Mode: As two sequentially working correlators of up to 16 chips length each

This mode is only used in combination with the TSI Gap Mode shown below!

This mode is used to define a gap between the two patterns which is preset in the **TSI Gap Length Register** . To identify exactly the beginning of the gap it would be helpful on occasion to place the first CV of the gap into the TSI Pattern A. In this case, the gap length needed for the **TSI Gap Length Register** must be shortened and the **Timing Violation Window Register** length must be extended.

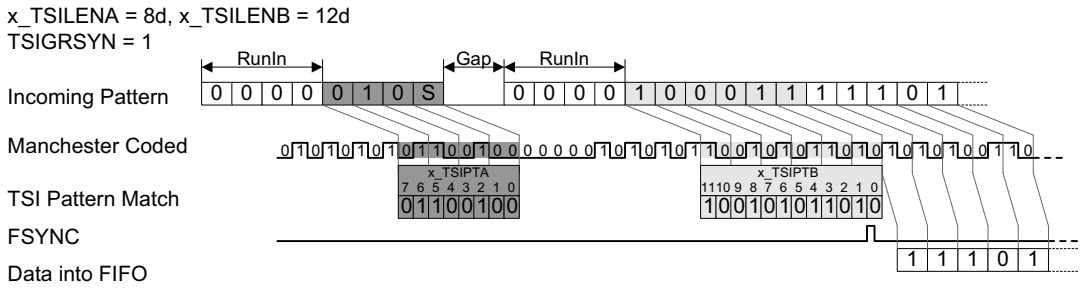


Figure 71 8-Bit Gap TSI Mode

Selection of a TSI Pattern

TSI patterns must be different to the wake-up bit stream and the RUNIN to clearly mark the start of the following payload data frame. It should be considered that the synchronization has a tolerance of about one bit. In addition, synchronization is related to data chips, and may occur in the middle of a data bit. This all must be tolerated by the data framer. Further details can be seen in **“RUNIN, Synchronization Search Time and Inter-Frame Time” on Page 103**.

Ideal TSI patterns have a unique bit combination at their end, which may also contain a number of code violations (CVs), when possible (see **“Data Slicer” on Page 84**).

Some examples of TSI patterns:

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

When CVs are used:

0 0 0 0 0 0 0 0 0 0 0 0 0 M 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 M 0

Note: CVs in a TSI are practical for better differentiation to the real data, especially if repetition of data frames is used for wake-up.

End of Message (EOM) Detection

An End Of Message (EOM) detection feature is provided by the EOM detector. Three criteria can be selected in the **End Of Message Control Register** to indicate an EOM.

- Data length
- Code Violation
- Loss of SYNC

The first is based on the number of received bits since frame synchronization. The number of expected bits is preset in the **EOM Data Length Limit Register**. Sending fewer bits as defined in the register will result in no EOM. The EOM counter will be reset after new frame synchronization. In 8-Bit Parallel TSI Mode and 8-Bit Extended TSI Mode, the payload length for the two independent TSI pattern may be different. Therefore the payload length for TSI B pattern can be preset in the **EOM Data Length Limit Parallel Mode Register**, while payload length for TSI A pattern can be preset in the **EOM Data Length Limit Register**. The second criterion is the detection of a Code Violation. This EOM criterion is not applicable for Data Slicer Bit mode.The third criterion is the loss of symbol synchronization. Depending on the **Timing Violation Window Register**, the Sync signal persists for a certain amount of time after the end of the pattern has been reached. Therefore, more bits could be written into the FIFO than sent.

The three EOM criteria can be combined with each other. If one of the selected EOM criteria is fulfilled, an EOM signal will be generated.

TSI Gap Mode

The TSI Gap Mode is only used if TSI patterns contain a gap that is not integer multiple of the data rate, e.g. if a gap is 7.7 data bits, or if a gap is longer than 10 data bits. In all other cases, gaps should be included in the TSI pattern as code violations.

Because of its complexity in configuration, TSI Gap Mode should be only used in applications as noted above!

For these special protocols, it is possible to lock the actual data frequency during a long Code Violation period inside a TSI (**TSI Gap Length Register** must have a minimum of 8 chips). TSIGAP is used to lock the PLL after TSI A was found. After the lock period, two different resynchronization modes are available (TSI Gap ReSYNchronization, TSIGRSYN):

- Frequency readjustment (PLL starts from the beginning), **TSI Detection Mode Register**.TSIGRSYN = 1. In this mode the T/2 gap resolution can be set in the 5 MSB x_TSIGAP register bits. The value in GAPVAL (3 LSB in **TSI Gap Length Register**) is not used. This is the preferred mode in TSI Gap Mode.

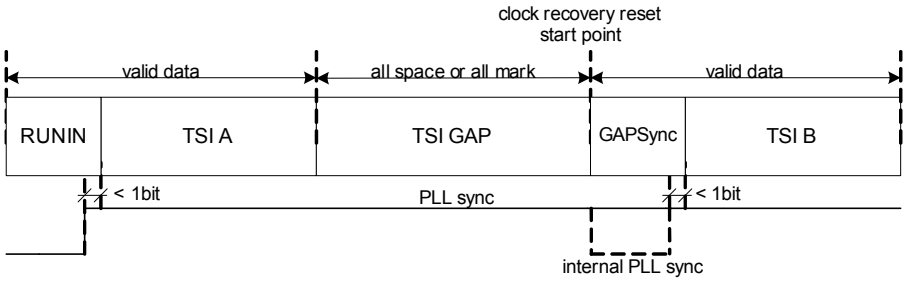


Figure 72 Clock Recovery Gap Resynchronization Mode TSIGRSYN = 1

- Phase readjustment only, **TSI Gap Length Register**.TSIGRSYN = 0. In this mode, the value in GAPVAL is used to correct the phase after the gap phase. Overall gap time can be defined in T/16 steps. The 5 MSB bits (**TSI Gap Length Register**.TSIGAP) define the real gap time and the 3 LSB bits (**TSI Gap Length Register**.GAPVAL) the DCO (digital controlled oscillator) phase correction value.

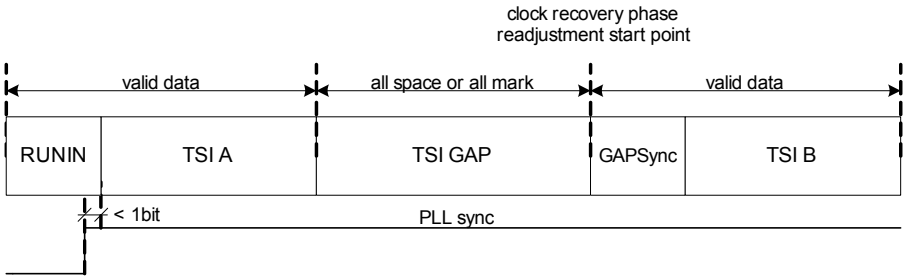


Figure 73 Clock Recovery Gap Resynchronization Mode TSIGRSYN = 0

When the time TSI GAP in the start sequence of the transmitted telegram has elapsed, the receiver needs a certain time (GAPSync = 5...6 chips) to readjust the PLL settings.

Behavior of the system at the starting position of the TSI B:

The starting position (TSI B start) for the TSI B comparison is independent from the RUNIN settings (**CDR Configuration Register 0**) and the resynchronization mode (**TSI Detection Mode Register**):

$$TSIB_{start}[chips] = TSIGAP[chips] + 6.8 \quad (22)$$

The incoming chips at TSI B start and the following incoming chips are compared with the contents of the register TSI B. Please notice that the receiver's PLL runs at the data rate determined before the gap. Therefore, the receiver calculates the gap based on this data rate.

Behavior of the system at the ending position of TSI B:

The system checks for the TSI B to match within a limited time. If there is no match within this time, then the receiver starts again to search for the TSI A pattern at the following incoming chips:

$$TSIB_{stop}[chips] = TSIGAP[chips] + TSIGAP[chips] + 11 \quad (23)$$

For a successful TSI B pattern match, the defined TSI B pattern must be between "Start of TSI B" and "Stop of TSI B". In the example below, the earliest possible start position would be the 18th chip and the latest possible start position would be the 22nd chip.

Please note that after a gap, the internal TSI comparison register is cleared (all chips set to ’0’). In this case, a TSI B criteria of “0000” would always match at the beginning. To avoid such an unwanted matching, set the highest TSI B match chip to ’1’.

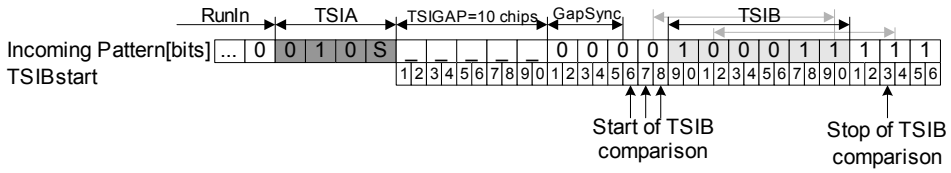


Figure 74 TSIGap TSIB Timing

The **Timing Violation Window Register** and TSIGAP dependency is shown in Figure 34.

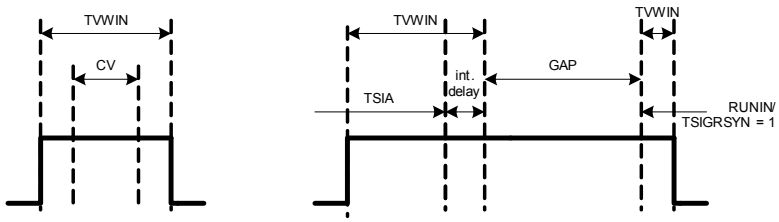


Figure 75 TVWIN and TSIGAP dependency example

Timing Violation Window Register calculation for pattern without Gap time:

$$TVWIN = round\left(\left(8 + 16 \cdot CV + 8\right) \cdot 1.25\right) \tag{24}$$

The entire **Timing Violation Window Register** time is made up of the CV number itself, the half bit before CV and the half bit after the CV. To reach all frequency and duty cycle errors, 25% of the overall sum must be added.

Timing Violation Window Register calculation with Gap time:

$$TTVWIN = round\left(\max\left\{\left(\left(8 + 16 \cdot CV + 8\right) \cdot 1.25\right), \left(8 + 16 \cdot TSIA_{CV} + 16 + 8\right) \cdot 1.25\right\}\right) \tag{25}$$

6.13.16 Message ID Scanning

This unit is used to define an ID or special combination of bits in the payload data stream, which identifies the pattern. All SFRs configuring the Message ID Scanning Unit feature the Multi-Configuration capability. Furthermore, it is available in the Slave and Self Polling Mode. The MID Unit can be mainly configured in two modes: 4-Byte and 2-Byte organized Message ID (see **Message ID Control Register 1**.MIDBO). For each configuration there are 20 8-bit registers designed for ID storage. SFRs are used to configure the MID Unit: Enabling of the MID scanning, setting of the ID storage organization, the starting position of the comparison and number of bytes to scan. When the Message ID Scanning Unit is activated, the incoming data stream is compared bit-wise serially with all stored IDs. If the Scan End Position is reached and all received data have matched the observed part of at least one MID the Message ID Scanning Unit indicates a successful MID scanning to the Master FSM, which generates an MID interrupt. Please note that the default register value of the **Message ID Register 0** to **Message ID Register 19** is set to 0x00. All MID registers must be set to a pattern value to avoid matching to default value 0x00.If the MID Unit finishes ID matching without success, the data receiving is stopped and the FSM waits again for a Frame Start criterion. The received bits are still stored in the FIFO.

4-Byte Organized Message ID:

In this mode four bytes are merged to define an ID-Pattern. This does not mean that the ID must be exact four bytes long. The number of bytes used is defined in the MIDNTS bits in the **Message ID Control Register 1**. Up to 5 ID Patterns are available.

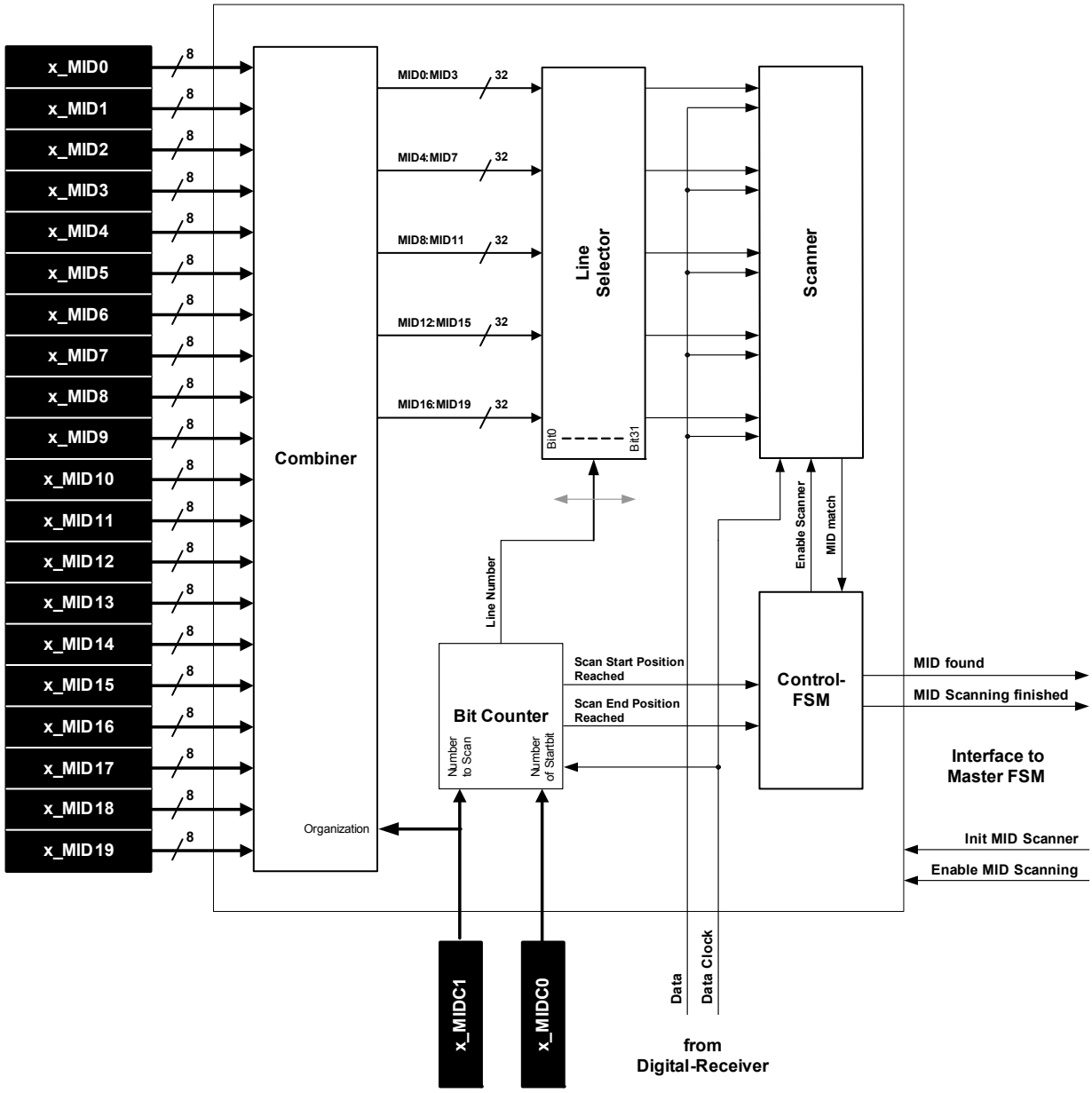


Figure 76 4-Byte Message ID Scanning

2-Byte Organized Message ID:

In this mode two bytes are merged to define an ID Pattern. Up to 10 patterns are possible.

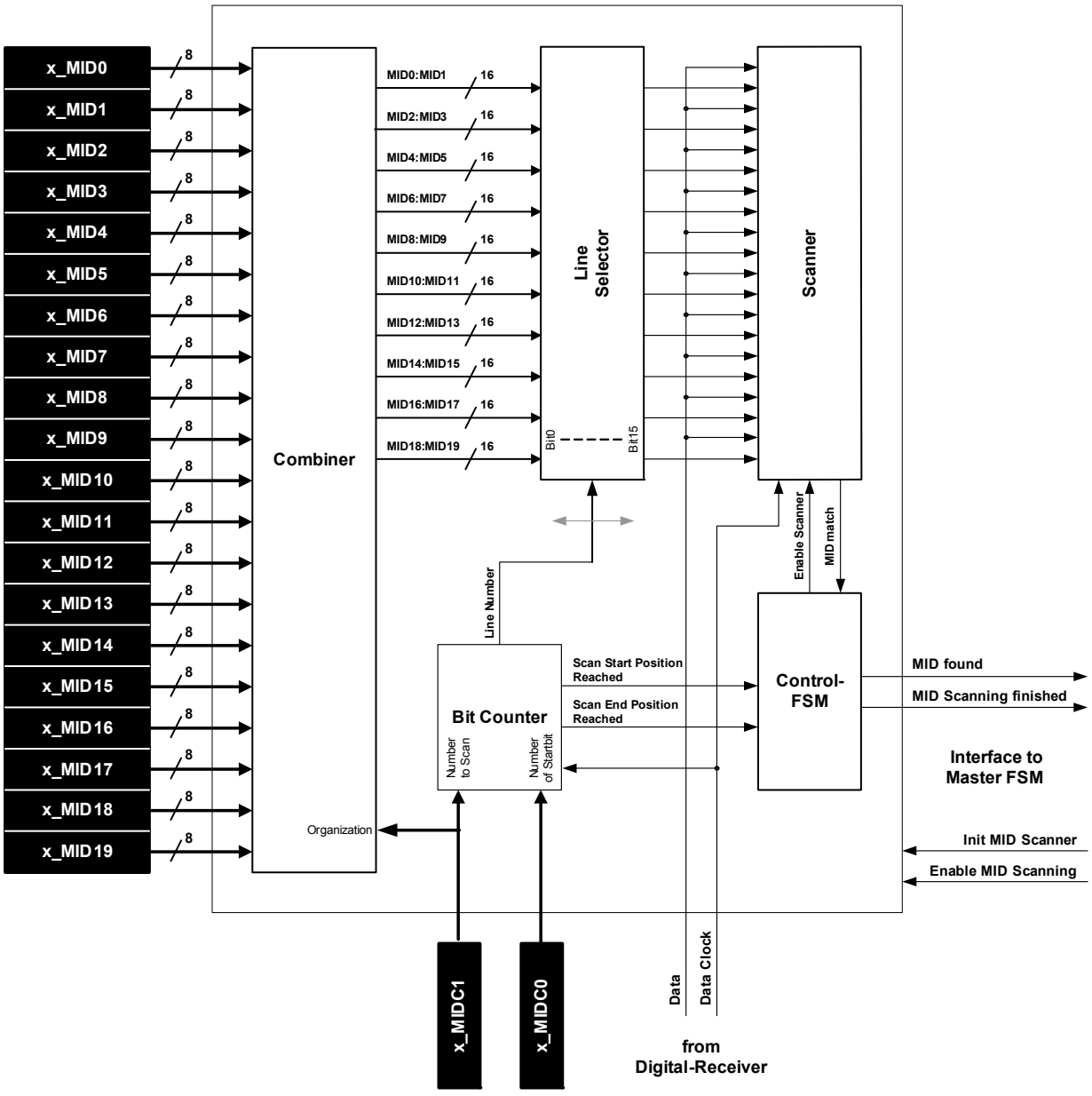


Figure 77 2-Byte Message ID Scanning

ID Position Configuration:

It is possible to choose which part of the incoming data stream is compared against the stored MIDs. The **Message ID Control Register 0** contains the Scan Start Position. If the Bit Counter detects the Scan Start Position, the Control FSM enables the Scanner. The **Message ID Control Register 1** contains the number of bytes to scan. During the observation period, the Message ID Scanning is aborted immediately by the Master FSM, if symbol synchronization is lost or an EOM (End Of Message) is detected.

Example:

Start Selection: 0010001b

Number to scan: 00b, 01b, 10b, 11b

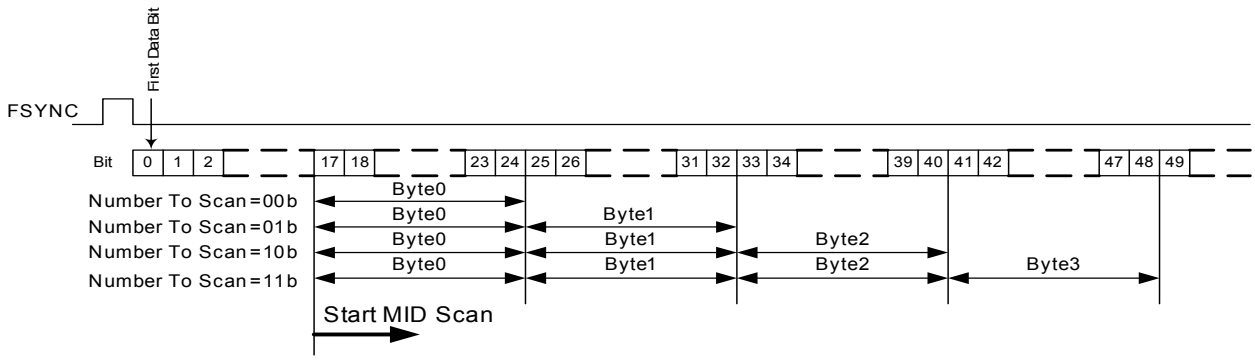


Figure 78 MID Scanning

The starting position in this case is Bit 17. Depending on the number to scan, the corresponding number of bytes is compared with the stored MIDs.

6.13.17 RUNIN, Synchronization Search Time and Inter-Frame Time

The functionality of the Digital Baseband Receiver is divided into four consecutive data processing stages; the data filter, clock and data recovery, data slicer and frame synchronization unit. The architecture of the Digital Baseband Receiver is optimized for processing bi-phase coded data streams.The basic structure of a payload frame is shown in **Figure 79**. The protocol starts with a so called RUNIN. The RUNIN with the minimum length of four bi-phase coded symbols is used for internal filter settling and frequency adjustment. The TSI (Telegram Start Identifier), which is used as framing word, follows the RUNIN sequence. The payload contains the effective data. The length of the valid payload data is defined as the length itself or additional criteria (e.g. loss of Sync). Please note that almost all transmitted protocols send a wake-up sequence before the payload frame. This wake-up sequence allows a very fast decision, whether there is a suitable message available or not.

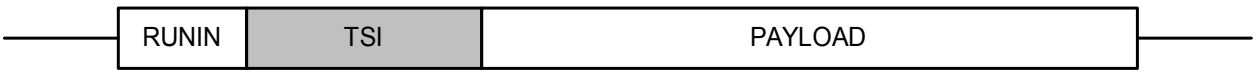


Figure 79 Structure of Payload Frame

Two important system parameters are described in this section: the Synchronization Search Time Out (**Synchronization Search Time-Out Register**) and the Inter-Frame Time. The processing sequence of a payload frame is shown in **Figure 80**.

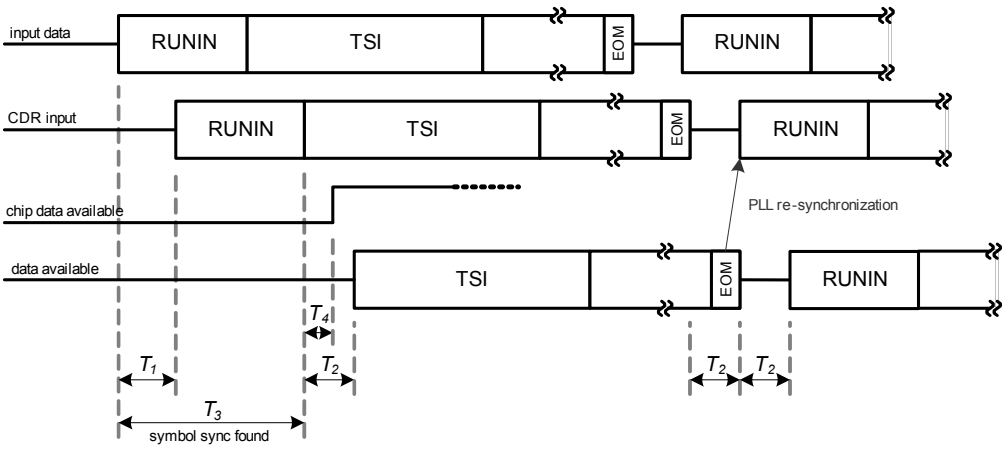


Figure 80 Data Latency

The overall system latency time is calculated in two steps: T1 is the delay between ADC input (ASK) / limiter output (FSK) and the CDR input, and T2 is the time between Symbol Sync Found and the Framer output (decoded data available). T4 is the time between Symbol Sync Found and Chip Data output (RX mode TMCDS). T4 = 1 T. T is the nominal duration of one data bit. T1 latency time include: (T1 = 12.5µs + 2 T)

- digital frontend processing delaymatched filter computation timesignal detector delay

T2 latency time include: (T2 = 1.5 T + 0.5 T[1])

- Data Slicer computation time
- Framer computation time.

The synchronization search time T3 is the time the receiver requires to search for a pattern in an incoming data stream and needs to be considered in the receivers start-up phase. The minimum value of the search time out length is the consequence of the system latency time T1, the RUNIN length and the time of asynchronous between transmitter and receiver.This means, that for the minimum length of register value for **Synchronization Search Time-Out Register**, the value 2 bits plus 12.5 µs plus the RUNIN length, which is set in the **CDR Configuration Register 0**. RUNLEN register, plus 2 bits (to consider worst case RUNIN patterns and TX-RX asynchronous) have to be used. To reach data rate and duty cycle errors, 10% of the overall sum must be added.

$$SYSRCTO = roundup\left(\left(\left(\frac{12.5\mu s}{T_{bit}} + 2 + RUNINLEN + 2\right)\cdot 16\right)\cdot 1.1\right) \tag{26}$$

A second important system parameter that must be considered, is the minimal Inter-Frame Time (time between two data frames). This time is equal to the time T2 and has a length of 1.5 or 2 bits. The EOM to PLL resynchronization time is negligible in case **Digital Receiver Configuration Register**. INITDRXES is disabled. Otherwise T1 has to be added.

Note that the described Inter-Frame Time is based on the input pattern with equal signal power in the following data frame; in other cases, the Inter-Frame Time can vary from the calculated value.

$$T_{Inter-Frame1} = 1.5 \cdot T_{Bit}$$
$$T_{Inter-Frame2} = 1.5 \cdot T_{Bit} + 0.5 \cdot T_{Bit} + T_1 \tag{27}$$

1) The 0.5 T have to be added in case of activation of Bi-phase mark / space decoding mode and Data Slicer Bit mode without Code Violation see **Slicer Configuration Register**

The 0.5 T_{bit} have to be added in case of activation of Bi-phase mark / space decoding mode and Data Slicer Bit mode without Code Violation see **Slicer Configuration Register**

The T_1 has to be added in case of **Digital Receiver Configuration Register**.INITDRXES is enabled.

6.14 Decoding/Encoding Modes

The IC supports the following Bi-phase encodings:

- Manchester code
- Differential Manchester code
- Bi-phase space code
- Bi-phase mark code
- Miller code (TX only)
- NRZ

The encoding mode is set and enabled by bit group CODE in **Digital Receiver Configuration Register** (receiver) and **TX Configuration Regsiter** (transmitter) configuration register.

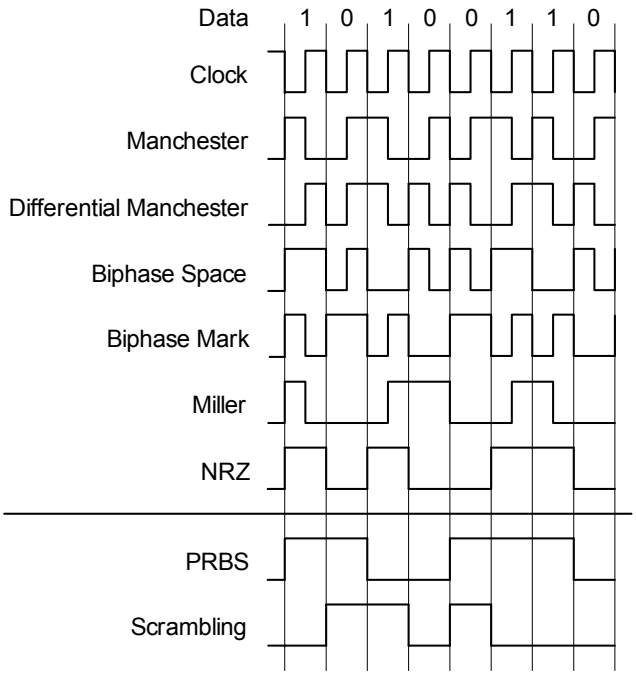


Figure 81 Encoding/Decoding Schemes

NRZ Mode

The performance of the receiver in NRZ mode is highly influenced by the length of the synchronization pattern (preamble) and also from the maximum allowed consecutive equal bits in the NRZ bit stream. The longer the synchronization pattern and the lower the max allowed consecutive equal bits (for example 3 out of 6 coding has only 3 consecutive equal bits) the better the performance of the system. The synchronization pattern should contain as much as possible bit transitions to enable a good settling of the Clock Data Recovery.

After the synchronization pattern the receiver found the symbol synchronization and the consecutive equal bits are bridged by the Clock Data Recovery using the Timing Violation Window which can be selected in the register **Timing Violation Window Register**.

The maximum number of consecutive equal bits are limited by:

- **Timing Violation Window Register** configuration (max 31 Bits)
- Peak Memory Filter Up and Down coefficient in case of ASK (see **Chapter 6.13.2**)

For NRZ the **Slicer Configuration Register** has to be set to 0x8C.

6.15 Definitions

6.15.1 Definition of Bit Rate

The definition for the bit rate in the following description is:

$$bitrate = \frac{symbols}{s} \tag{28}$$

If a symbol contains n chips (for Manchester n=2; for NRZ n=1) the chip rate is n times the bit rate:

$$chiprate = n \cdot bitrate \tag{29}$$

6.15.2 Definition of Manchester Duty Cycle

Several different definitions for the Manchester duty cycle (MDC) are in place. To avoid wrong interpretation some of the definitions are given below.

Level-based Definition
MDC = Duration of H-level / Symbol period

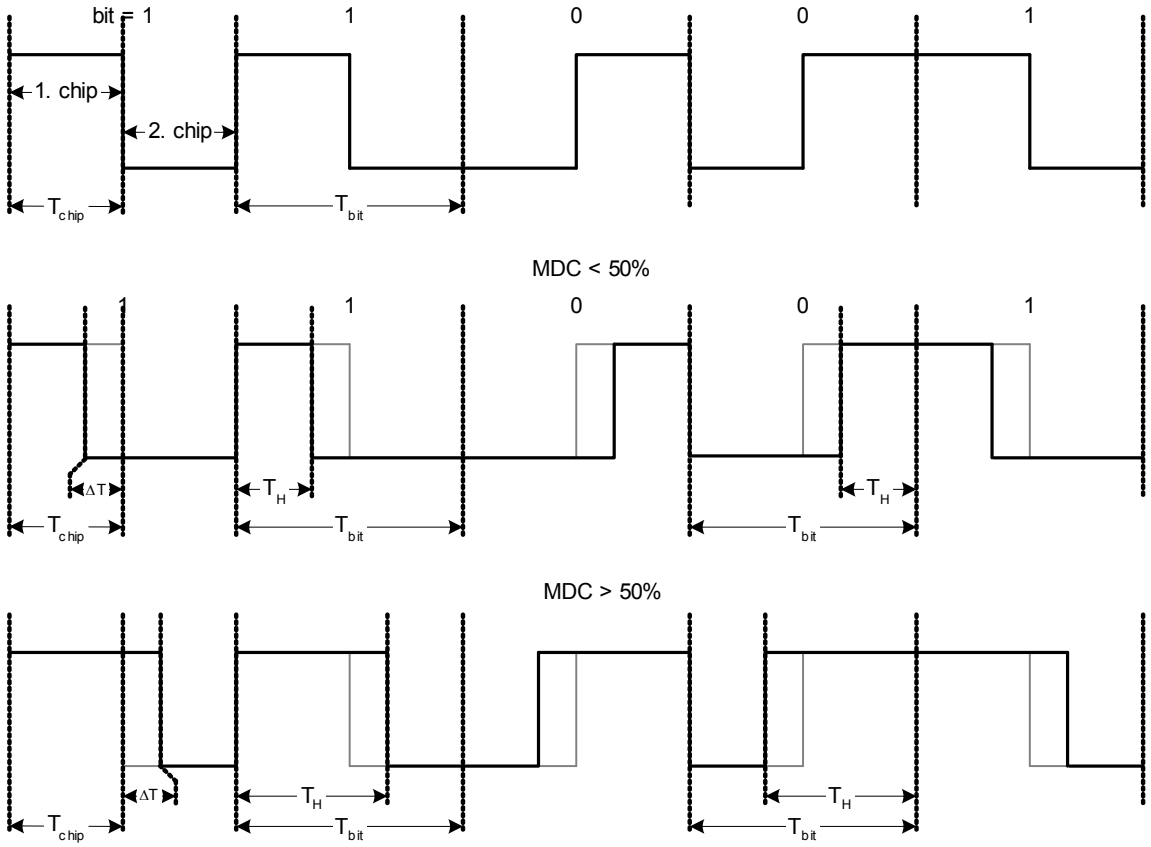


Figure 82 Definition A: Level-based definition

This definition determinates the duty cycle to be the ratio of the high pulse width and the ideal symbol period. The DC content is constant and directly proportional to the specified duty cycle. For DT > 0 the high period is longer than the chip-period and for DT < 0 the high period is shorter than the chip-period. Depending on the bit content, the same type of edge (e.g. rising edge) is sometimes shifted and sometimes not.

With this definition the Manchester duty cycle is calculated to

$$MDC_A = \frac{T_H}{T_{bit}} = \frac{T_{chip} + T}{T_{bit}}$$

(30)

Chip-based Definition
MDC = Duration of the first chip / Symbol period

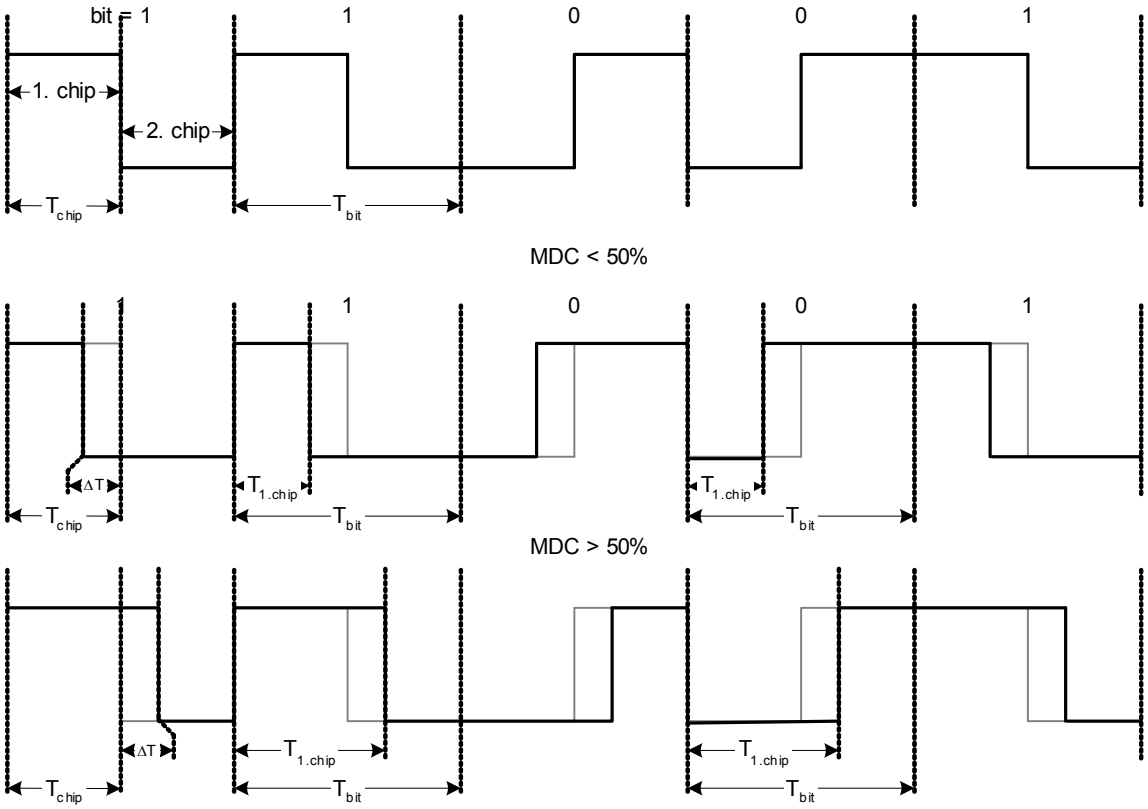


Figure 83 Definition B: Chip-based definition

This definition determinates the duty cycle to be the ratio of the first symbol chip and the ideal symbol period independently of the information bit content. The DC content depends on the information bit and it is balanced only if the message itself is balanced.For DT > 0 the first chip-period is longer than the ideal chip-period and for DT < 0 the first chip-period is shorter than the ideal chip-period.Depending on the bit content, the same type of edge (e.g. rising edge) is sometimes shifted and sometimes not.

With this definition the Manchester duty cycle is calculated to

$$MDC_B = \frac{T_{1,chip}}{T_{bit}} = \frac{T_{chip} + T}{T_{bit}}$$

(31)

Edge delay Definition
MDC = Duration delayed edge / Symbol period

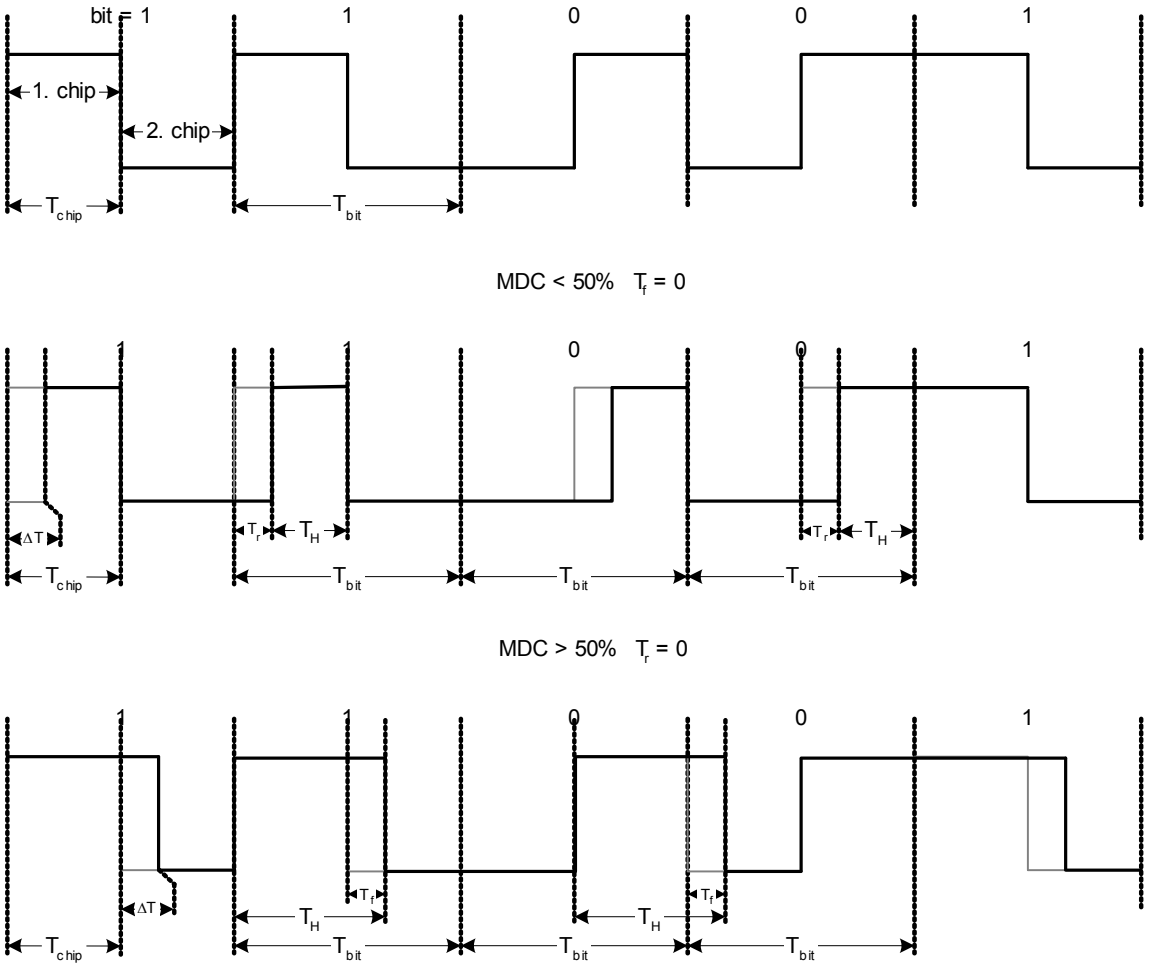


Figure 84 Definition C: Edge delay definition

This definition determinates the duty cycle to be the ratio of the duration of the delayed high-chip and the ideal symbol period independently of the information bit content. The position of the high-chip is determined by the delayed rising edge and/or the delayed falling edge. For T = T_{fall} -T_{rise} the Manchester duty cycle is calculated to

$$MDC_C = \frac{T_{delayedHighchip}}{T_{bit}} = \frac{T_{chip} + \Delta T}{T_{bit}} = \frac{T_{chip} + T_{fall} - T_{rise}}{T_{bit}} \quad (32)$$

Independent on the bit content, the same type of edge (rising edge and/or falling edge) is shifted.

6.15.3 Definition of Power Level

The reference plane for the power level is the input of the receiver board. This means, the power level at this point (P_r) is corrected for all offsets in the signal path (e.g. attenuation of cables, power combiners etc.).The specification value of power levels in terms of sensitivity is related to the peak power of P_r in case of On-Off Keying (OOK). This is noted by the unit dBm peak.

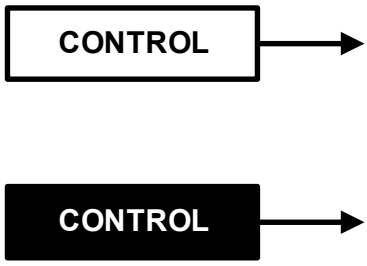
Specification value of power levels is related to a Manchester encoded signal with a Manchester duty cycle of 50% in case of ASK modulation.An RF signal generator usually displays the level of the unmodulated carrier ($P_{carrier}$). This has following consequences for the different modulation types:

Table 9 Power Level

Modulation schema	Realization with RF signal generator	Power level specification value
ASK	AM 100%	$P_r = P_{carrier}$ + 6dB
Pulse modulation (=OOK)	ASK	$P_r = P_{carrier}$
FSK	FM with deviation f:f_1 = $f_{carrier}$ - f f_2 = $f_{carrier}$ + f	$P_r = P_{carrier}$

For power levels in sensitivity parameters given as average power, this is noted by the unit dBm. Peak power can be calculated by adding 3 dB to the average power level in case of ASK modulation and a Manchester duty cycle of 50%.

6.15.4 Symbols of SFR Registers and Control Bits



Symbolizes unique SFR registers or SFR control bit(s), which are common for all configuration sets .

Symbolizes SFR registers or SFR control bit(s) with Multi-Configuration capability (protocol specific). In case of SFR register, the name starts with A_, B_, C_ or D_, depending on the selected configuration. This is generally noted by the prefix „x_“.

Figure 85 SFR Symbols

Generated Registers Overview

Table 10 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Registers, Registers			
A_MID0	Message ID Register 0	000_H	123
A_MID1	Message ID Register 1	001_H	123
A_MID2	Message ID Register 2	002_H	123
A_MID3	Message ID Register 3	003_H	124
A_MID4	Message ID Register 4	004_H	124
A_MID5	Message ID Register 5	005_H	124
A_MID6	Message ID Register 6	006_H	125
A_MID7	Message ID Register 7	007_H	125
A_MID8	Message ID Register 8	008_H	126
A_MID9	Message ID Register 9	009_H	126
A_MID10	Message ID Register 10	$00A_H$	126
A_MID11	Message ID Register 11	$00B_H$	127
A_MID12	Message ID Register 12	$00C_H$	127
A_MID13	Message ID Register 13	$00D_H$	127
A_MID14	Message ID Register 14	$00E_H$	128
A_MID15	Message ID Register 15	$00F_H$	128
A_MID16	Message ID Register 16	010_H	128
A_MID17	Message ID Register 17	011_H	129
A_MID18	Message ID Register 18	012_H	129
A_MID19	Message ID Register 19	013_H	130
A_MIDC0	Message ID Control Register 0	014_H	130
A_MIDC1	Message ID Control Register 1	015_H	130
A_IF1	IF1 Register	016_H	131
A_WUC	Wake-Up Control Register	017_H	132
A_WUPAT0	Wake-Up Pattern Register 0	018_H	133
A_WUPAT1	Wake-Up Pattern Register 1	019_H	134
A_WUBCNT	Wake-Up Bit or Chip Count Register	$01A_H$	134
A_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$01B_H$	135
A_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$01C_H$	135
A_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$01D_H$	136
A_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$01E_H$	136
A_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$01F_H$	137

Table 10 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
A_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	020_H	137
A_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	021_H	137
A_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	022_H	138
A_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	023_H	138
A_WURSSITH4	RSSI Wake-Up Threshold for Channel 4 Register	024_H	139
A_WURSSIBL4	RSSI Wake-Up Blocking Level Low Channel 4 Register	025_H	139
A_WURSSIBH4	RSSI Wake-Up Blocking Level High Channel 4 Register	026_H	139
A_SRTHR	Signal Recognition Threshold Register	027_H	140
A_SIGDETSAT	Slicing Level Saturation Register	028_H	140
A_WULOT	Wake-up on Level Observation Time Register	029_H	141
A_SYSRCTO	Synchronization Search Time-Out Register	$02A_H$	141
A_TOTIM0	Timeout Timer Register 0	$02B_H$	142
A_TOTIM1	Timeout Timer Register 1	$02C_H$	142
A_TOTIM_SYNC	SYNC Timeout Timer Register	$02D_H$	143
A_TOTIM_TSI	TSI Timeout Timer Register	$02E_H$	143
A_TOTIM_EOM	EOM Timeout Timer Register	$02F_H$	144
A_AFCLIMIT	AFC Limit Configuration Register	030_H	144
A_AFCAGCADRD	AFC/AGC/ADR Freeze Delay Register	031_H	145
A_AFCSFCFG	AFC Start/Freeze Configuration Register	032_H	145
A_AFCKCFG0	AFC Integrators Gain Coefficients Register 0	033_H	146
A_AFCKCFG1	AFC Integrators Gain Coefficients Register 1	034_H	146
A_PMFUDSF	Peak Memory Filter Up-Down Factor Register	035_H	147
A_AGCSFCFG	AGC Start/Freeze Configuration Register	036_H	148
A_AGCCFG0	AGC Configuration Register 0	037_H	149
A_AGCCFG1	AGC Configuration Register 1	038_H	150
A_AGCTHR	AGC Threshold Register	039_H	150
A_DIGRXC	Digital Receiver Configuration Register	$03A_H$	151
A_PKBITPOS	RSSI Peak Detector Bit Position Register	$03B_H$	152
A_PDFMFC	PD Filter and Matched Filter Configuration Register	$03C_H$	152
A_PDECF	Pre Decimation Factor Register	$03D_H$	153
A_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$03E_H$	153
A_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$03F_H$	154
A_SRC	Sample Rate Converter	040_H	154
A_EXTSLC0	External Data Slicer Configuration Register 0	041_H	155

Table 10 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
A_EXTSLC1	External Data Slicer Configuration Register 1	042_H	155
A_EXTSLC2	External Data Slicer Configuration Register 2	043_H	156
A_EXTSLTHR0	Externel Data Slicer BW Switching Threshold Register 0	044_H	157
A_EXTSLTHR1	Externel Data Slicer BW Switching Threshold Register 1	045_H	157
A_SIGDET0	Signal Detector Threshold Level Register - Run Mode	046_H	158
A_SIGDET1	Signal Detector Threshold Level Register - Wakeup	047_H	158
A_SIGDETLO	Signal Detector Threshold Low Level Register	048_H	158
A_SIGDETSEL	Signal Detector Range Selection Register	049_H	159
A_SIGDETCFG	Signal Detector Configuration Register	$04A_H$	160
A_NDTHRES	FSK Noise Detector Threshold Register	$04B_H$	160
A_NDCONFIG	FSK Noise Detector Configuration Register	$04C_H$	161
A_CDRP	Clock and Data Recovery P Configuration Register	$04D_H$	161
A_CDRI	Clock and Data Recovery Configuration Register	$04E_H$	163
A_CDRCFG0	CDR Configuration Register 0	$04F_H$	163
A_CDRCFG1	CDR Configuration Register 1	050_H	164
A_TVWIN	Timing Violation Window Register	051_H	165
A_SLCCFG	Slicer Configuration Register	052_H	165
A_TSIMODE	TSI Detection Mode Register	053_H	166
A_TSILENA	TSI Length Register A	054_H	167
A_TSILENB	TSI Length Register B	055_H	167
A_TSIGAP	TSI Gap Length Register	056_H	168
A_TSIPTA0	TSI Pattern Data Reference A Register 0	057_H	168
A_TSIPTA1	TSI Pattern Data Reference A Register 1	058_H	169
A_TSIPTB0	TSI Pattern Data Reference B Register 0	059_H	169
A_TSIPTB1	TSI Pattern Data Reference B Register 1	$05A_H$	169
A_EOMC	End Of Message Control Register	$05B_H$	170
A_EOMDLEN	EOM Data Length Limit Register	$05C_H$	170
A_EOMDLENP	EOM Data Length Limit Parallel Mode Register	$05D_H$	171
A_CHCFG	Channel Configuration Register	$05E_H$	172
A_TXRF	TX RF Configuration Register	$05F_H$	173
A_TXCFG	TX Configuration Regsiter	060_H	173
A_TXCHOFFS0	TX Channel Offset Register 0	061_H	174
A_TXCHOFFS1	TX Channel Offset Register 1	062_H	175
A_TXBDRDIV0	TX Baudrate Divider Register 0	063_H	175

Table 10 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
A_TXBDRDIV1	TX Baudrate Divider Register 1	064_H	175
A_TXDSHCFG0	TX Data Shaping Configuration Register 0	065_H	176
A_TXDSHCFG1	TX Data Shaping Configuration Register 1	066_H	176
A_TXDSHCFG2	TX Data Shaping Configuration Register 2	067_H	176
A_TXPOWER0	TX Power Configuration Register 0	068_H	177
A_TXPOWER1	TX Power Configuration Register 1	069_H	177
A_TXFDEV	TX Frequency Deviation Register	$06A_H$	178
A_PLLINTC1	PLL MMD Integer Value Register Channel 1	$06B_H$	178
A_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$06C_H$	179
A_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$06D_H$	179
A_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$06E_H$	180
A_PLLINTC2	PLL MMD Integer Value Register Channel 2	$06F_H$	180
A_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	070_H	181
A_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	071_H	181
A_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	072_H	182
A_PLLINTC3	PLL MMD Integer Value Register Channel 3	073_H	182
A_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	074_H	183
A_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	075_H	183
A_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	076_H	184
A_PLLINTC4	PLL MMD Integer Value Register Channel 4	077_H	184
A_PLLFRAC0C4	PLL Fractional Division Ratio Register 0 Channel 4	078_H	184
A_PLLFRAC1C4	PLL Fractional Division Ratio Register 1 Channel 4	079_H	185
A_PLLFRAC2C4	PLL Fractional Division Ratio Register 2 Channel 4	$07A_H$	185
A_RXPLLBW	PLL Bandwidth Selection Register for RX Mode	$07B_H$	186
A_TXPLLBW	PLL Bandwidth Selection Register for TX Mode	$07C_H$	187
A_PLLTST	PLL Startup Time Register	$07D_H$	187
A_ANTSW	Antenna Switch Configuration Register	$07E_H$	188
A_ADRSFCFG	ADR Start/Freeze Configuration Register	$07F_H$	189
A_ADRTCFG0	ADR Timeout Configuration Register 0	080_H	190
A_ADRTCFG1	ADR Timeout Configuration Register 1	081_H	190
A_ADRTCFG2	ADR Timeout Configuration Register 2	082_H	191
A_ADRTHR0	ADR Threshold Register 0	083_H	191
A_ADRTHR1	ADR Threshold Register 1	084_H	192
SFRPAGE	Special Function Register Page Register	$0A0_H$	192
PPCFG0	PP0 and PP1 Configuration Register	$0A1_H$	193
PPCFG1	PP2 and PPRF Configuration Register	$0A2_H$	194
PPCFG2	PPx Port Configuration Register	$0A3_H$	195
PPCFG3	PPRF_RSSI Configuration Register	$0A4_H$	196

Table 10 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
RXRUNCFG0	RX RUN Configuration Register 0	$0A5_H$	197
RXRUNCFG1	RX RUN Configuration Register 1	$0A6_H$	198
CLKOUT0	Clock Divider Register 0	$0A7_H$	199
CLKOUT1	Clock Divider Register 1	$0A8_H$	200
CLKOUT2	Clock Divider Register 2	$0A9_H$	200
ANTSW	Antenna Switch Configuration Register	$0AA_H$	201
RFC	RF Control Register	$0AB_H$	202
XTALCAL0	XTAL Coarse Calibration Register	$0AE_H$	202
XTALCAL1	XTAL Fine Calibration Register	$0AF_H$	203
RSSICFG	RSSI Configuration Register	$0B0_H$	203
ADCINSEL	ADC Input Selection Register	$0B1_H$	204
RSSIOFFS	RSSI Offset Register	$0B2_H$	205
RSSISLOPE	RSSI Slope Register	$0B3_H$	205
DELOGSFT	DELOG Shift Register	$0B4_H$	206
CDRDRTHRP	CDR Data Rate Acceptance Positive Threshold Register	$0B5_H$	206
CDRDRTHRN	CDR Data Rate Acceptance Negative Threshold Register	$0B6_H$	207
IM0	Interrupt Mask Register 0	$0B7_H$	207
IM1	Interrupt Mask Register 1	$0B8_H$	208
IM2	Interrupt Mask Register 2	$0B9_H$	209
SPMIP	Self Polling Mode Idle Periods Register	$0BA_H$	210
SPMC	Self Polling Mode Control Register	$0BB_H$	211
SPMRT	Self Polling Mode Reference Timer Register	$0BC_H$	211
SPMOFFT0	Self Polling Mode Off Time Register 0	$0BD_H$	212
SPMOFFT1	Self Polling Mode Off Time Register 1	$0BE_H$	212
SPMONTA0	Self Polling Mode On Time Config A Register 0	$0BF_H$	213
SPMONTA1	Self Polling Mode On Time Config A Register 1	$0C0_H$	213
SPMONTB0	Self Polling Mode On Time Config B Register 0	$0C1_H$	214
SPMONTB1	Self Polling Mode On Time Config B Register 1	$0C2_H$	214
SPMONTC0	Self Polling Mode On Time Config C Register 0	$0C3_H$	215
SPMONTC1	Self Polling Mode On Time Config C Register 1	$0C4_H$	215
SPMONTD0	Self Polling Mode On Time Config D Register 0	$0C5_H$	216
SPMONTD1	Self Polling Mode On Time Config D Register 1	$0C6_H$	216
EXTPCMD	External Processing Command Register	$0C7_H$	217
TXC	TX Control Register	$0C8_H$	218
RXC	RX Control Register	$0C9_H$	219
CMC	Chip Mode Control Register	$0CA_H$	220
TXCHNL	TX Channel Configuration Register	$0CB_H$	221

Table 10 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
PLLCFG	PLL Configuration Register	$0CC_H$	222
VACERRTH	VCO Autocalibration Error Threshold	$0CD_H$	222
PRBS	PRBS Starting Value Register	$0CE_H$	223
TXFIFOAEL	TX FIFO Almost Empty Level Register	$0CF_H$	223
TXFIFOAFL	TX FIFO Almost Full Level Register	$0D0_H$	224
RXFIFOAFL	RX FIFO Almost Full Level Register	$0D1_H$	224
PLLSTAT	PLL Status Register	$0D2_H$	224
IS2	Interrupt Status Register 2	$0D3_H$	225
IS0	Interrupt Status Register 0	$0D4_H$	226
IS1	Interrupt Status Register 1	$0D5_H$	227
RFPLLACC	RF PLL Actual Channel and Configuration Register	$0D6_H$	229
RSSIPWU	Wakeup Peak Detector Readout Register	$0D7_H$	230
RSSIPRX	RSSI Peak Detector Readout Register	$0D8_H$	230
RSSIPPL	RSSI Payload Peak Detector Readout Register	$0D9_H$	230
PLDLEN	Payload Data Length Register	$0DA_H$	231
ADCRESH	ADC Result High Byte Register	$0DB_H$	231
ADCRESL	ADC Result Low Byte Register	$0DC_H$	232
AFCOFFSET	AFC Offset Read Register	$0DD_H$	232
AGCADRR	AGC and ADR Readout Register	$0DE_H$	233
SPIAT	SPI Address Tracer Register	$0DF_H$	233
SPIDT	SPI Data Tracer Register	$0E0_H$	234
SPICHKSUM	SPI Checksum Register	$0E1_H$	234
SN0	Serial Number Register 0	$0E2_H$	235
SN1	Serial Number Register 1	$0E3_H$	235
SN2	Serial Number Register 2	$0E4_H$	235
SN3	Serial Number Register 3	$0E5_H$	236
CHIPID	Chip ID Register	$0E6_H$	236
RSSIRX	RSSI Readout Register	$0E7_H$	236
RSSIPMF	RSSI Peak Memory Filter Readout Register	$0E8_H$	237
SPWR	Signal Power Readout Register	$0E9_H$	237
NPWR	Noise Power Readout Register	$0EA_H$	238

Table 11 Registers Reset Values

Register Short Name	Register Long Name	Offset Address	Reset Value
Registers			
A_MID0	Message ID Register 0	000_H	00_H
A_MID1	Message ID Register 1	001_H	00_H
A_MID2	Message ID Register 2	002_H	00_H

Table 11 Registers Reset Values (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
A_MID3	Message ID Register 3	003_H	00_H
A_MID4	Message ID Register 4	004_H	00_H
A_MID5	Message ID Register 5	005_H	00_H
A_MID6	Message ID Register 6	006_H	00_H
A_MID7	Message ID Register 7	007_H	00_H
A_MID8	Message ID Register 8	008_H	00_H
A_MID9	Message ID Register 9	009_H	00_H
A_MID10	Message ID Register 10	$00A_H$	00_H
A_MID11	Message ID Register 11	$00B_H$	00_H
A_MID12	Message ID Register 12	$00C_H$	00_H
A_MID13	Message ID Register 13	$00D_H$	00_H
A_MID14	Message ID Register 14	$00E_H$	00_H
A_MID15	Message ID Register 15	$00F_H$	00_H
A_MID16	Message ID Register 16	010_H	00_H
A_MID17	Message ID Register 17	011_H	00_H
A_MID18	Message ID Register 18	012_H	00_H
A_MID19	Message ID Register 19	013_H	00_H
A_MIDC0	Message ID Control Register 0	014_H	00_H
A_MIDC1	Message ID Control Register 1	015_H	00_H
A_IF1	IF1 Register	016_H	$A3_H$
A_WUC	Wake-Up Control Register	017_H	04_H
A_WUPAT0	Wake-Up Pattern Register 0	018_H	00_H
A_WUPAT1	Wake-Up Pattern Register 1	019_H	00_H
A_WUBCNT	Wake-Up Bit or Chip Count Register	$01A_H$	00_H
A_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$01B_H$	00_H
A_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$01C_H$	FF_H
A_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$01D_H$	00_H
A_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$01E_H$	00_H
A_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$01F_H$	FF_H
A_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	020_H	00_H
A_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	021_H	00_H
A_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	022_H	FF_H
A_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	023_H	00_H
A_WURSSITH4	RSSI Wake-Up Threshold for Channel 4 Register	024_H	00_H

Table 11 Registers Reset Values (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
A_WURSSIBL4	RSSI Wake-Up Blocking Level Low Channel 4 Register	025_H	FF_H
A_WURSSIBH4	RSSI Wake-Up Blocking Level High Channel 4 Register	026_H	00_H
A_SRTHR	Signal Recognition Threshold Register	027_H	10_H
A_SIGDETSAT	Slicing Level Saturation Register	028_H	FF_H
A_WULOT	Wake-up on Level Observation Time Register	029_H	00_H
A_SYSRCTO	Synchronization Search Time-Out Register	$02A_H$	87_H
A_TOTIM0	Timeout Timer Register 0	$02B_H$	FF_H
A_TOTIM1	Timeout Timer Register 1	$02C_H$	$0F_H$
A_TOTIM_SYNC	SYNC Timeout Timer Register	$02D_H$	FF_H
A_TOTIM_TSI	TSI Timeout Timer Register	$02E_H$	00_H
A_TOTIM_EOM	EOM Timeout Timer Register	$02F_H$	00_H
A_AFCLIMIT	AFC Limit Configuration Register	030_H	02_H
A_AFCAGCADRD	AFC/AGC/ADR Freeze Delay Register	031_H	00_H
A_AFCSFCFG	AFC Start/Freeze Configuration Register	032_H	00_H
A_AFCKCFG0	AFC Integrators Gain Coefficients Register 0	033_H	00_H
A_AFCKCFG1	AFC Integrators Gain Coefficients Register 1	034_H	00_H
A_PMFUDSF	Peak Memory Filter Up-Down Factor Register	035_H	42_H
A_AGCSFCFG	AGC Start/Freeze Configuration Register	036_H	00_H
A_AGCCFG0	AGC Configuration Register 0	037_H	$0B_H$
A_AGCCFG1	AGC Configuration Register 1	038_H	$2F_H$
A_AGCTHR	AGC Threshold Register	039_H	08_H
A_DIGRXC	Digital Receiver Configuration Register	$03A_H$	40_H
A_PKBITPOS	RSSI Peak Detector Bit Position Register	$03B_H$	00_H
A_PDFMFC	PD Filter and Matched Filter Configuration Register	$03C_H$	77_H
A_PDECF	Pre Decimation Factor Register	$03D_H$	00_H
A_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$03E_H$	00_H
A_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$03F_H$	20_H
A_SRC	Sample Rate Converter	040_H	00_H
A_EXTSLC0	External Data Slicer Configuration Register 0	041_H	02_H
A_EXTSLC1	External Data Slicer Configuration Register 1	042_H	02_H
A_EXTSLC2	External Data Slicer Configuration Register 2	043_H	00_H
A_EXTSLTHR0	Externel Data Slicer BW Switching Threshold Register 0	044_H	00_H
A_EXTSLTHR1	Externel Data Slicer BW Switching Threshold Register 1	045_H	00_H
A_SIGDET0	Signal Detector Threshold Level Register - Run Mode	046_H	00_H

Table 11 Registers Reset Values (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
A_SIGDET1	Signal Detector Threshold Level Register - Wakeup	047_H	00_H
A_SIGDETLO	Signal Detector Threshold Low Level Register	048_H	00_H
A_SIGDETSEL	Signal Detector Range Selection Register	049_H	$7F_H$
A_SIGDETCFG	Signal Detector Configuration Register	$04A_H$	00_H
A_NDTHRES	FSK Noise Detector Threshold Register	$04B_H$	00_H
A_NDCONFIG	FSK Noise Detector Configuration Register	$04C_H$	07_H
A_CDRP	Clock and Data Recovery P Configuration Register	$04D_H$	$E6_H$
A_CDRI	Clock and Data Recovery Configuration Register	$04E_H$	45_H
A_CDRCFG0	CDR Configuration Register 0	$04F_H$	$4C_H$
A_CDRCFG1	CDR Configuration Register 1	050_H	$1E_H$
A_TVWIN	Timing Violation Window Register	051_H	28_H
A_SLCCFG	Slicer Configuration Register	052_H	90_H
A_TSIMODE	TSI Detection Mode Register	053_H	80_H
A_TSILENA	TSI Length Register A	054_H	00_H
A_TSILENB	TSI Length Register B	055_H	00_H
A_TSIGAP	TSI Gap Length Register	056_H	00_H
A_TSIPTA0	TSI Pattern Data Reference A Register 0	057_H	00_H
A_TSIPTA1	TSI Pattern Data Reference A Register 1	058_H	00_H
A_TSIPTB0	TSI Pattern Data Reference B Register 0	059_H	00_H
A_TSIPTB1	TSI Pattern Data Reference B Register 1	$05A_H$	00_H
A_EOMC	End Of Message Control Register	$05B_H$	05_H
A_EOMDLEN	EOM Data Length Limit Register	$05C_H$	00_H
A_EOMDLENP	EOM Data Length Limit Parallel Mode Register	$05D_H$	00_H
A_CHCFG	Channel Configuration Register	$05E_H$	00_H
A_TXRF	TX RF Configuration Register	$05F_H$	04_H
A_TXCFG	TX Configuration Regsiter	060_H	05_H
A_TXCHOFFS0	TX Channel Offset Register 0	061_H	00_H
A_TXCHOFFS1	TX Channel Offset Register 1	062_H	00_H
A_TXBDRDIV0	TX Baudrate Divider Register 0	063_H	00_H
A_TXBDRDIV1	TX Baudrate Divider Register 1	064_H	00_H
A_TXDSHCFG0	TX Data Shaping Configuration Register 0	065_H	00_H
A_TXDSHCFG1	TX Data Shaping Configuration Register 1	066_H	00_H
A_TXDSHCFG2	TX Data Shaping Configuration Register 2	067_H	00_H
A_TXPOWER0	TX Power Configuration Register 0	068_H	00_H
A_TXPOWER1	TX Power Configuration Register 1	069_H	00_H
A_TXFDEV	TX Frequency Deviation Register	$06A_H$	00_H
A_PLLINTC1	PLL MMD Integer Value Register Channel 1	$06B_H$	93_H

Table 11 Registers Reset Values (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
A_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$06C_H$	$F3_H$
A_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$06D_H$	07_H
A_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$06E_H$	09_H
A_PLLINTC2	PLL MMD Integer Value Register Channel 2	$06F_H$	13_H
A_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	070_H	$F3_H$
A_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	071_H	07_H
A_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	072_H	09_H
A_PLLINTC3	PLL MMD Integer Value Register Channel 3	073_H	13_H
A_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	074_H	$F3_H$
A_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	075_H	07_H
A_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	076_H	09_H
A_PLLINTC4	PLL MMD Integer Value Register Channel 4	077_H	13_H
A_PLLFRAC0C4	PLL Fractional Division Ratio Register 0 Channel 4	078_H	$F3_H$
A_PLLFRAC1C4	PLL Fractional Division Ratio Register 1 Channel 4	079_H	07_H
A_PLLFRAC2C4	PLL Fractional Division Ratio Register 2 Channel 4	$07A_H$	09_H
A_RXPLLBW	PLL Bandwidth Selection Register for RX Mode	$07B_H$	$0C_H$
A_TXPLLBW	PLL Bandwidth Selection Register for TX Mode	$07C_H$	27_H
A_PLLTST	PLL Startup Time Register	$07D_H$	$5B_H$
A_ANTSW	Antenna Switch Configuration Register	$07E_H$	22_H
A_ADRSFCFG	ADR Start/Freeze Configuration Register	$07F_H$	00_H
A_ADRTCFG0	ADR Timeout Configuration Register 0	080_H	40_H
A_ADRTCFG1	ADR Timeout Configuration Register 1	081_H	40_H
A_ADRTCFG2	ADR Timeout Configuration Register 2	082_H	00_H
A_ADRTHR0	ADR Threshold Register 0	083_H	05_H
A_ADRTHR1	ADR Threshold Register 1	084_H	84_H
SFRPAGE	Special Function Register Page Register	$0A0_H$	00_H
PPCFG0	PP0 and PP1 Configuration Register	$0A1_H$	50_H
PPCFG1	PP2 and PPRF Configuration Register	$0A2_H$	$F2_H$
PPCFG2	PPx Port Configuration Register	$0A3_H$	00_H
PPCFG3	PPRF_RSSI Configuration Register	$0A4_H$	$0F_H$
RXRUNCFG0	RX RUN Configuration Register 0	$0A5_H$	FF_H
RXRUNCFG1	RX RUN Configuration Register 1	$0A6_H$	FF_H
CLKOUT0	Clock Divider Register 0	$0A7_H$	$0B_H$
CLKOUT1	Clock Divider Register 1	$0A8_H$	00_H
CLKOUT2	Clock Divider Register 2	$0A9_H$	10_H
ANTSW	Antenna Switch Configuration Register	$0AA_H$	$1D_H$
RFC	RF Control Register	$0AB_H$	$E7_H$
XTALCAL0	XTAL Coarse Calibration Register	$0AE_H$	90_H

Table 11 Registers Reset Values (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
XTALCAL1	XTAL Fine Calibration Register	$0AF_H$	00_H
RSSICFG	RSSI Configuration Register	$0B0_H$	10_H
ADCINSEL	ADC Input Selection Register	$0B1_H$	00_H
RSSIOFFS	RSSI Offset Register	$0B2_H$	80_H
RSSISLOPE	RSSI Slope Register	$0B3_H$	80_H
DELOGSFT	DELOG Shift Register	$0B4_H$	00_H
CDRDRTHRP	CDR Data Rate Acceptance Positive Threshold Register	$0B5_H$	$1E_H$
CDRDRTHRN	CDR Data Rate Acceptance Negative Threshold Register	$0B6_H$	23_H
IM0	Interrupt Mask Register 0	$0B7_H$	00_H
IM1	Interrupt Mask Register 1	$0B8_H$	00_H
IM2	Interrupt Mask Register 2	$0B9_H$	00_H
SPMIP	Self Polling Mode Idle Periods Register	$0BA_H$	01_H
SPMC	Self Polling Mode Control Register	$0BB_H$	08_H
SPMRT	Self Polling Mode Reference Timer Register	$0BC_H$	01_H
SPMOFFT0	Self Polling Mode Off Time Register 0	$0BD_H$	01_H
SPMOFFT1	Self Polling Mode Off Time Register 1	$0BE_H$	00_H
SPMONTA0	Self Polling Mode On Time Config A Register 0	$0BF_H$	01_H
SPMONTA1	Self Polling Mode On Time Config A Register 1	$0C0_H$	00_H
SPMONTB0	Self Polling Mode On Time Config B Register 0	$0C1_H$	01_H
SPMONTB1	Self Polling Mode On Time Config B Register 1	$0C2_H$	00_H
SPMONTC0	Self Polling Mode On Time Config C Register 0	$0C3_H$	01_H
SPMONTC1	Self Polling Mode On Time Config C Register 1	$0C4_H$	00_H
SPMONTD0	Self Polling Mode On Time Config D Register 0	$0C5_H$	01_H
SPMONTD1	Self Polling Mode On Time Config D Register 1	$0C6_H$	00_H
EXTPCMD	External Processing Command Register	$0C7_H$	00_H
TXC	TX Control Register	$0C8_H$	01_H
RXC	RX Control Register	$0C9_H$	84_H
CMC	Chip Mode Control Register	$0CA_H$	10_H
TXCHNL	TX Channel Configuration Register	$0CB_H$	00_H
PLLCFG	PLL Configuration Register	$0CC_H$	28_H
VACERRTH	VCO Autocalibration Error Threshold	$0CD_H$	00_H
PRBS	PRBS Starting Value Register	$0CE_H$	50_H
TXFIFOAEL	TX FIFO Almost Empty Level Register	$0CF_H$	00_H
TXFIFOAFL	TX FIFO Almost Full Level Register	$0D0_H$	00_H
RXFIFOAFL	RX FIFO Almost Full Level Register	$0D1_H$	00_H
PLLSTAT	PLL Status Register	$0D2_H$	00_H
IS2	Interrupt Status Register 2	$0D3_H$	FF_H

Table 11 Registers Reset Values (cont'd)

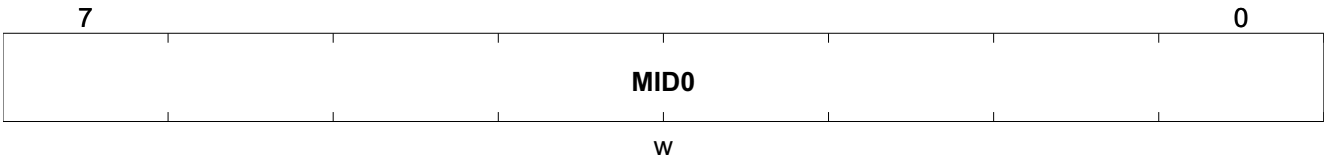
Register Short Name	Register Long Name	Offset Address	Reset Value
IS0	Interrupt Status Register 0	$0D4_H$	FF_H
IS1	Interrupt Status Register 1	$0D5_H$	FF_H
RFPLLACC	RF PLL Actual Channel and Configuration Register	$0D6_H$	00_H
RSSIPWU	Wakeup Peak Detector Readout Register	$0D7_H$	00_H
RSSIPRX	RSSI Peak Detector Readout Register	$0D8_H$	00_H
RSSIPPL	RSSI Payload Peak Detector Readout Register	$0D9_H$	00_H
PLDLEN	Payload Data Length Register	$0DA_H$	00_H
ADCRESH	ADC Result High Byte Register	$0DB_H$	00_H
ADCRESL	ADC Result Low Byte Register	$0DC_H$	00_H
AFCOFFSET	AFC Offset Read Register	$0DD_H$	00_H
AGCADRR	AGC and ADR Readout Register	$0DE_H$	00_H
SPIAT	SPI Address Tracer Register	$0DF_H$	00_H
SPIDT	SPI Data Tracer Register	$0E0_H$	00_H
SPICHKSUM	SPI Checksum Register	$0E1_H$	00_H
SN0	Serial Number Register 0	$0E2_H$	00_H
SN1	Serial Number Register 1	$0E3_H$	00_H
SN2	Serial Number Register 2	$0E4_H$	00_H
SN3	Serial Number Register 3	$0E5_H$	00_H
CHIPID	Chip ID Register	$0E6_H$	00_H
RSSIRX	RSSI Readout Register	$0E7_H$	00_H
RSSIPMF	RSSI Peak Memory Filter Readout Register	$0E8_H$	00_H
SPWR	Signal Power Readout Register	$0E9_H$	00_H
NPWR	Noise Power Readout Register	$0EA_H$	00_H

7 Registers

7.1 Registers

Message ID Register 0

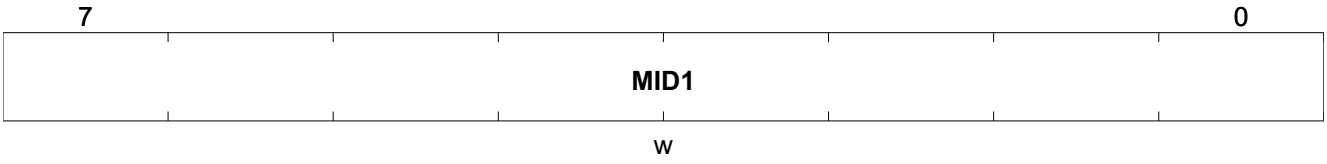
A_MID0 **Offset** **Reset Value**
Message ID Register 0 **000_H** **00_H**



Field	Bits	Type	Description
MID0	7:0	w	**Message ID Register 0** Reset: 00_H

Message ID Register 1

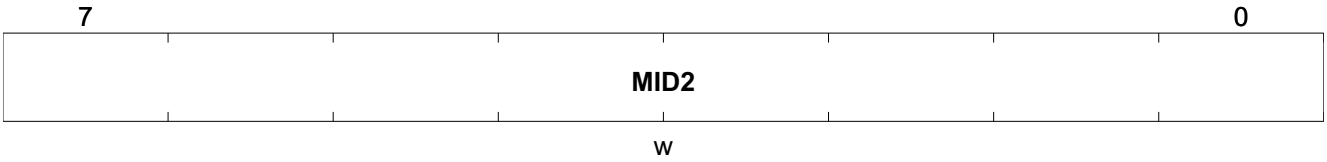
A_MID1 **Offset** **Reset Value**
Message ID Register 1 **001_H** **00_H**



Field	Bits	Type	Description
MID1	7:0	w	**Message ID Register 1** Reset: 00_H

Message ID Register 2

A_MID2 **Offset** **Reset Value**
Message ID Register 2 **002_H** **00_H**

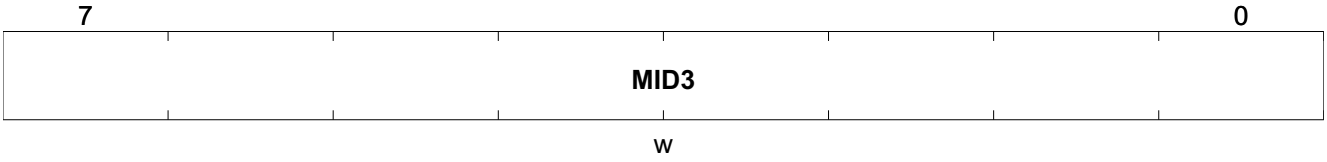


Field	Bits	Type	Description
MID2	7:0	w	**Message ID Register 2** Reset: 00_H

Message ID Register 3

A_MID3 **Offset** **Reset Value**

Message ID Register 3 **003_H** **00_H**

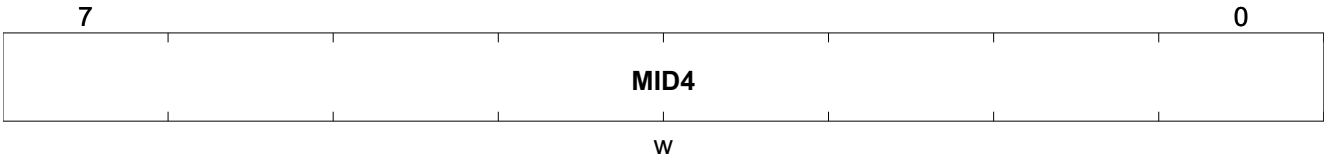


Field	Bits	Type	Description
MID3	7:0	w	**Message ID Register 3** Reset: 00_H

Message ID Register 4

A_MID4 **Offset** **Reset Value**

Message ID Register 4 **004_H** **00_H**

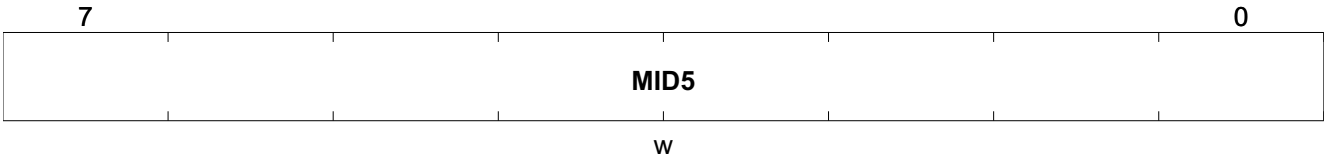


Field	Bits	Type	Description
MID4	7:0	w	**Message ID Register 4** Reset: 00_H

Message ID Register 5

A_MID5 **Offset** **Reset Value**

Message ID Register 5 **005_H** **00_H**

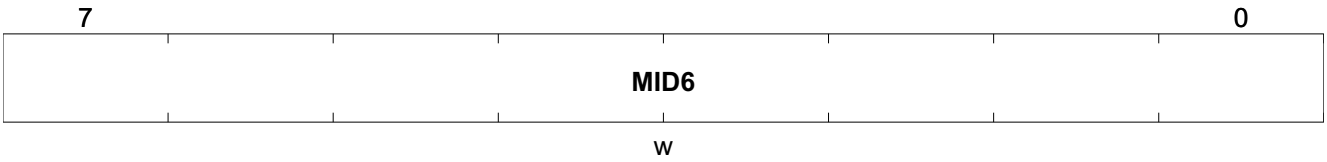


Field	Bits	Type	Description
MID5	7:0	w	**Message ID Register 5** Reset: 00_H

Message ID Register 6

A_MID6 **Offset** **Reset Value**

Message ID Register 6 **006_H** **00_H**

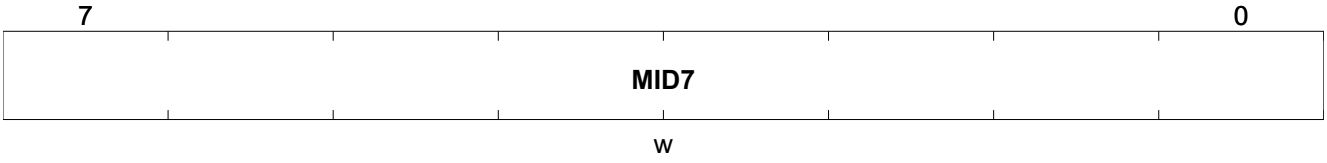


Field	Bits	Type	Description
MID6	7:0	w	**Message ID Register 6** Reset: 00_H

Message ID Register 7

A_MID7 **Offset** **Reset Value**

Message ID Register 7 **007_H** **00_H**

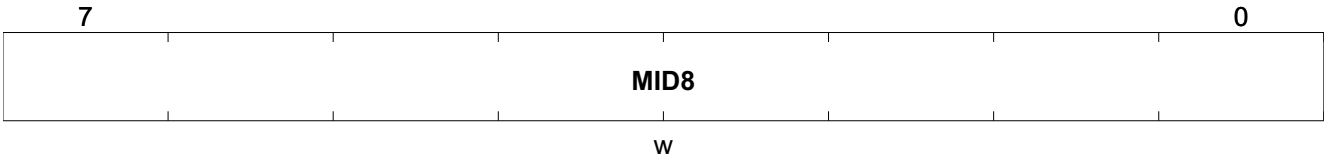


Field	Bits	Type	Description
MID7	7:0	w	**Message ID Register 7** Reset: 00_H

Message ID Register 8

A_MID8 **Offset** **Reset Value**

Message ID Register 8 **008_H** **00_H**

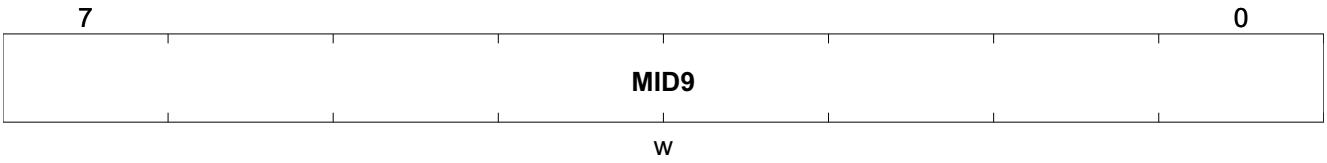


Field	Bits	Type	Description
MID8	7:0	w	**Message ID Register 8** Reset: 00_H

Message ID Register 9

A_MID9 **Offset** **Reset Value**

Message ID Register 9 **009_H** **00_H**

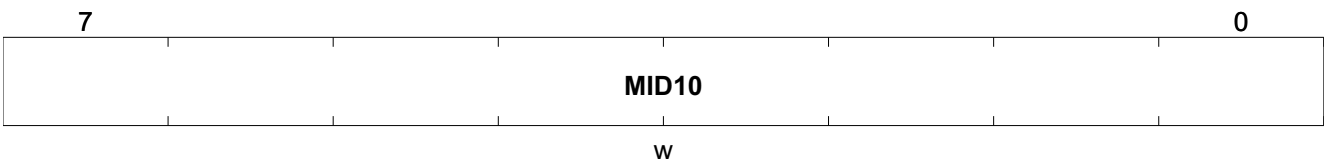


Field	Bits	Type	Description
MID9	7:0	w	**Message ID Register 9** Reset: 00_H

Message ID Register 10

A_MID10 **Offset** **Reset Value**

Message ID Register 10 **$00A_H$** **00_H**

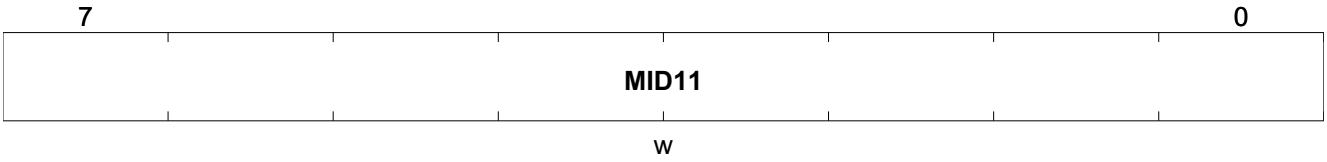


Field	Bits	Type	Description
MID10	7:0	w	**Message ID Register 10** Reset: 00_H

Message ID Register 11

A_MID11 **Offset** **Reset Value**

Message ID Register 11 **$00B_H$** **00_H**

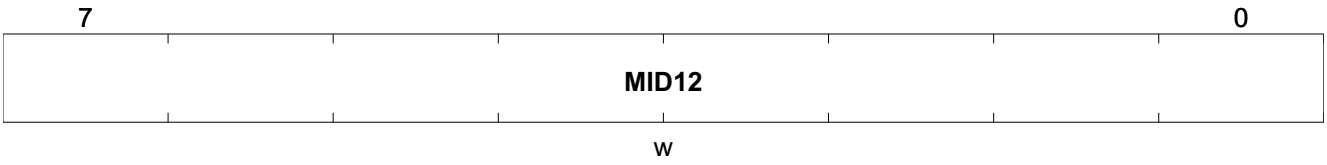


Field	Bits	Type	Description
MID11	7:0	w	**Message ID Register 11** Reset: 00_H

Message ID Register 12

A_MID12 **Offset** **Reset Value**

Message ID Register 12 **$00C_H$** **00_H**

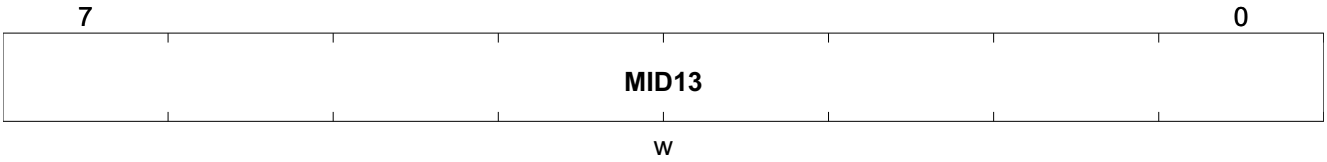


Field	Bits	Type	Description
MID12	7:0	w	**Message ID Register 12** Reset: 00_H

Message ID Register 13

A_MID13 **Offset** **Reset Value**

Message ID Register 13 **$00D_H$** **00_H**

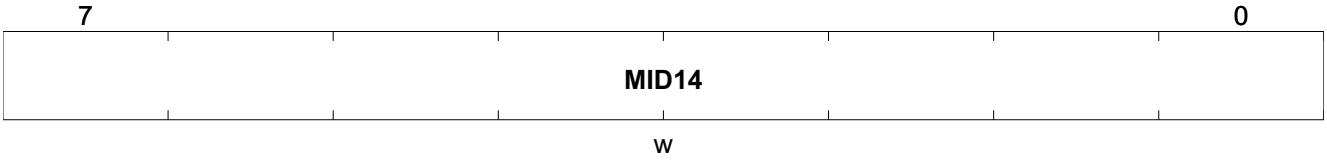


Field	Bits	Type	Description
MID13	7:0	w	**Message ID Register 13** Reset: 00_H

Message ID Register 14

A_MID14 **Offset** **Reset Value**

Message ID Register 14 **$00E_H$** **00_H**

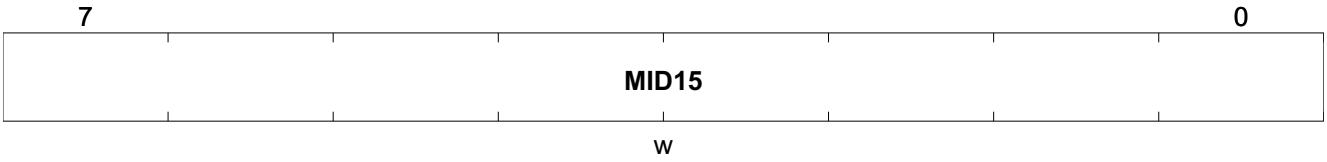


Field	Bits	Type	Description
MID14	7:0	w	**Message ID Register 14** Reset: 00_H

Message ID Register 15

A_MID15 **Offset** **Reset Value**

Message ID Register 15 **$00F_H$** **00_H**

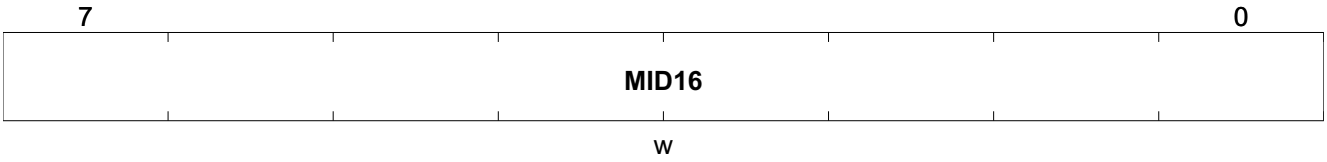


Field	Bits	Type	Description
MID15	7:0	w	**Message ID Register 15** Reset: 00_H

Message ID Register 16

A_MID16 **Offset** **Reset Value**

Message ID Register 16 **010_H** **00_H**

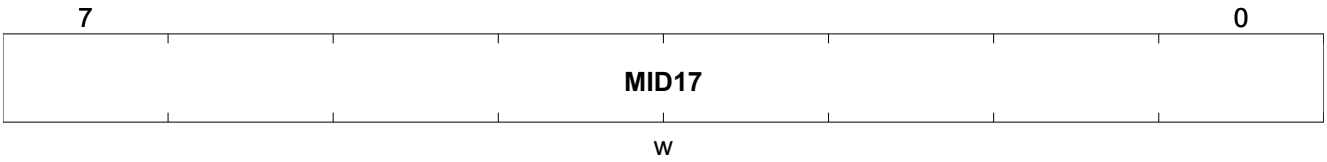


Field	Bits	Type	Description
MID16	7:0	w	**Message ID Register 16** Reset: 00_H

Message ID Register 17

A_MID17 **Offset** **Reset Value**

Message ID Register 17 **011_H** **00_H**

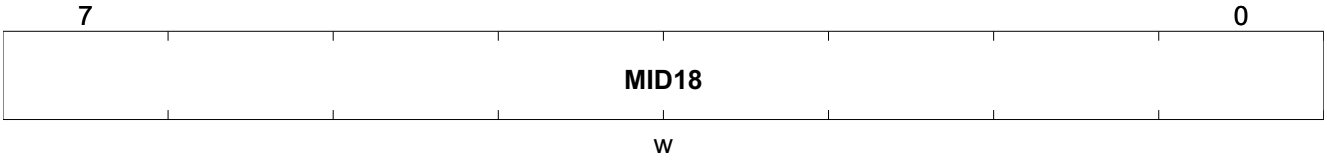


Field	Bits	Type	Description
MID17	7:0	w	**Message ID Register 17** Reset: 00_H

Message ID Register 18

A_MID18 **Offset** **Reset Value**

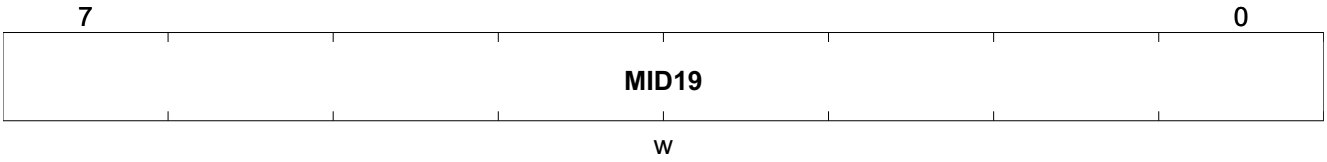
Message ID Register 18 **012_H** **00_H**



Field	Bits	Type	Description
MID18	7:0	w	**Message ID Register 18** Reset: 00_H

Message ID Register 19

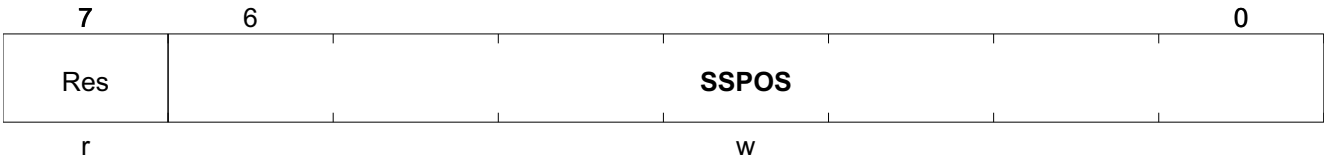
A_MID19	Offset	Reset Value
Message ID Register 19	013_H	00_H



Field	Bits	Type	Description
MID19	7:0	w	**Message ID Register 19** Reset: 00_H

Message ID Control Register 0

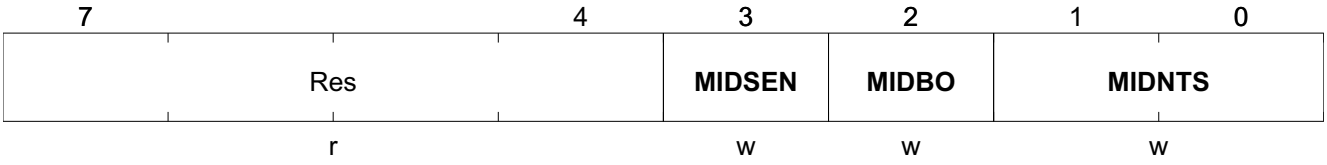
A_MIDC0	Offset	Reset Value
Message ID Control Register 0	014_H	00_H



Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H
SSPOS	6:0	w	**Message ID Scan Start Position** Min: 00h = Comparision starts one Bit after FSYNC Max: 7F = Comparision starts 128 Bits after FSYNC Reset: 00_H

Message ID Control Register 1

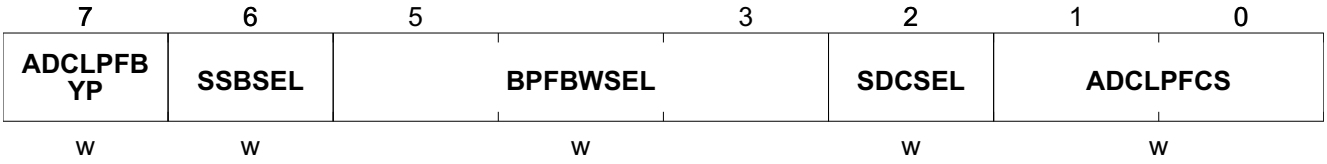
A_MIDC1	Offset	Reset Value
Message ID Control Register 1	015_H	00_H



Field	Bits	Type	Description
Res	7:4	r	**for future use** Reset: 0_H
MIDSEN	3	w	**Enable Message ID Screening** 0_B Disabled 1_B Enabled Reset: 0_H
MIDBO	2	w	**Message ID Byte Organisation** 0_B 2 Byte Mode 1_B 4 Byte Mode Reset: 0_H
MIDNTS	1:0	w	**Message ID Number of Bytes To Scan (4 Byte Mode / 2 Byte Mode)** 00_B 1 Byte to scan / 1 Byte to scan 01_B 2 Bytes to scan / 2 Bytes to scan 10_B 3 Bytes to scan / 2 Bytes to scan 11_B 4 Bytes to scan / 2 Bytes to scan Reset: 0_H

IF1 Register

A_IF1	Offset	Reset Value
IF1 Register	**016_H**	**$A3_H$**



Field	Bits	Type	Description
ADCLPFBYP	7	w	**ADC LPF bypass enable** 0_B Disabled 1_B Enabled Reset: 1_H
SSBSEL	6	w	**RXRF Receive Side Band Select** 0_B RF = LO + IF1 (Lo-side LO-injection) 1_B RF = LO - IF1 (Hi-side LO-injection) Reset: 0_H

Field	Bits	Type	Description
BPFBWSEL	5:3	w	**Band Pass Filter Bandwidth Selection** 000_B 50 kHz 001_B 80 kHz 010_B 125 kHz 011_B 200 kHz 100_B 300 kHz 101_B not used 110_B not used 111_B not used Reset: 4_H
SDCSEL	2	w	**Single / Double Conversion Selection** 0_B Double Conversion (10.7 MHz/274 kHz) 1_B Single Conversion (274 kHz) Reset: 0_H
ADCLPFCS	1:0	w	**ADC LPF Corner Frequency Selection** 00_B 2,144 kHz 01_B 4,511 kHz 10_B 10,063 kHz 11_B 26,165 kHz Reset: 3_H

Wake-Up Control Register

A_WUC	Offset	Reset Value
Wake-Up Control Register	**017_H**	**04_H**

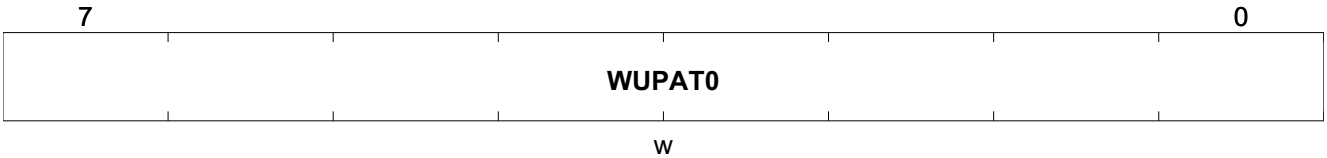
7	6	5	4	3	2	0
Res	**PWUEN**	**WUPMSEL**	**WULCUFFB**	**UFFBLCOO**	**WUCRT**	
r	w	w	w	w	w	

Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H
PWUEN	6	w	**Parallel Wake Up Mode Enable** This feature can only be used, when modulation type is the same for SPM and RMSP 0_B Disabled 1_B Enabled Reset: 0_H
WUPMSEL	5	w	**Wake Up Pattern Mode Selection** 0_B Chip mode 1_B Bit mode Reset: 0_H

Field	Bits	Type	Description
WULCUFFB	4	w	**Select a "Wake Up on Level Criterion", when UFFBLCOO is enabled.** 0_B RSSI automatically selected, when A_CHCFG.EXTPROC = "10" 1_B Signal Recognition Reset: 0_H
UFFBLCOO	3	w	**Ultrafast Fall Back to SLEEP or additional Level criterion in Constant On Off.** Enables additional parallel processing of "Level Criterion", when a "Data Criterion" is selected in WUCRT. In case of Fast Fall Back to SLEEP or Permanent Wake-Up Search, this mode is called UFFB (Ultrafast Fall Back). The same mode can be used in Constant On-Off. 0_B Disabled 1_B Enabled Reset: 0_H
WUCRT	2:0	w	**Select a "Wake Up Criterion"** 000_B Pattern Detection (Data Criterion) When A_CHCFG.EXTROC = "01" this setting is mapped to 3_H 001_B Random Bits (Data Criterion) When A_CHCFG.EXTROC = "01" this setting is mapped to 3_H 010_B Equal Bits (Data Criterion) When A_CHCFG.EXTROC = "01" this setting is mapped to 3_H 011_B Wake Up on Symbol Sync, Valid Data Rate (Data Criterion); The A_WUBCNT Register is not used in this mode 100_B RSSI (Level Criterion) automatically selected, when A_CHCFG.EXTPROC = "10" 101_B Signal Recognition (Level Criterion) 110_B Equal Zero Bits for Bi-phase encodings (Data Criterion) When A_CHCFG.EXTROC = "01" this setting is mapped to 3_H 111_B Equal One Bits for Bi-phase encodings (Data Criterion) When A_CHCFG.EXTROC = "01" this setting is mapped to 3_H Reset: 4_H

Wake-Up Pattern Register 0

A_WUPAT0	Offset	Reset Value
Wake-Up Pattern Register 0	**018_H**	**00_H**

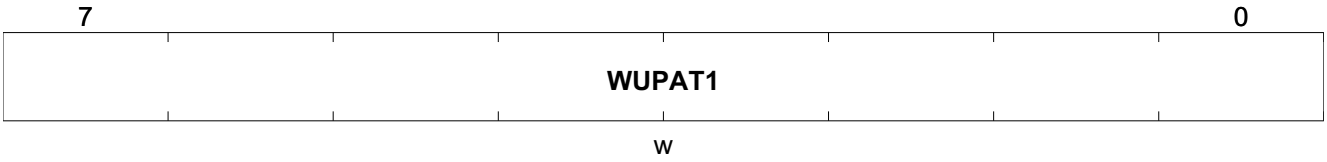


Field	Bits	Type	Description
WUPAT0	7:0	w	**Wake Up Detection Pattern: Bit 7...Bit 0(LSB) (in Bits/Chips)** Reset: 00_H

Wake-Up Pattern Register 1

A_WUPAT1 **Offset** **Reset Value**

Wake-Up Pattern Register 1 **019_H** **00_H**

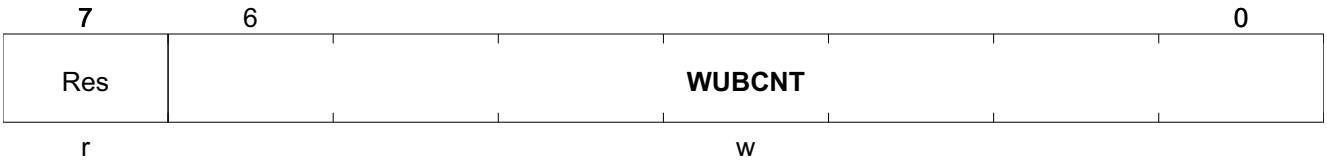


Field	Bits	Type	Description
WUPAT1	7:0	w	**Wake Up Detection Pattern: (MSB) Bit 15...Bit 8 (in Bits/Chips)** Reset: 00_H

Wake-Up Bit or Chip Count Register

A_WUBCNT **Offset** **Reset Value**

Wake-Up Bit or Chip Count Register **$01A_H$** **00_H**

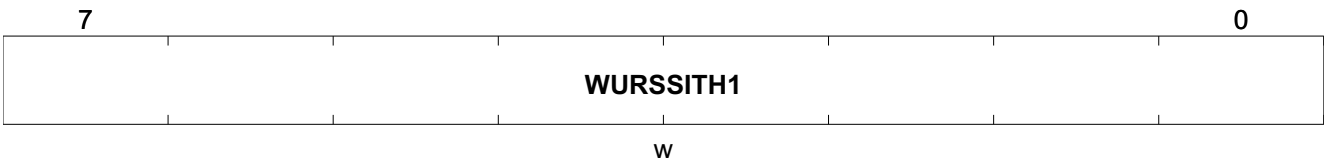


Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H

Field	Bits	Type	Description
WUBCNT	6:0	w	**Wake Up Bit/Chip Count Register (unit is bits; only exception is WU Pattern Chip Mode, where unit is chips, see A_WUC.WUPMSEL)** Counter Register to define the maximum counts of bits/chips for Wake Up detection. Min: 00h = 0 Bits/Chips to count In â€œRandom Bitsâ€? or â€œEqual Bitsâ€? Mode this will cause a Wake Up on Data Criterion immediately after Symbol Synchronization is found. In â€œPattern Detectionâ€? Mode this will cause no Wake Up on Data Criterion. In this Mode there is needed minimum 11h = 17 Bits/Chips to shift one Pattern through the whole Pattern Detector. Because comparision can only be started when at least the comparision register is completely filled. Max: 7Fh: 127 Bits/Chips to count after Symbol Sync found Reset: 00_H

RSSI Wake-Up Threshold for Channel 1 Register

A_WURSSITH1	Offset	Reset Value
RSSI Wake-Up Threshold for Channel 1 Register	**$01B_H$**	**00_H**



Field	Bits	Type	Description
WURSSITH1	7:0	w	**Wake Up on RSSI Threshold level for Channel 1** Wake Up Request generated when actual RSSI level is above this threshold Reset: 00_H

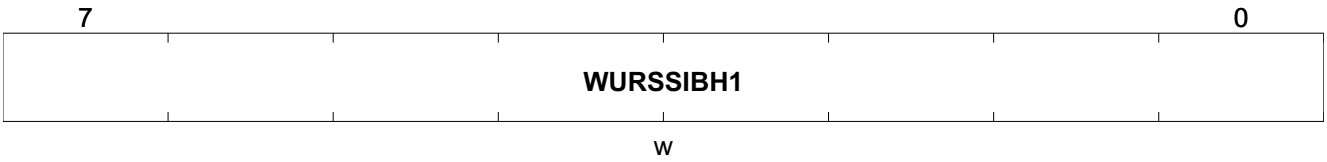
RSSI Wake-Up Blocking Level Low Channel 1 Register

A_WURSSIBL1	Offset	Reset Value
RSSI Wake-Up Blocking Level Low Channel 1 Register	**$01C_H$**	**FF_H**

Field	Bits	Type	Description
WURSSIBL1	7:0	w	**Wake Up on RSSI Blocking Level LOW for Channel 1** Reset: FF_H

RSSI Wake-Up Blocking Level High Channel 1 Register

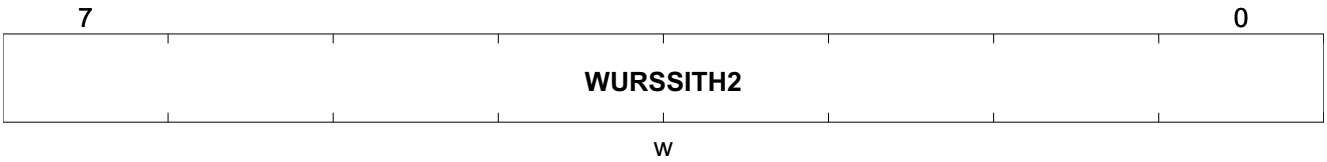
A_WURSSIBH1	Offset	Reset Value
RSSI Wake-Up Blocking Level High Channel 1 Register	**$01D_H$**	**00_H**



Field	Bits	Type	Description
WURSSIBH1	7:0	w	**Wake Up on RSSI Blocking Level HIGH for Channel 1, when RSSI is selected as WU criterion or FFB criterion.** Reset: 00_H

RSSI Wake-Up Threshold for Channel 2 Register

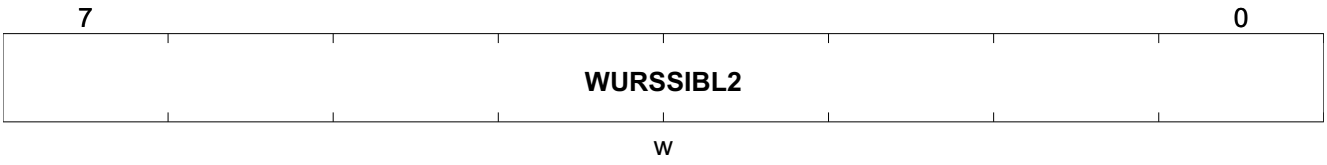
A_WURSSITH2	Offset	Reset Value
RSSI Wake-Up Threshold for Channel 2 Register	**$01E_H$**	**00_H**



Field	Bits	Type	Description
WURSSITH2	7:0	w	**Wake Up on RSSI Threshold level for Channel 2** Wake Up Request generated when actual RSSI level is above this threshold Reset: 00_H

RSSI Wake-Up Blocking Level Low Channel 2 Register

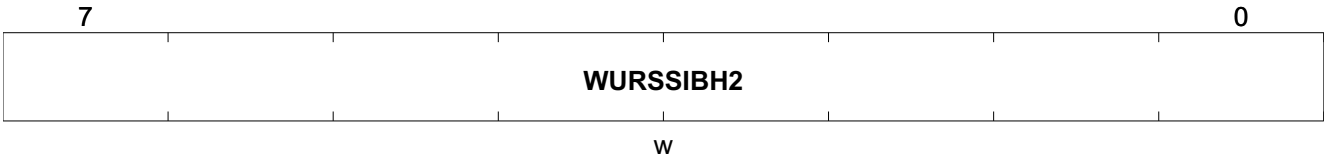
A_WURSSIBL2	Offset	Reset Value
RSSI Wake-Up Blocking Level Low Channel 2 Register	**$01F_H$**	**FF_H**



Field	Bits	Type	Description
WURSSIBL2	7:0	w	**Wake Up on RSSI Blocking Level LOW for Channel 2** Reset: FF_H

RSSI Wake-Up Blocking Level High Channel 2 Register

A_WURSSIBH2	Offset	Reset Value
RSSI Wake-Up Blocking Level High Channel 2 Register	**020_H**	**00_H**

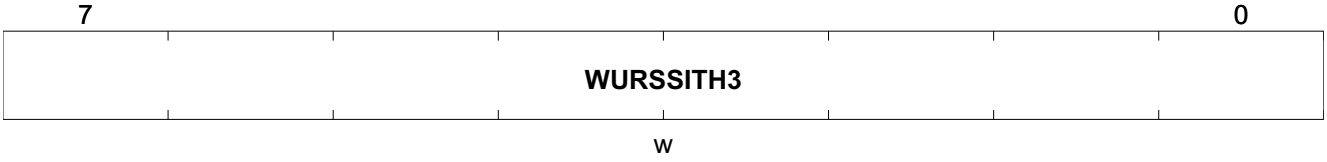


Field	Bits	Type	Description
WURSSIBH2	7:0	w	**Wake Up on RSSI Blocking Level HIGH for Channel 2, when RSSI is selected as WU criterion or FFB criterion.** Reset: 00_H

RSSI Wake-Up Threshold for Channel 3 Register

A_WURSSITH3 **Offset** **Reset Value**

RSSI Wake-Up Threshold for Channel 3 Register **021_H** **00_H**

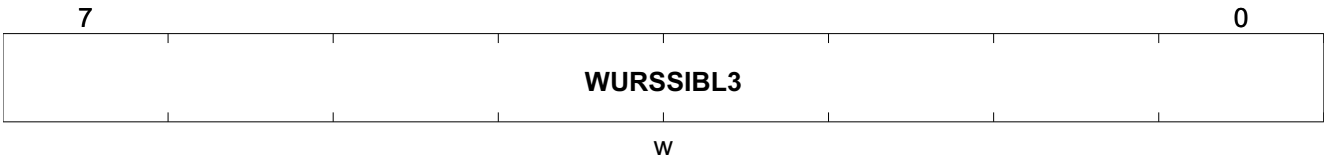


Field	Bits	Type	Description
WURSSITH3	7:0	w	**Wake Up on RSSI Threshold level for Channel 3** Wake Up Request generated when actual RSSI level is above this threshold Reset: 00_H

RSSI Wake-Up Blocking Level Low Channel 3 Register

A_WURSSIBL3 **Offset** **Reset Value**

RSSI Wake-Up Blocking Level Low Channel 3 Register **022_H** **FF_H**

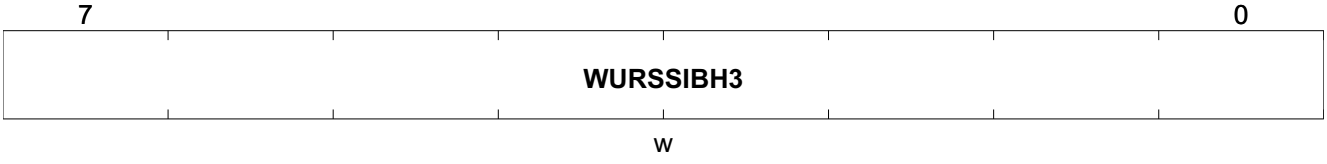


Field	Bits	Type	Description
WURSSIBL3	7:0	w	**Wake Up on RSSI Blocking Level LOW for Channel 3** Reset: FF_H

RSSI Wake-Up Blocking Level High Channel 3 Register

A_WURSSIBH3 **Offset** **Reset Value**

RSSI Wake-Up Blocking Level High Channel 3 Register **023_H** **00_H**



Field	Bits	Type	Description
WURSSIBH3	7:0	w	**Wake Up on RSSI Blocking Level HIGH for Channel 3, when RSSI is selected as WU criterion or FFB criterion.** Reset: 00_H

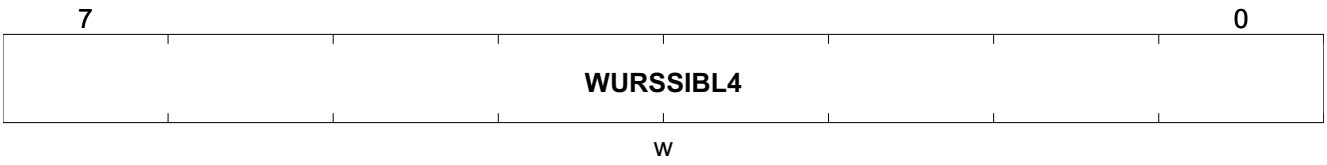
RSSI Wake-Up Threshold for Channel 4 Register

A_WURSSITH4	Offset	Reset Value
RSSI Wake-Up Threshold for Channel 4 Register	**024_H**	**00_H**

Field	Bits	Type	Description
WURSSITH4	7:0	w	**Wake Up on RSSI Threshold level for Channel 4** Wake Up Request generated when actual RSSI level is above this threshold Reset: 00_H

RSSI Wake-Up Blocking Level Low Channel 4 Register

A_WURSSIBL4	Offset	Reset Value
RSSI Wake-Up Blocking Level Low Channel 4 Register	**025_H**	**FF_H**



Field	Bits	Type	Description
WURSSIBL4	7:0	w	**Wake Up on RSSI Blocking Level LOW for Channel 4** Reset: FF_H

RSSI Wake-Up Blocking Level High Channel 4 Register

A_WURSSIBH4	Offset	Reset Value
RSSI Wake-Up Blocking Level High Channel 4 Register	026_H	00_H

7							0
WURSSIBH4							
w							

Field	Bits	Type	Description
WURSSIBH4	7:0	w	**Wake Up on RSSI Blocking Level HIGH for Channel 4, when RSSI is selected as WU criterion or FFB criterion.** Reset: 00_H

Signal Recognition Threshold Register

A_SRTHR	Offset	Reset Value
Signal Recognition Threshold Register	027_H	10_H

7							0
SRTHR							
w							

Field	Bits	Type	Description
SRTHR	7:0	w	**In case of Signal Recognition as WU criterion or FFB criterion, the register defines the minimum consecutive T/16 samples of the Signal Recognition output to be at high level for a positive wake up event generation or FFB generation** Reset: 10_H

Slicing Level Saturation Register

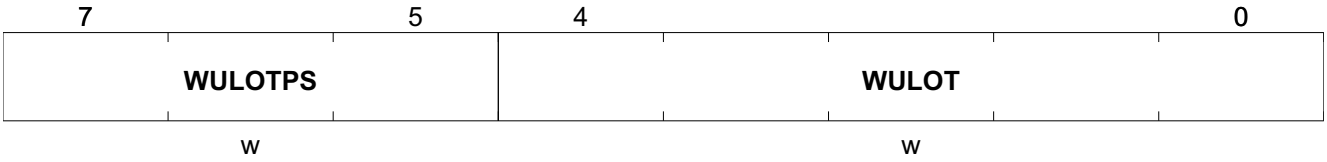
A_SIGDETSAT	Offset	Reset Value
Slicing Level Saturation Register	028_H	FF_H

7							0
SIGDETSAT							
w							

Field	Bits	Type	Description
SIGDETSAT	7:0	w	**Saturation limit of the data slicing level** Reset: FF_H

Wake-up on Level Observation Time Register

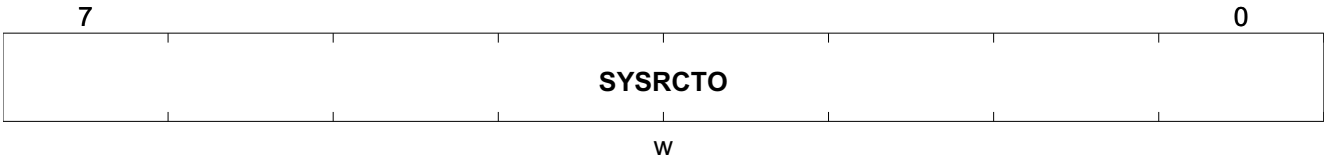
A_WULOT	Offset	Reset Value
Wake-up on Level Observation Time Register	**029_H**	**00_H**



Field	Bits	Type	Description
WULOTPS	7:5	w	**Wake-Up Level Observation Time PreScaler** 000_B 4 001_B 8 010_B 16 011_B 32 100_B 64 101_B 128 110_B 256 111_B 512 Reset: 0_H
WULOT	4:0	w	**Wake-Up Level Observation Time** Min. 01h : Twulot = 1 * WULOTPS * 64 / Fsys Max 1Fh : Twulot = 31 * WULOTPS * 64 / Fsys Value 00h : Twulot = 32 * WULOTPS * 64 / Fsys Reset: 00_H

Synchronization Search Time-Out Register

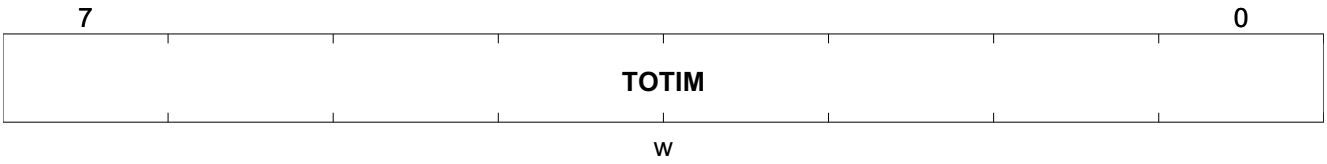
A_SYSRCTO	Offset	Reset Value
Synchronization Search Time-Out Register	**$02A_H$**	**87_H**



Field	Bits	Type	Description
SYSRCTO	7:0	w	**Synchronization search time out** FFh: 15 15/16 bit 00h: 0 bit Reset: 87_H

Timeout Timer Register 0

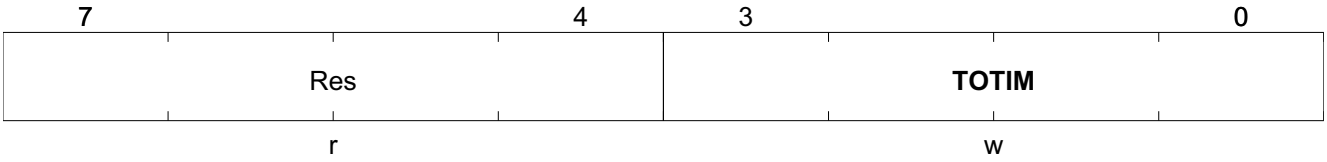
A_TOTIM0	Offset	Reset Value
Timeout Timer Register 0	**$02B_H$**	**FF_H**



Field	Bits	Type	Description
TOTIM	7:0	w	**Set value of Time-Out Timer** Timer is used to get back from Run Mode Self Polling to the Self Polling Timer is set back at new cycle start of Run Mode Self Polling. TimeOut= (TOTIM * 64 * 512) / fsys Min: 001h = (1 * 64 * 512)/ fsys Max: FFFh= (4095 * 64 * 512) / fsys 00h: disabled Reset: FF_H

Timeout Timer Register 1

A_TOTIM1	Offset	Reset Value
Timeout Timer Register 1	**$02C_H$**	**$0F_H$**

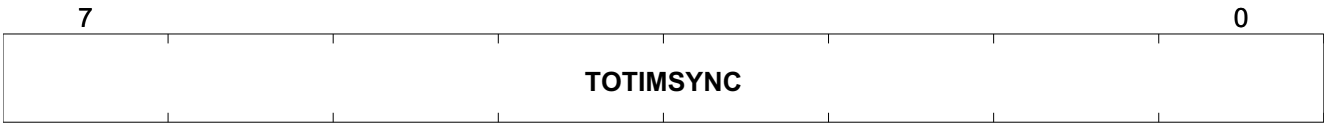


Field	Bits	Type	Description
Res	7:4	r	**for future use** Reset: 0_H

Field	Bits	Type	Description
TOTIM	3:0	w	**Set value of Time-Out Timer** Timer is used to get back from Run Mode Self Polling to the Self Polling Timer is set back at new cycle start of Run Mode Self Polling. TimeOut= (TOTIM * 64 * 512) / fsys Min: 001h = (1 * 64 * 512)/ fsys Max: FFFh= (4095 * 64 * 512) / fsys 00h: disabled Reset: F_H

SYNC Timeout Timer Register

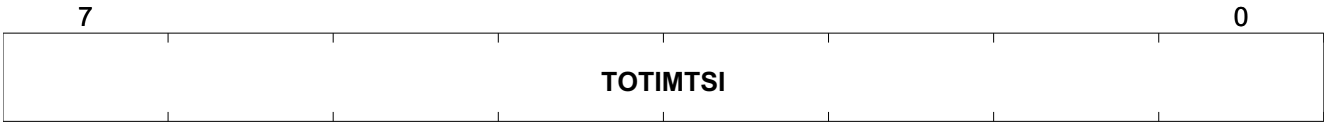
A_TOTIM_SYNC	Offset	Reset Value
SYNC Timeout Timer Register	$02D_H$	FF_H



Field	Bits	Type	Description
TOTIMSYNC	7:0	w	**Set value of Time-Out Timer (Symbol Synchronization)** Timer is used to get back from Run Mode Self Polling to the Self Polling Mode whenever there is no Symbol Synchronization. Timer is set back at new cycle start of Run Mode Self Polling. TimeOut= (TOTIMSYNC * 64 * 512) / fsys Min: 01h = (1 * 64 * 512)/ fsys Max: FFh= (255 * 64 * 512) / fsys 00h: disabled Reset: FF_H

TSI Timeout Timer Register

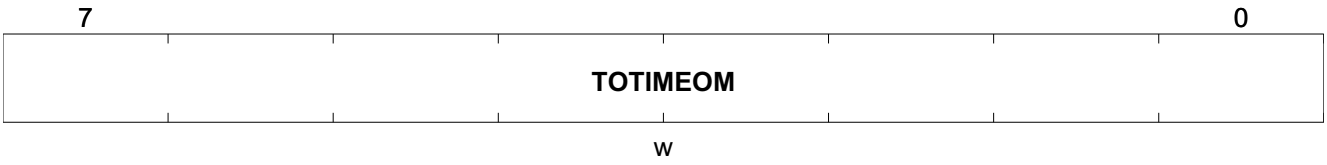
A_TOTIM_TSI	Offset	Reset Value
TSI Timeout Timer Register	$02E_H$	00_H



Field	Bits	Type	Description
TOTIMTSI	7:0	w	**Set value of Time-Out Timer (Telegram Start Identifier)** Timer is used to get back from Run Mode Self Polling to the Self Polling Mode whenever a Symbol Synchronisation is available but there is no TSI detected. Timer is set back at new cycle start of Run Mode Self Polling. TimeOut= (TOTIMTSI * 64 * 512) / fsys Min: 01h = (1 * 64 * 512)/ fsys Max: FFh= (255 * 64 * 512) / fsys 00h: disabled Reset: 00_H

EOM Timeout Timer Register

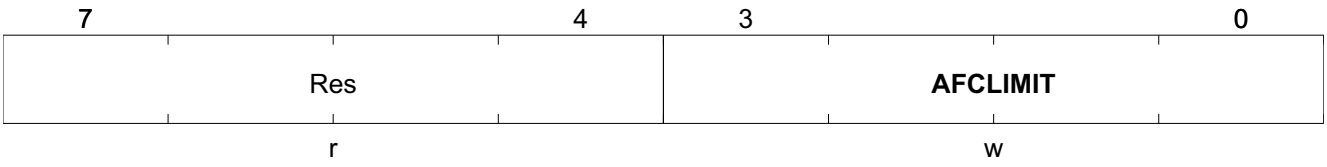
A_TOTIM_EOM	Offset	Reset Value
EOM Timeout Timer Register	**$02F_H$**	**00_H**



Field	Bits	Type	Description
TOTIMEOM	7:0	w	**Set value of Time-Out Timer (End of Message)** Timer is used to get back from Run Mode Self Polling to the Self Polling Mode whenever a TSI has been detected but there is no EOM detected. Timer is set back at new cycle start of Run Mode Self Polling. TimeOut= (TOTIMEOM * 64 * 512 * 2) / fsys Min: 01h = (1 * 64 * 512 * 2)/ fsys Max: FFh= (255 * 64 * 512 * 2) / fsys 00h: disabled Reset: 00_H

AFC Limit Configuration Register

A_AFCLIMIT	Offset	Reset Value
AFC Limit Configuration Register	**030_H**	**02_H**



Field	Bits	Type	Description
Res	7:4	r	**for future use** Reset: 0_H
AFCLIMIT	3:0	w	**AFC Frequency Offset Saturation Limit ==> 1...16 x 10.7 kHz** Min: 0h = +/- Fsys / 2^11 Hz Max: Fh = +/- 16 * Fsys / 2^11 Hz Reset: 2_H

AFC/AGC/ADR Freeze Delay Register

A_AFCAGCADRD	Offset	Reset Value
AFC/AGC/ADR Freeze Delay Register	**031_H**	**00_H**

7	6	5	4	3	2	1	0
AFCAGCADRD							
w							

Field	Bits	Type	Description
AFCAGCADRD	7:0	w	**AFC/AGC/ADR Freeze Delay Counter Division Ratio** The base period for the delay counter is the 8-16 samples/chip (matched filter input strobe) divided by 4 Reset: 00_H

AFC Start/Freeze Configuration Register

A_AFCSFCFG	Offset	Reset Value
AFC Start/Freeze Configuration Register	**032_H**	**00_H**

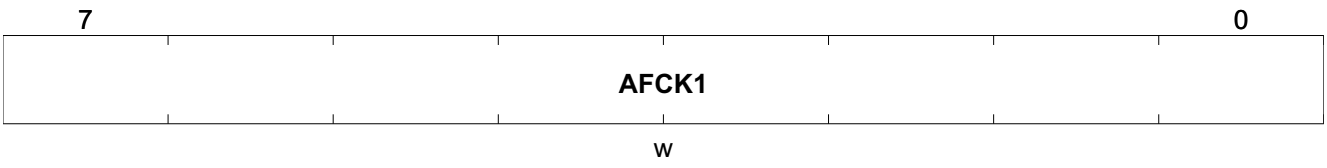
7	6	5	4	3	2	1	0
AFCBLASK	AFCRESATCC	AFCUNFREEZE		AFCFREEZE		AFCSTART	
w	w	w		w		w	

Field	Bits	Type	Description
AFCBLASK	7	w	**AFC blocking during a low phase in the ASK signal** 0_B Disabled 1_B Enabled Reset: 0_H

Field	Bits	Type	Description
AFCRESATCC	6	w	**Enable AFC Restart at Channel Change and at the beginning of the current configuration in Self Polling Mode** and at leaving the HOLD state (when bit CMC0.INITPLLHOLD is set) in Run Mode Slave 0_B Disabled 1_B Enabled Reset: 0_H
AFCUNFREEZE	5:4	w	**AFC Unfreeze Configuration** 00_B No Unfreeze 01_B Unfreeze on NOT RSSI Event 10_B Unfreeze on NOT Signal Recognition Event 11_B Unfreeze on NOT Symbol Synchronization Reset: 0_H
AFCFREEZE	3:2	w	**AFC Freeze Configuration** 00_B Stay ON 01_B Freeze on RSSI Event + Delay (AFCAGCDEL) 10_B Freeze on Signal Recognition Event + Delay (AFCAGCDEL) 11_B Freeze on Symbol Synchronization + Delay (AFCAGCDEL) Reset: 0_H
AFCSTART	1:0	w	**AFC Start Configuration** 00_B OFF 01_B Direct ON 10_B Start on RSSI event 11_B Start on Signal Recognition event Reset: 0_H

AFC Integrators Gain Coefficients Register 0

A_AFCKCFG0	Offset	Reset Value
AFC Integrators Gain Coefficients Register 0	**033_H**	**00_H**



Field	Bits	Type	Description
AFCK1	7:0	w	**AFC Filter coefficient K1 (bits 7:0)** K1 = AFCK1 Reset: 00_H

AFC Integrators Gain Coefficients Register 1

A_AFCKCFG1	Offset	Reset Value
AFC Integrators Gain Coefficients Register 1	034_H	00_H

7	5	4	0
AFCK2SEL		AFCK1	
w		w	

Field	Bits	Type	Description
AFCK2SEL	7:5	w	**AFC Filter coefficient K2 division factor selection** K2 = K1 * y(AFCK2SEL) 000_B y = 1 001_B y = 1/2 010_B y = 1/3 011_B y = 1/4 100_B y = 1/5.6 101_B y = 1/7.1 110_B y = 1/9 111_B y = 1/11 Reset: 0_H
AFCK1	4:0	w	**AFC Filter coefficient K1 (bits 12:8)** K1 = AFCK1 Reset: 00_H

Peak Memory Filter Up-Down Factor Register

A_PMFUDSF	Offset	Reset Value
Peak Memory Filter Up-Down Factor Register	035_H	42_H

7	6	4	3	2	0
Res	PMFUP		Res	PMFDN	
r	w		r	w	

Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H

Field	Bits	Type	Description
PMFUP	6:4	w	**Peak Memory Filter Attack (Up) Factor** 000_B 2^-1 001_B 2^-2 010_B 2^-3 011_B 2^-4 100_B 2^-5 101_B 2^-6 110_B 2^-7 111_B 2^-8 Reset: 4_H
Res	3	r	**for future use** Reset: 0_H
PMFDN	2:0	w	**Peak Memory Filter Decay (Down) Factor (additional to Attack Factor)** 000_B 2^-2 001_B 2^-3 010_B 2^-4 011_B 2^-5 100_B 2^-6 101_B 2^-7 110_B 2^-8 111_B 2^-9 Reset: 2_H

AGC Start/Freeze Configuration Register

A_AGCSFCFG	Offset	Reset Value
AGC Start/Freeze Configuration Register	**036_H**	**00_H**

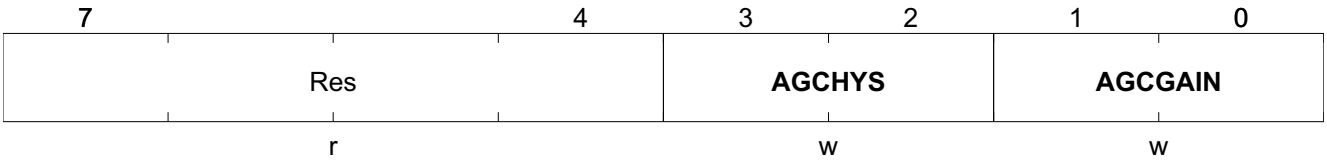
7	6	5	4	3	2	1	0
Res	AGCRESATCC	AGCUNFREEZE		AGCFREEZE		AGCSTART	
r	w	w		w		w	

Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H
AGCRESATCC	6	w	**Enable AGC Restart at Channel Change and at the beginning of the current configuration in Self Polling Mode** and at leaving the HOLD state (when bit CMC0.INITPLLHOLD is set) in Run Mode Slave 0_B Disabled 1_B Enabled Reset: 0_H

Field	Bits	Type	Description
AGCUNFREEZE	5:4	w	**AGC Unfreeze Configuration** 00_B No Unfreeze 01_B Unfreeze on NOT RSSI Event 10_B Unfreeze on NOT Signal Recognition Event 11_B Unfreeze on NOT Symbol Synchronization Reset: 0_H
AGCFREEZE	3:2	w	**AGC Freeze Configuration** 00_B Stay ON 01_B Freeze on RSSI Event + Delay (AFCAGCDEL) 10_B Freeze on Signal Recognition Event + Delay (AFCAGCDEL) 11_B Freeze on Symbol Synchronization + Delay (AFCAGCDEL) Reset: 0_H
AGCSTART	1:0	w	**AGC Start Configuration** 00_B OFF 01_B Direct ON 10_B Start on RSSI event 11_B Start on Signal Recognition event Reset: 0_H

AGC Configuration Register 0

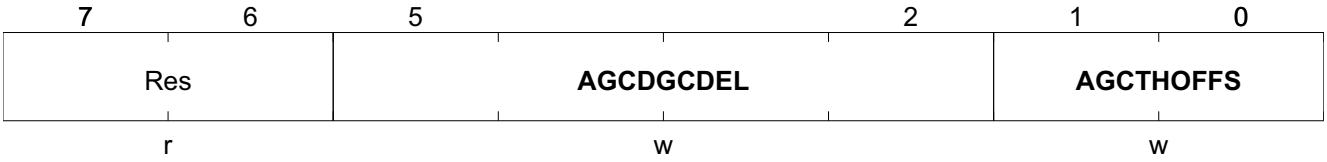
A_AGCCFG0	Offset	Reset Value
AGC Configuration Register 0	**037_H**	**$0B_H$**



Field	Bits	Type	Description
Res	7:4	r	**for future use** Reset: 0_H
AGCHYS	3:2	w	**AGC Threshold Hysteresis** 00_B 12.8 dB 01_B 17.1 dB 10_B 21.3 dB 11_B 25.6 dB Reset: 2_H
AGCGAIN	1:0	w	**AGC Gain Control** 00_B 0 dB 01_B -15 dB 10_B -30 dB 11_B Automatic Reset: 3_H

AGC Configuration Register 1

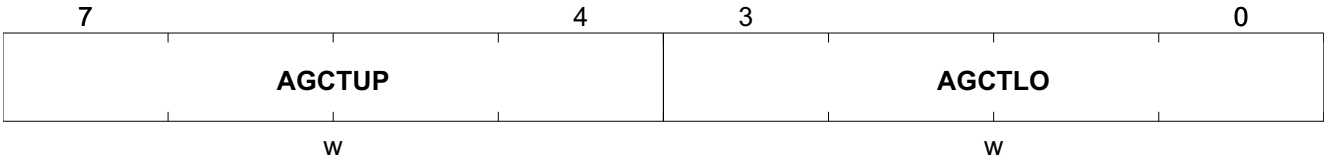
A_AGCCFG1	Offset	Reset Value
AGC Configuration Register 1	038_H	$2F_H$



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
AGCDGCDEL	5:2	w	**AGC Digital Gain delay in Fsys/80 samples** Reset: B_H
AGCTHOFFS	1:0	w	**AGC Threshold Offset** 00_B 25.5 dB 01_B 38.3 dB 10_B 51.1 dB 11_B 63.9 dB Reset: 3_H

AGC Threshold Register

A_AGCTHR	Offset	Reset Value
AGC Threshold Register	039_H	08_H



Field	Bits	Type	Description
AGCTUP	7:4	w	**AGC Upper Attack Threshold [dB]** AGC Upper Threshold = A_AGCCFG1.AGCTHOFFS + 25.6 + AGCTUP*1.6 Reset: 0_H
AGCTLO	3:0	w	**AGC Lower Attack Threshold [dB]** AGC Lower Threshold = A_AGCCFG1.AGCTHOFFS + AGCTLO*1.6 Reset: 8_H

Digital Receiver Configuration Register

A_DIGRXC	Offset	Reset Value
Digital Receiver Configuration Register	$03A_H$	40_H

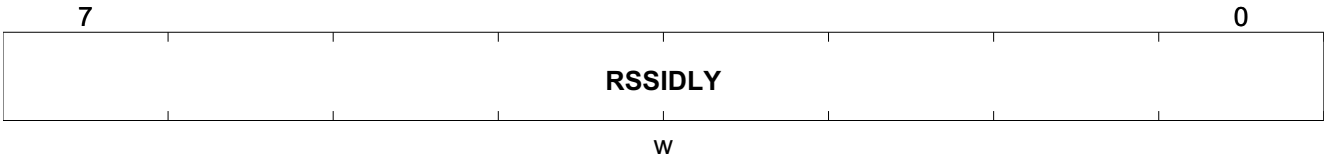
7	6	5	4	3	2	1	0
INITDRXES	INITFRCS	CODE		CHIPDINV	DINVEXT	AAFBYP	AAFFCSEL
w	w	w		w	w	w	w

Field	Bits	Type	Description
INITDRXES	7	w	**Init the Digital Receiver at EOM or Loss of Symbol Sync (e.g. for initialization of the Peak Memory Filter)** 0_B Disabled 1_B Enabled Reset: 0_H
INITFRCS	6	w	**Init the Framer at Cycle Start in RMSP.** If disabled, the WUP Data can be used as part of TSI as well in case the modulation type is the same for SPM and RMSP 0_B Disabled 1_B Enabled Reset: 1_H
CODE	5:4	w	**Encoding Mode Selection** 00_B Manchester Code 01_B Differential Manchester Code 10_B Biphase Space 11_B Biphase Mark Reset: 0_H
CHIPDINV	3	w	**Baseband Chip Data Inversion for CH_DATA and Decoder/Framer input. Therefore Inverted Manchester and Inverted Differential Manchester can be decoded internally.** 0_B Not inverted 1_B Inverted Reset: 0_H
DINVEXT	2	w	**Data Inversion of signal DATA and DATA_MATCHFIL for External Processing** 0_B Not inverted 1_B Inverted Reset: 0_H
AAFBYP	1	w	**Anti-Alliasing Filter Bypass** 0_B Not bypassed 1_B Bypassed Reset: 0_H

Field	Bits	Type	Description
AAFFCSEL	0	w	**Anti-Alliasing Filter Corner Frequency Select** 0_B 40 kHz 1_B 80 kHz Reset: 0_H

RSSI Peak Detector Bit Position Register

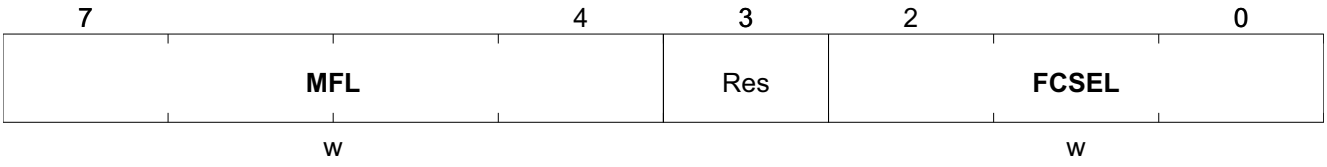
A_PKBITPOS	Offset	Reset Value
RSSI Peak Detector Bit Position Register	**$03B_H$**	**00_H**



Field	Bits	Type	Description
RSSIDLY	7:0	w	**RSSI Detector Start-up Delay** Min: 00h: 0 bit delay (Start with first bit after FSYNC) Max: FFh: 255 bit delay Note: Due to filtering and signal computation, the latency T1 and T2 have to be added Reset: 00_H

PD Filter and Matched Filter Configuration Register

A_PDFMFC	Offset	Reset Value
PD Filter and Matched Filter Configuration Register	**$03C_H$**	**77_H**



Field	Bits	Type	Description
MFL	7:4	w	**Matched Filter Length** MF Length = MFL + 1 Reset: 7_H

Field	Bits	Type	Description
FCSEL	2:0	w	**Pre-demodulation Filter Corner Frequency Selection for FSK signal path** 000_B 33 kHz 001_B 46 kHz 010_B 65 kHz 011_B 93 kHz 100_B 132 kHz 101_B 190 kHz 110_B 239 kHz 111_B 282 kHz Reset: 7_H

Pre Decimation Factor Register

A_PDECF	Offset	Reset Value
Pre Decimation Factor Register	**$03D_H$**	**00_H**

7	6	0
Res	PREDECF	
r	w	

Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H
PREDECF	6:0	w	**Predecimation Filter Decimation Factor** Predecimation Factor = PREDECF + 1 Reset: 00_H

Pre Decimation Scaling Register FSK Mode

A_PDECSCFSK	Offset	Reset Value
Pre Decimation Scaling Register FSK Mode	**$03E_H$**	**00_H**

7	6	5	4	0
Res		INTPOLENF	PDSCALEF	
		w	w	

Field	Bits	Type	Description
INTPOLENF	5	w	**FSK Data Interpolation Enable** 0_B Disabled 1_B Enabled Reset: 0_H
PDSCALEF	4:0	w	**Predecimation Block Scaling Factor for FSK** Min 00h : 2**-10 Max 17h : 2**13 Reset: 00_H

Pre Decimation Scaling Register ASK Mode

A_PDECSCASK **Offset** **Reset Value**

Pre Decimation Scaling Register ASK Mode **$03F_H$** **20_H**

7	6	5	4	0
Res	Res	**INTPOLENA**	**PDSCALEA**	
r		w	w	

Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H
INTPOLENA	5	w	**ASK Data Interpolation Enable** 0_B Disabled 1_B Enabled Reset: 1_H
PDSCALEA	4:0	w	**Predecimation Block Scaling Factor for ASK** Min 00h : 2**-10 Max 17h : 2**13 Reset: 00_H

Sample Rate Converter

A_SRC **Offset** **Reset Value**

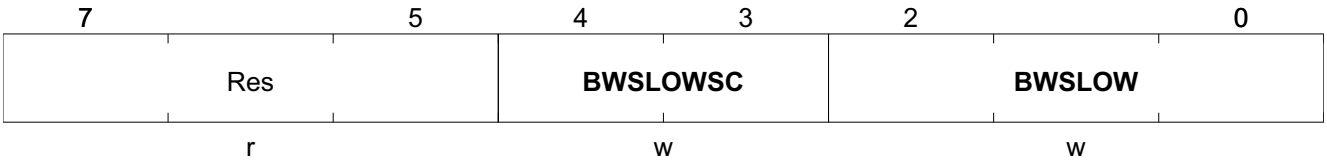
Sample Rate Converter **040_H** **00_H**

7	0
SRCNCO	
w	

Field	Bits	Type	Description
SRCNCO	7:0	w	**Sampling Rate Conversion Factor** Min 00h : Fout = Fin Max FFh : Fout = Fin / 2 Reset: 00_H

External Data Slicer Configuration Register 0

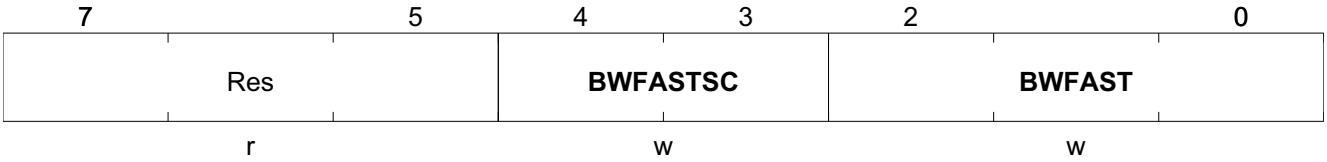
A_EXTSLC0	Offset	Reset Value
External Data Slicer Configuration Register 0	**041_H**	**02_H**



Field	Bits	Type	Description
Res	7:5	r	**for future use** Reset: 0_H
BWSLOWSC	4:3	w	**DC Offset Cancelation Bandwidth Scaling Selection for slow setting** 00_B 1/2 01_B 1/4 10_B 1/8 11_B 1/16 Reset: 0_H
BWSLOW	2:0	w	**DC Offset Cancelation Bandwidth Coefficient Selection for slow setting** 000_B 1/8 001_B 1/16 010_B 1/24 011_B 1/32 100_B 1/40 101_B 1/48 110_B FREEZE Might be used for suppressing "occasional pulse interferer". Could be activated after decission of software CDR. 111_B n.u. Reset: 2_H

External Data Slicer Configuration Register 1

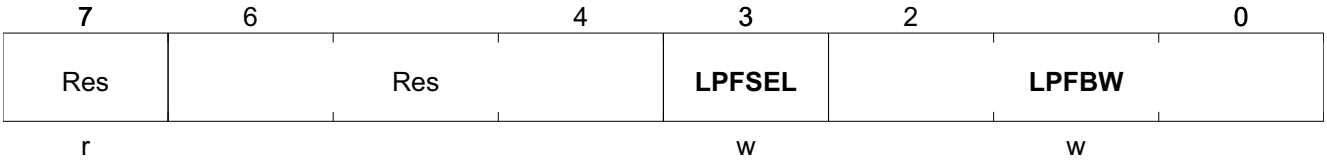
A_EXTSLC1	Offset	Reset Value
External Data Slicer Configuration Register 1	**042_H**	**02_H**



Field	Bits	Type	Description
Res	7:5	r	**for future use** Reset: 0_H
BWFASTSC	4:3	w	**DC Offset Cancelation Bandwidth Scaling Selection for fast setting** 00_B 1/2 01_B 1/4 10_B 1/8 11_B 1/16 Reset: 0_H
BWFAST	2:0	w	**DC Offset Cancelation Bandwidth Coefficient Selection for fast setting** 000_B 1/8 001_B 1/16 010_B 1/24 011_B 1/32 100_B 1/40 101_B 1/48 110_B FREEZE Might be used for suppressing "occasional pulse interferer". Could be activated after decission of software CDR. 111_B n.u. Reset: 2_H

External Data Slicer Configuration Register 2

A_EXTSLC2	Offset	Reset Value
External Data Slicer Configuration Register 2	**043_H**	**00_H**

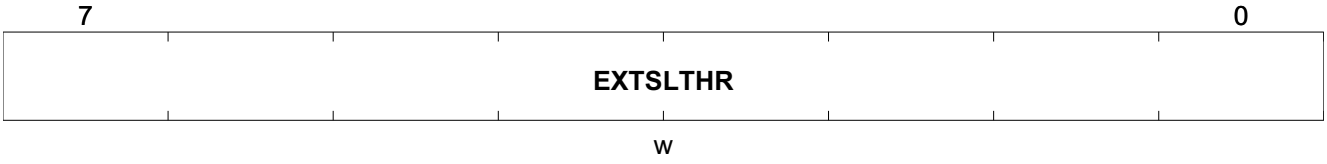


Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H

Field	Bits	Type	Description
LPFSEL	3	w	**Low Pass Filter select** 0_B Matched Filter selected 1_B LPF selected Reset: 0_H
LPFBW	2:0	w	**Low Pass Filter Bandwidth Coefficient Selection** 000_B 1/1.6 001_B 1/2 010_B 1/2.67 011_B n.u. 100_B 1/3.2 101_B 1/4 110_B 1/5.33 111_B n.u. Reset: 0_H

Externel Data Slicer BW Switching Threshold Register 0

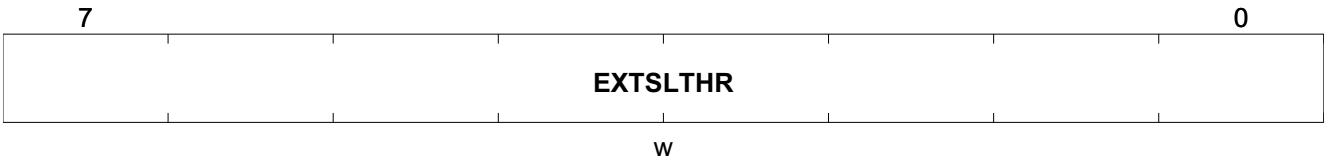
A_EXTSLTHR0	Offset	Reset Value
Externel Data Slicer BW Switching Threshold Register 0	**044_H**	**00_H**



Field	Bits	Type	Description
EXTSLTHR	7:0	w	**Externel Data Slicer BW Switching Threshold** Reset: 00_H

Externel Data Slicer BW Switching Threshold Register 1

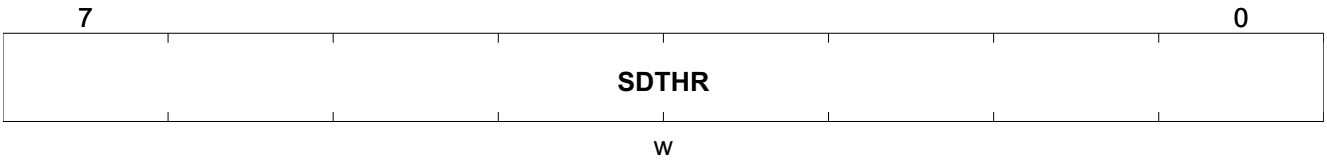
A_EXTSLTHR1	Offset	Reset Value
Externel Data Slicer BW Switching Threshold Register 1	**045_H**	**00_H**



Field	Bits	Type	Description
EXTSLTHR	7:0	w	**Externel Data Slicer BW Switching Threshold** Reset: 00_H

Signal Detector Threshold Level Register - Run Mode

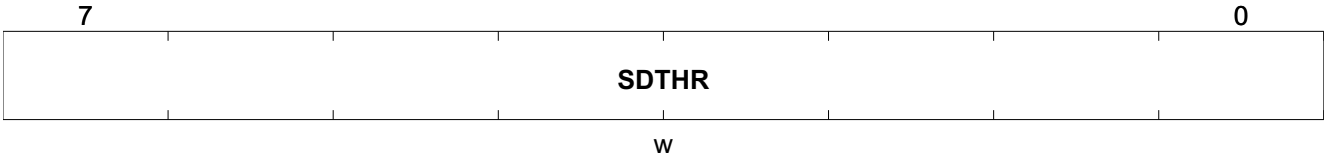
A_SIGDET0	Offset	Reset Value
Signal Detector Threshold Level Register - Run Mode	**046_H**	**00_H**



Field	Bits	Type	Description
SDTHR	7:0	w	**Signal Detector Threshold Level for Run Mode** Reset: 00_H

Signal Detector Threshold Level Register - Wakeup

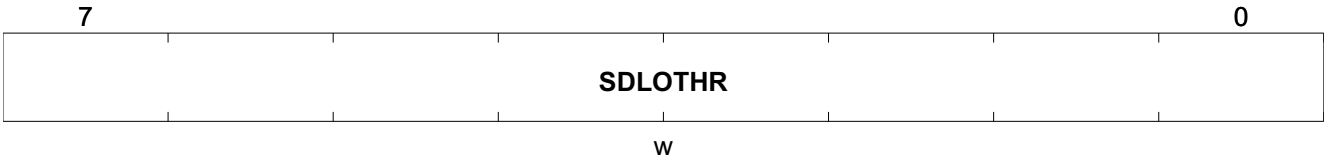
A_SIGDET1	Offset	Reset Value
Signal Detector Threshold Level Register - Wakeup	**047_H**	**00_H**



Field	Bits	Type	Description
SDTHR	7:0	w	**Signal Detector Threshold Level for Wakeup** Reset: 00_H

Signal Detector Threshold Low Level Register

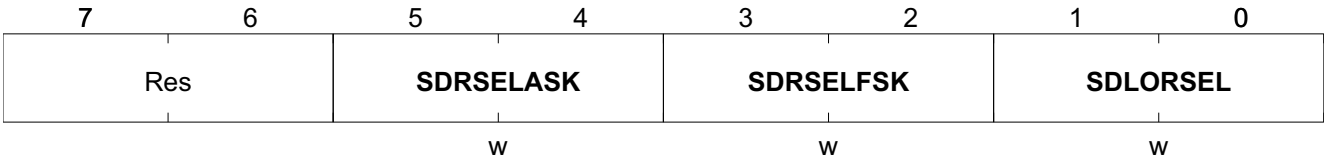
A_SIGDETLO	Offset	Reset Value
Signal Detector Threshold Low Level Register	**048_H**	**00_H**



Field	Bits	Type	Description
SDLOTHR	7:0	w	**Signal Detector Threshold Low Level. This threshold level is** only valid, if the FSK Noise detector selection in the A_NDCONFIG register is set to 11b Reset: 00_H

Signal Detector Range Selection Register

A_SIGDETSEL	Offset	Reset Value
Signal Detector Range Selection Register	**049_H**	**$7F_H$**



Field	Bits	Type	Description
SDRSELASK	5:4	w	**A_SIGDET0/1 range selection factor for ASK. The selected signal detector value is multiplied by the 2^range selection factor. Use the right setting to fit the measured SPWR value.** 00_B 6 01_B 7 10_B 7+6 11_B 8 Reset: 3_H
SDRSELFSK	3:2	w	**A_SIGDET0/1 range selection factor for FSK. The selected signal detector value is multiplied by the 2^range selection factor. Use the right setting to fit the measured SPWR value.** 00_B 2 01_B 4 10_B 6 11_B 8 Reset: 3_H

Field	Bits	Type	Description
SDLORSEL	1:0	w	**SIGDETLO range selection factor. The selected signal detector value is multiplied by the 2^range selection factor. Use the right setting to fit the measured SPWR value.** 00_B 2 01_B 4 10_B 6 11_B 8 Reset: 3_H

Signal Detector Configuration Register

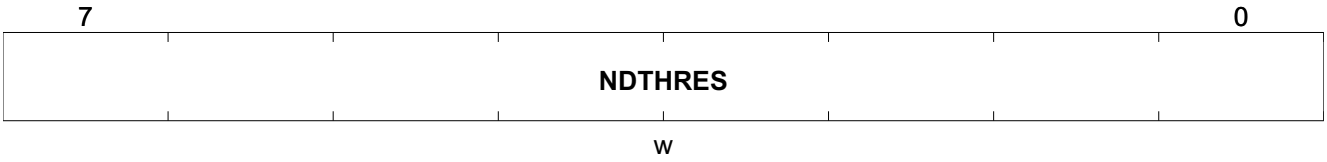
A_SIGDETCFG	Offset	Reset Value
Signal Detector Configuration Register	**$04A_H$**	**00_H**

7	6	5	4	3	2	1	0
Res		Res	**SDLORE**	**SDBCNTWU**		**SDBCNTR**	
r			w	w		w	

Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
SDLORE	4	w	**Source selection of Signal Power Readout Register** 0_B Signal Power for A_SIGDET0/1 1_B Signal for minimal usable FSK deviation, the sigdet low level can be read out with SPWR register Reset: 0_H
SDBCNTWU	3:2	w	**Signal Detector Bridging Counter for Wakeup** Signal detector output will be bridged for a selected length 00_B Disabled 01_B 1 chip 10_B 5 chips 11_B 10 chips Reset: 0_H
SDBCNTR	1:0	w	**Signal Detector Bridging Counter for Run Mode** Signal detector output will be bridged for a selected length 00_B Disabled 01_B 1 chip 10_B 5 chips 11_B 10 chips Reset: 0_H

FSK Noise Detector Threshold Register

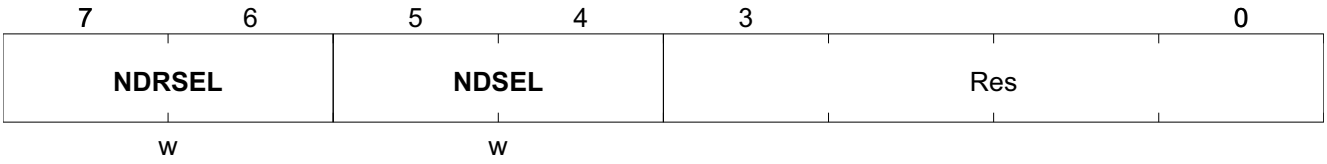
A_NDTHRES	Offset	Reset Value
FSK Noise Detector Threshold Register	$04B_H$	00_H



Field	Bits	Type	Description
NDTHRES	7:0	w	**FSK Noise Detector Threshold** Reset: 00_H

FSK Noise Detector Configuration Register

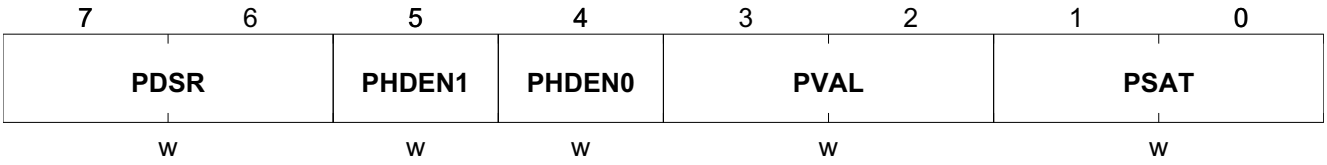
A_NDCONFIG	Offset	Reset Value
FSK Noise Detector Configuration Register	$04C_H$	07_H



Field	Bits	Type	Description
NDRSEL	7:6	w	**FSK Noise Detector Range Selection** 00_B 2^7 01_B 2^6 10_B 2^5 11_B 2^4 Reset: 0_H
NDSEL	5:4	w	**Signal and Noise Detector Selection** 00_B Signal detection (=Squelch) only. This mode is recommended for ASK. 01_B Noise detection only 10_B Signal and noise detection simultaneously 11_B Signal and noise detection simultaneously, but the FSK noise detect signal is valid only if the SIGDETLO threshold is exceeded. This is the recommended mode for FSK. Reset: 0_H

Clock and Data Recovery P Configuration Register

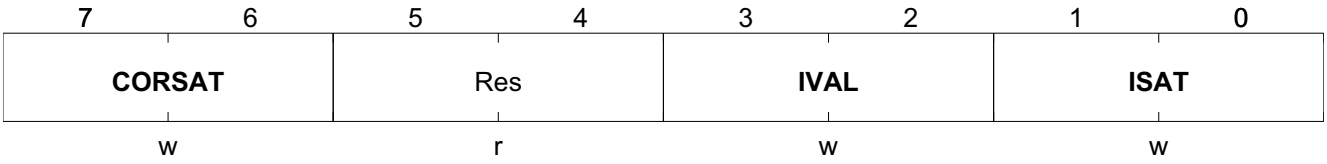
A_CDRP	Offset	Reset Value
Clock and Data Recovery P Configuration Register	$04D_H$	$E6_H$



Field	Bits	Type	Description
PDSR	7:6	w	**Peak-Detector slew rate. The slew rate of the Peak-Detector in the clock-recovery path will be set with** PDSR. Actually, Peak-Detector part of Signal Detector Block 00_B up/down = 1/64 01_B up = 1/64; down = 1/128 10_B up = 1/32; down = 1/128 11_B up = 1/32; down = 1/256 Reset: 3_H
PHDEN1	5	w	**Phase detector error (PDE) outer tolerance range** 0_B Disabled: PDEout = PDEin. 1_B Enabled: If PDEin > abs(7/16) bit then PDEout = 0 else PDEout = PDEin. Reset: 1_H
PHDEN0	4	w	**Phase detector error (PDE) inner tolerance range** 0_B Disabled: PDEout = PDEin. 1_B Enabled: If PDEin < abs(1/16) bit then PDEout = 0 else PDEout = PDEin. Reset: 0_H
PVAL	3:2	w	**P Value. The PVAL is the P value of the Clock-Recovery PI Loop-Filter. The Phase-** Detector output error will be multiplied with the set value. 00_B 1/1 phase detector error 01_B 1/2 phase detector error 10_B 1/4 phase detector error 11_B 1/8 phase detector error Reset: 1_H
PSAT	1:0	w	**P Value Saturation. The saturation of the P-Loop-Filter path will be set according to the PSAT** value. Remark that the internal phase resolution of the phase detector is 1/16 bit. 00_B saturation to 1/16 bit 01_B saturation to 2/16 bit 10_B saturation to 4/16 bit 11_B saturation to 8/16 bit Reset: 2_H

Clock and Data Recovery Configuration Register

A_CDRI	Offset	Reset Value
Clock and Data Recovery Configuration Register	$04E_H$	45_H



Field	Bits	Type	Description
CORSAT	7:6	w	**Correlator output value (Timing extrapolation unit). The timing extrapolation unit output value will be multiplied with the LFSAT** value. The timing extrapolation unit measures the data rate error during the RUNIN sequence and sets the I-Loop-Filter path when the RUNIN length is reached. 00_B 1/4 calculated value 01_B 1/8 calculated value 10_B 1/16 calculated value 11_B 1/32 calculated value Reset: 1_H
Res	5:4	r	**for future use** Reset: 0_H
IVAL	3:2	w	**I Value. The IVAL is the I value of the Clock-Recovery PI Loop-Filter. The Phase-** Detector output error will be multiplied with this set value. 00_B 1/32 phase detector error 01_B 1/64 phase detector error 10_B 1/128 phase detector error 11_B 1/256 phase detector error Reset: 1_H
ISAT	1:0	w	**I Value Saturation. The saturation of the I-Loop-Filter accumulator will be set according to the** ISAT value. Remark that the internal phase resolution of the phase detector is 1/16 bit. 00_B saturation to 1/16 bit 01_B saturation to 2/16 bit 10_B saturation to 4/16 bit 11_B saturation to 8/16 bit Reset: 1_H

CDR Configuration Register 0

A_CDRCFG0	Offset	Reset Value
CDR Configuration Register 0	**$04F_H$**	**$4C_H$**

7	6	5	3	2	0
RUNLEN		**TOLCHIPH**		**TOLCHIPL**	
w		w		w	

Field	Bits	Type	Description
RUNLEN	7:6	w	**RUNIN Length. The RUNIN length is equal to PLL-start-value calculation time. This means** that the shorter RUNIN length decreases the data rate offset calculation accuracy and symbol synchronization found signal generation stability. Note that the RUNLEN have to be changed together with the TSI configuration registers. 00_B 8 chips 01_B 7 chips 10_B 6 chips 11_B 5 chips Reset: 1_H
TOLCHIPH	5:3	w	**Duty Cycle Tolerance for Chip Border High Level. Represents the number of 1/16 bit sample deviation from the ideal chip border where an edge can occur in direction to the following chip border.** Reset: 1_H
TOLCHIPL	2:0	w	**Duty Cycle Tolerance for Chip Border Low Level. Represents the number of 1/16 bit sample deviation from the ideal chip border where an edge can occur in direction to the previous chip border.** Reset: 4_H

CDR Configuration Register 1

A_CDRCFG1	Offset	Reset Value
CDR Configuration Register 1	**050_H**	**$1E_H$**

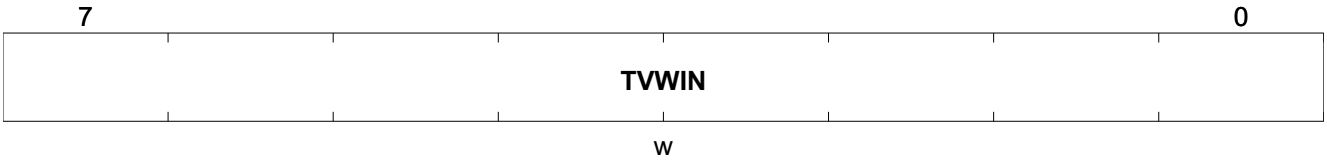
7	6	5	3	2	0
Res	**DRLIMEN**	**TOLBITH**		**TOLBITL**	
r	w	w		w	

Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H

Field	Bits	Type	Description
DRLIMEN	6	w	**Enable data rate error acceptance limitation.** The limits are defined in CDRDRTHRP and CDRDRTHRN registers. 0_B Disabled 1_B Enabled Reset: 0_H
TOLBITH	5:3	w	**Duty Cycle Tolerance for Bit Border High Level. Represents the number of 1/16 bit sample deviation from the ideal bit border where an edge can occur in direction to the following bit border.** Reset: 3_H
TOLBITL	2:0	w	**Duty Cycle Tolerance for Bit Border Low Level. Represents the number of 1/16 bit sample deviation from the ideal bit border where an edge can occur in direction to the previous bit border.** Reset: 6_H

Timing Violation Window Register

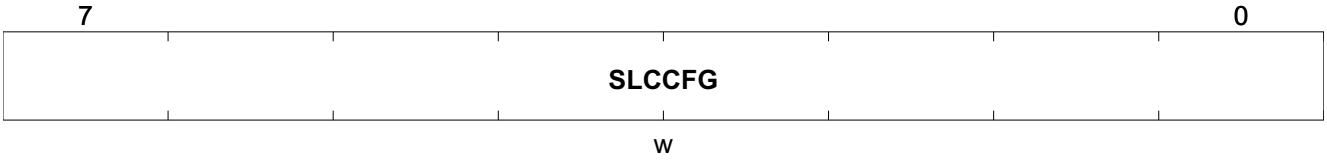
A_TVWIN	Offset	Reset Value
Timing Violation Window Register	**051_H**	**28_H**



Field	Bits	Type	Description
TVWIN	7:0	w	**Timing Violation Window Length.** Defines the maximal number of 1/16 data samples without detected edge which will be tolerated by CDR with no Loss of Symbol Synchronization 28h: 40/16 bit ((8 + 16 *CV + 8)*1.25) FFh: 255/16 bit Note: in TSIGAP mode the value must be higher. Reset: 28_H

Slicer Configuration Register

A_SLCCFG	Offset	Reset Value
Slicer Configuration Register	**052_H**	**90_H**



Field	Bits	Type	Description
SLCCFG	7:0	w	**Data Slicer Configuration** Value 94_H : Chip Mode with Code Violations enabled (A_EOMC.EOMDATLEN enabled) Value 90_H : Chip Mode with Code Violations enabled (A_EOMC.EOMCV enabled and A_EOMC.EOMDATLEN disabled) Value 75_H : Bit Mode without Code Violation Value $8C_H$: NRZ Mode Reset: 90_H

TSI Detection Mode Register

A_TSIMODE	Offset	Reset Value
TSI Detection Mode Register	**053_H**	**80_H**

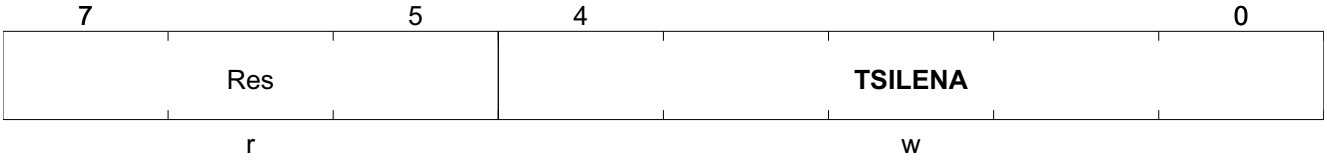
7	6	3	2	1	0
TSIGRSYN	**TSIWCA**		**CPHRA**	**TSIDETMOD**	
w	w		w	w	

Field	Bits	Type	Description
TSIGRSYN	7	w	**TSI Gap Resync Mode (only for TSIDETMODE=2_H)** 0_B Disabled - In this mode the GAPVAL and TSIGAP values are used, so the overall GAP time can be defined in T/16 steps. 1_B Enabled - PLL resync after TSI Gap In this mode the T/2 GAP resolution can be set in the 5 MSB TSIGAP register bits. GAPVAL value is not used. Prefered in TSI Gap Mode. Reset: 1_H
TSIWCA	6:3	w	**Wild Cards for 4 LSB bits of Correlator A** If bit is 0, the whole TSI pattern for Correlator A is valid if bit is 1, the corresponding bit from the TSI pattern is ignored Reset: 0_H
CPHRA	2	w	**Code Phase Readjustment in Payload** 0_B disabled - code polarity is defined by the TSI pattern 1_B enabled - code phase readjustment in payload Reset: 0_H

Field	Bits	Type	Description
TSIDETMOD	1:0	w	**TSI Detection Mode** 00_B 16 Bit TSI Mode - TSI configuration B AND A valid (sequentially), B is valid if the A_TSILENB > 0 01_B 8 Bit Parallel TSI Mode - TSI configurations A OR B (parallel) 10_B 8 Bit TSI Gap Mode - TSI configurations A AND B with Gap (sequentially with Gap between TSIA & TSIB) 11_B 8 Bit Extended TSI Mode - TSI configurations A OR B (parallel with matching information), dependent on found TSI A or B, 0 resp. 1 will be sent as 1st received bit. Reset: 0_H

TSI Length Register A

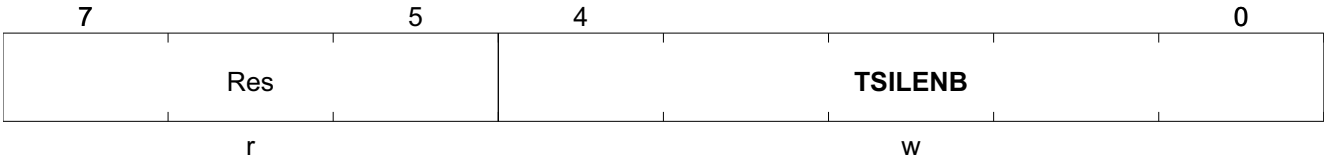
A_TSILENA	Offset	Reset Value
TSI Length Register A	**054_H**	**00_H**



Field	Bits	Type	Description
Res	7:5	r	**for future use** Reset: 0_H
TSILENA	4:0	w	**TSI A Length (in chips):** (11_H up to $1F_H$ not used) Min: 00h = 0 Bit; Does only work in 16 Bit Mode: FSYNC will be generated after Symbol Synchronization. In other Modes the smallest possible value to generate a FSYNC will be 01h. Be aware that such small values makes it impossible to find the right phase of the pattern in the data stream and therefore wrong data and code violations can be generated. Max: 10h = 16 Chips = 8 Bit Reset: 00_H

TSI Length Register B

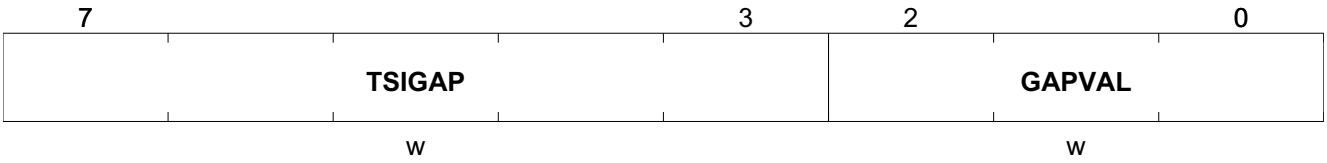
A_TSILENB	Offset	Reset Value
TSI Length Register B	**055_H**	**00_H**



Field	Bits	Type	Description
Res	7:5	r	**for future use** Reset: 0_H
TSILENB	4:0	w	**TSI B Length (in chips):** (11_H up to $1F_H$ not used) Min: 00h =0 Bit(see also A_TSILENA) Max: 10h = 16 Chips = 8 Bit Reset: 00_H

TSI Gap Length Register

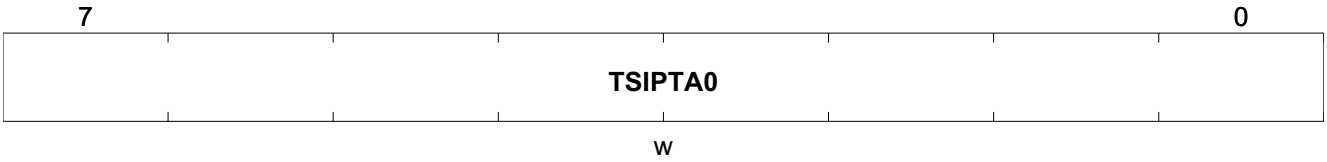
A_TSIGAP	Offset	Reset Value
TSI Gap Length Register	**056_H**	**00_H**



Field	Bits	Type	Description
TSIGAP	7:3	w	**TSI Gap (T/2 bit resolution)** 1Fh: 15 1/2 bit gap 00h: 0 bit gap TSIGAP is used to lock the PLL after TSI A is found, if the TSI detection mode 10b is selected. Reset: 00_H
GAPVAL	2:0	w	**TSI Gap (T/16 bit resolution)** 111b: 7/16 bit gap 000b: 0 bit gap GAPVAL is used to correct the DCO phase after TSIGAP time, if A_TSIMODE.TSIGRSYN is disabled Reset: 0_H

TSI Pattern Data Reference A Register 0

A_TSIPTA0	Offset	Reset Value
TSI Pattern Data Reference A Register 0	**057_H**	**00_H**

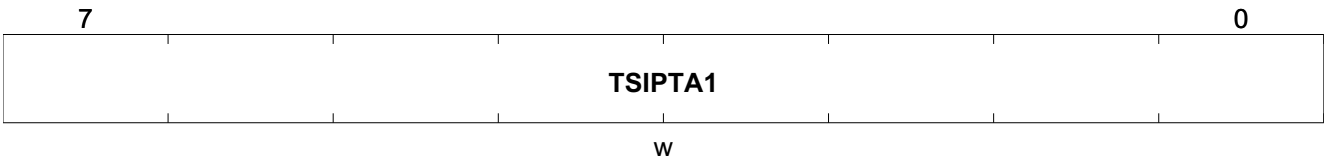


Field	Bits	Type	Description
TSIPTA0	7:0	w	**Data Pattern for TSI comparison: Bit 7...Bit 0(LSB) (in Chips)** Reset: 00_H

TSI Pattern Data Reference A Register 1

A_TSIPTA1 **Offset** **Reset Value**

TSI Pattern Data Reference A Register 1 **058_H** **00_H**

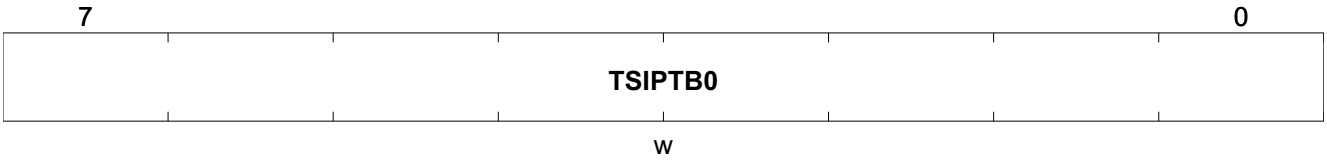


Field	Bits	Type	Description
TSIPTA1	7:0	w	**Data Pattern for TSI comparison: Bit 15(MSB)...Bit 8 (in Chips)** Reset: 00_H

TSI Pattern Data Reference B Register 0

A_TSIPTB0 **Offset** **Reset Value**

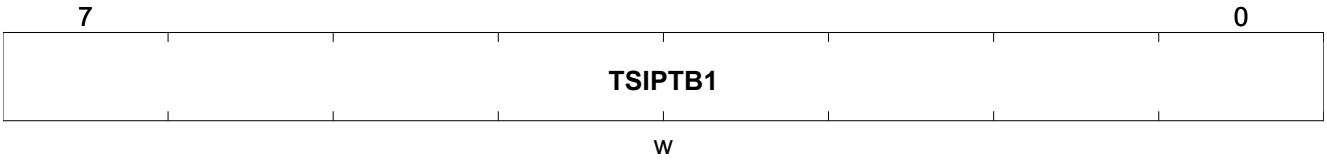
TSI Pattern Data Reference B Register 0 **059_H** **00_H**



Field	Bits	Type	Description
TSIPTB0	7:0	w	**Data Pattern for TSI comparison: Bit 7...Bit 0(LSB) (in Chips)** Reset: 00_H

TSI Pattern Data Reference B Register 1

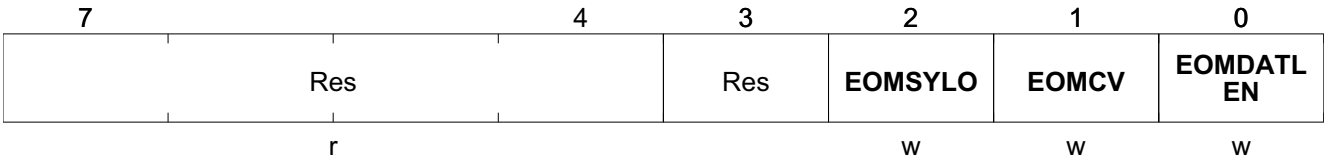
A_TSIPTB1	Offset	Reset Value
TSI Pattern Data Reference B Register 1	$05A_H$	00_H



Field	Bits	Type	Description
TSIPTB1	7:0	w	**Data Pattern for TSI comparison: Bit 15(MSB)...Bit 8 (in Chips)** Reset: 00_H

End Of Message Control Register

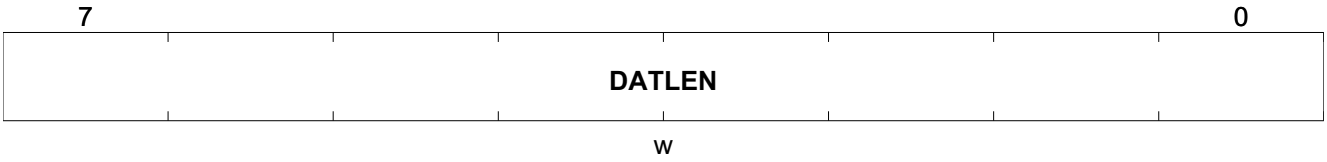
A_EOMC	Offset	Reset Value
End Of Message Control Register	$05B_H$	05_H



Field	Bits	Type	Description
Res	7:4	r	**for future use** Reset: 0_H
EOMSYLO	2	w	**EOM by Sync Loss** 0_B Disabled 1_B Enabled Reset: 1_H
EOMCV	1	w	**EOM by Code Violation** 0_B Disabled 1_B Enabled Reset: 0_H
EOMDATLEN	0	w	**EOM by Data Length** 0_B Disabled 1_B Enabled Reset: 1_H

EOM Data Length Limit Register

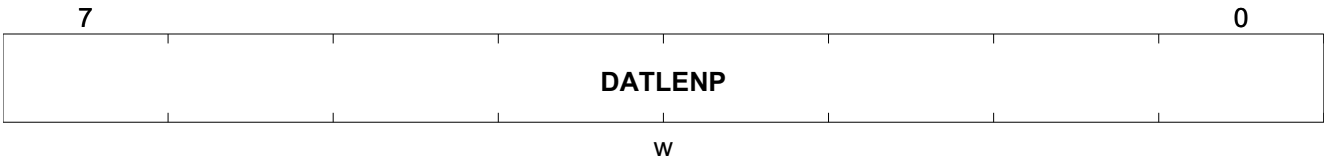
A_EOMDLEN	Offset	Reset Value
EOM Data Length Limit Register	$05C_H$	00_H



Field	Bits	Type	Description
DATLEN	7:0	w	**Length of Data Field in Telegram, only valid when EOM criterion is EOMDATLEN** Counting of number of payload bits starts after the last TSI Bit. EOM will be generated after the last payload bit. In 8-bit extended TSI mode, the value must be the payload length + 1, because of the additional bit inserted (matching information). Min: 00h = 256 payload bits Reg. value 01h = 1 payload bit Max: FFh = 255 payload bits Reset: 00_H

EOM Data Length Limit Parallel Mode Register

A_EOMDLENP	Offset	Reset Value
EOM Data Length Limit Parallel Mode Register	$05D_H$	00_H



Field	Bits	Type	Description
DATLENP	7:0	w	**Length of Data Field in Telegram in Parallel Mode for TSI Pattern B, only valid when EOM criterion is EOMDATLEN** Counting of number of payload bits starts after the last TSI Bit. EOM will be generated after the last payload bit. In 8-bit extended TSI mode, the value must be the payload length + 1, because of the additional bit inserted (matching information). Min: 00h = 256 payload bits Reg. value 01h = 1 payload bit Max: FFh = 255 payload bits Reset: 00_H

Channel Configuration Register

A_CHCFG	Offset	Reset Value
Channel Configuration Register	$05E_H$	00_H

7	6	5	4	3	2	1	0
Res	EXTPROC		EOM2SPM	NOC		MT	
r	w		w	w		w	

Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H
EXTPROC	6:5	w	**External Data Processing** 00_B No deactivation of functional blocks 01_B Chip Data (RX Mode: TMCDS) - no framing - FSYNC, MID and EOM interrupts disabled - only TOTIM_SYNC is active - random, equal and pattern WU are disabled (mapped to sync) 10_B Data + Data MF (RX Mode: TMMF, TMRDS) - no framing - FSYNC, MID and EOM interrupts disabled - all TOTIMs are inactive - only WU on RSSI (Level Criterion) possible 11_B not used Reset: 0_H
EOM2SPM	4	w	**Continue with Self Polling Mode after EOM detected in Run Mode Self Polling** 0_B Disabled - stay in Run Mode Self Polling (next Payload Frame is expected) 1_B Enabled - leave Run Mode Self Polling after EOM Reset: 0_H
NOC	3:2	w	**Number of Channels (Run Mode Slave / Self Polling Mode - Run Mode Self Polling)** 00_B Channel 1 / Channel 1 01_B Channel 2 / Channel 1 + 2 10_B Channel 3 / Channel 1 + 2 + 3 11_B Channel 4 / Channel 1 + 2 + 3 + 4 Reset: 0_H

Field	Bits	Type	Description
MT	1:0	w	**Modulation Type (Run Mode Slave / Self Polling Mode - Run Mode Self Polling)** 00_B ASK / ASK - ASK 01_B FSK / FSK - FSK 10_B ASK / FSK - ASK 11_B FSK / ASK - FSK Reset: 0_H

TX RF Configuration Register

A_TXRF	Offset	Reset Value
TX RF Configuration Register	**$05F_H$**	**04_H**

7	4	3	2	0
Res		Res	**DCCSEL**	
r			w	

Field	Bits	Type	Description
Res	7:4	r	**for future use** Reset: 0_H
DCCSEL	2:0	w	**Duty Cycle Control selection** Duty Cycle = (DCCSEL + 8) / 32 Reset: 3_H

TX Configuration Regsiter

A_TXCFG	Offset	Reset Value
TX Configuration Regsiter	**060_H**	**05_H**

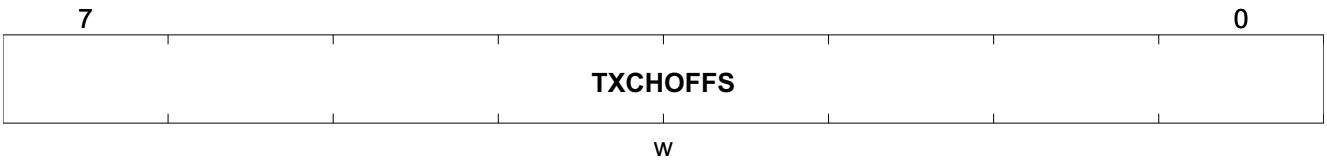
7	6	5	4	3	2	0
Res	**ASKFSK**	**ASKSLOPEN**	**GFSKEN**	**INVERSION**	**ENCODING**	
r	w	w	w	w	w	

Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H

Field	Bits	Type	Description
ASKFSK	6	w	**Modulation Type Selection** 0_B ASK 1_B FSK Reset: 0_H
ASKSLOPEN	5	w	**ASK sloping enable** In FSK mode enable for power-up sloping 0_B Disabled 1_B Enabled Reset: 0_H
GFSKEN	4	w	**GFSK (Gaussian Filter) enable** FSK mode only 0_B Disabled 1_B Enabled Reset: 0_H
INVERSION	3	w	**TX data inversion** 0_B Disabled 1_B Enabled Reset: 0_H
ENCODING	2:0	w	**Encoding mode, code selection** 000_B Manchester 001_B Differential manchester 010_B Biphase Space 011_B Biphase Mark 100_B Miller 101_B NRZ 110_B Scrambling (PRBS) 111_B n.u. Reset: 5_H

TX Channel Offset Register 0

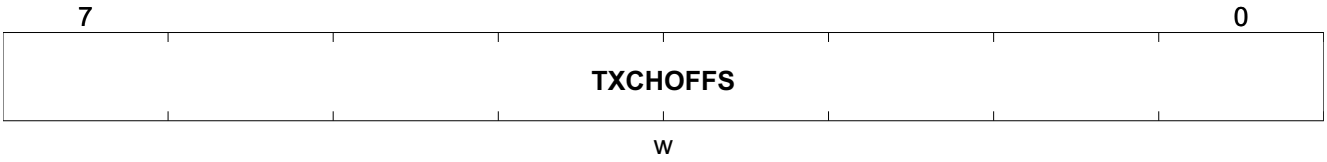
A_TXCHOFFS0	Offset	Reset Value
TX Channel Offset Register 0	**061_H**	**00_H**



Field	Bits	Type	Description
TXCHOFFS	7:0	w	**Channel Offset Frequency** Resolution = 1.493 kHz Reset: 00_H

TX Channel Offset Register 1

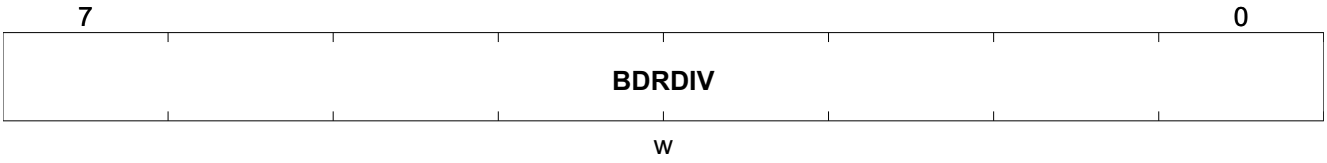
A_TXCHOFFS1	Offset	Reset Value
TX Channel Offset Register 1	**062_H**	**00_H**



Field	Bits	Type	Description
TXCHOFFS	7:0	w	**Channel Offset Frequency** Resolution = 1.493 kHz Reset: 00_H

TX Baudrate Divider Register 0

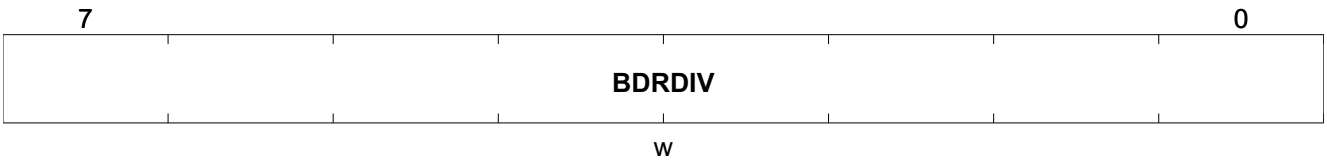
A_TXBDRDIV0	Offset	Reset Value
TX Baudrate Divider Register 0	**063_H**	**00_H**



Field	Bits	Type	Description
BDRDIV	7:0	w	**Baudrate division factor (bits 7:0)** Resolution = Tsys Reset: 00_H

TX Baudrate Divider Register 1

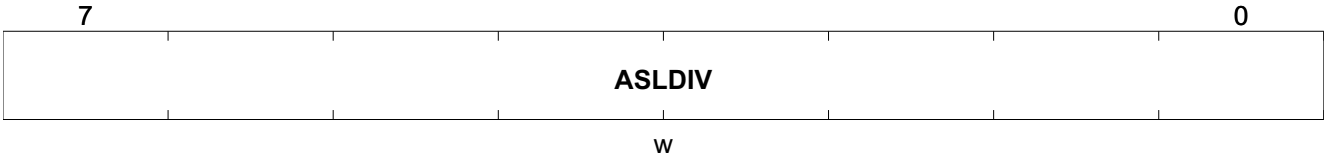
A_TXBDRDIV1	Offset	Reset Value
TX Baudrate Divider Register 1	**064_H**	**00_H**



Field	Bits	Type	Description
BDRDIV	7:0	w	**Baudrate division factor (bits 15:8)** Resolution = Tsys Reset: 00_H

TX Data Shaping Configuration Register 0

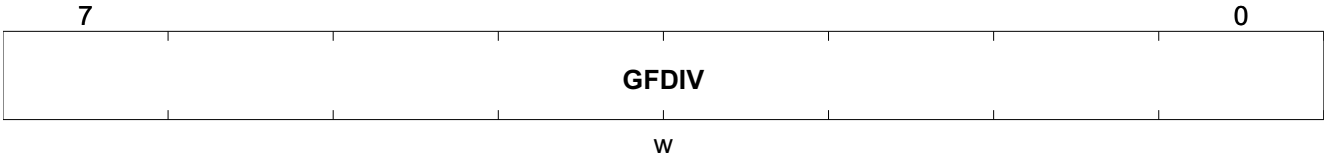
A_TXDSHCFG0	Offset	Reset Value
TX Data Shaping Configuration Register 0	**065_H**	**00_H**



Field	Bits	Type	Description
ASLDIV	7:0	w	**ASK sloping division factor (bits 7:0)** Resolution = Tsys Reset: 00_H

TX Data Shaping Configuration Register 1

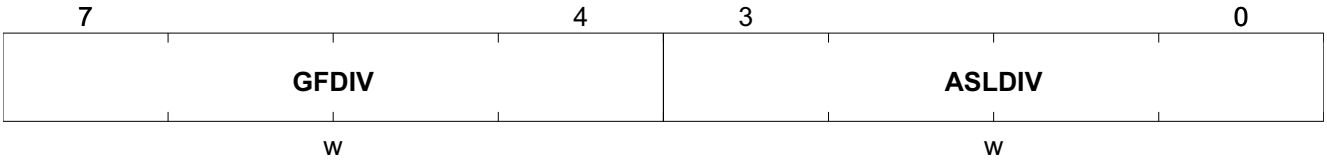
A_TXDSHCFG1	Offset	Reset Value
TX Data Shaping Configuration Register 1	**066_H**	**00_H**



Field	Bits	Type	Description
GFDIV	7:0	w	**Gaussian filter division factor (bits 7:0)** Resolution = Tsys Reset: 00_H

TX Data Shaping Configuration Register 2

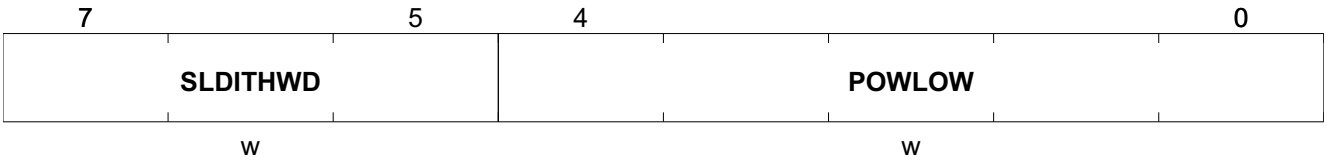
A_TXDSHCFG2	Offset	Reset Value
TX Data Shaping Configuration Register 2	**067_H**	**00_H**



Field	Bits	Type	Description
GFDIV	7:4	w	**Gaussian filter division factor (bits 11:8)** Resolution = Tsys Reset: 0_H
ASLDIV	3:0	w	**ASK sloping division factor (bits 11:8)** Resolution = Tsys Reset: 0_H

TX Power Configuration Register 0

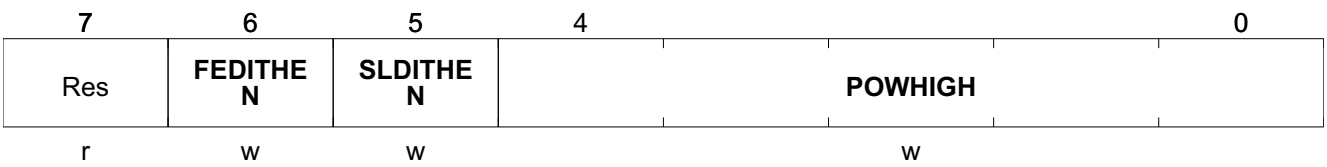
A_TXPOWER0	Offset	Reset Value
TX Power Configuration Register 0	**068_H**	**00_H**



Field	Bits	Type	Description
SLDITHWD	7:5	w	**ASK sloping dithering width** Dithering range : - 2**SLDITHWD to 2**SLDITHWD - 1 Reset: 0_H
POWLOW	4:0	w	**Output power for data LOW in ASK, not used in FSK mode** POWLOW defines the number of enabled PA stages during the low phase of ASK Reset: 00_H

TX Power Configuration Register 1

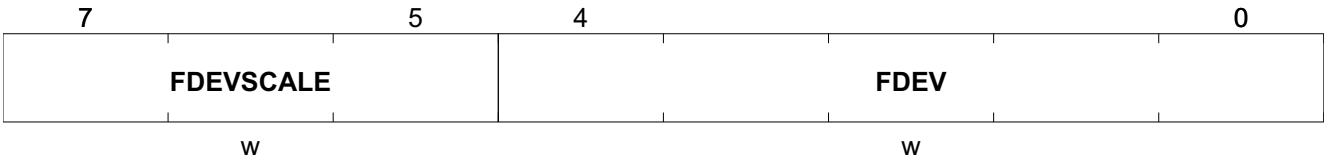
A_TXPOWER1	Offset	Reset Value
TX Power Configuration Register 1	**069_H**	**00_H**



Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H
FEDITHEN	6	w	**Falling edge dithering enable** 0_B Disabled 1_B Enabled Reset: 0_H
SLDITHEN	5	w	**ASK sloping dithering enable** 0_B Disabled 1_B Enabled Reset: 0_H
POWHIGH	4:0	w	**Output power for data HIGH in ASK, output power in FSK** POWHIGH defines the number of enabled PA stages in FSK or during the high phase of ASK Reset: 00_H

TX Frequency Deviation Register

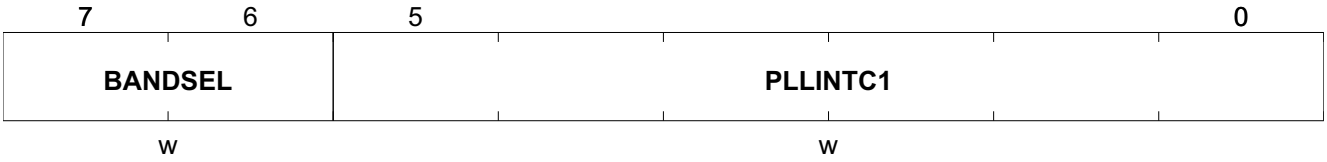
A_TXFDEV	Offset	Reset Value
TX Frequency Deviation Register	**$06A_H$**	**00_H**



Field	Bits	Type	Description
FDEVSCALE	7:5	w	**Scaling factor of the frequency deviation FDEV** 000_B Divide by 64 001_B Divide by 32 010_B Divide by 16 011_B Divide by 8 100_B Divide by 4 101_B Divide by 2 110_B Divide by 1 111_B Multiply by 2 Reset: 0_H
FDEV	4:0	w	**Frequency deviation selection factor** Reset: 00_H

PLL MMD Integer Value Register Channel 1

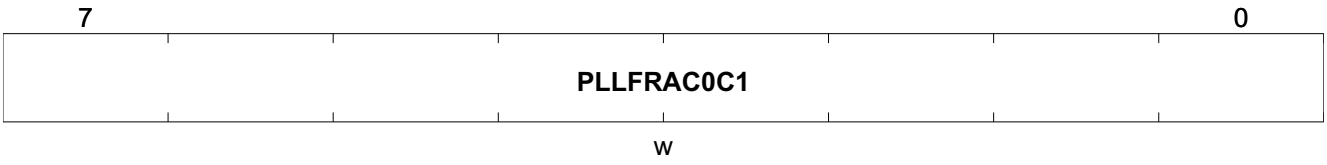
A_PLLINTC1	Offset	Reset Value
PLL MMD Integer Value Register Channel 1	$06B_H$	93_H



Field	Bits	Type	Description
BANDSEL	7:6	w	**Frequency Band Selection** 00_B not used 01_B 863-960 MHz 10_B 415-495 MHz 11_B 300-320 MHz Reset: 2_H
PLLINTC1	5:0	w	**SDPLL Multi Modulus Divider Integer Offset value for Channel 1** PLLINT(5:0) = dec2hex(INT(f_LO / f_XTAL)) Reset: 13_H

PLL Fractional Division Ratio Register 0 Channel 1

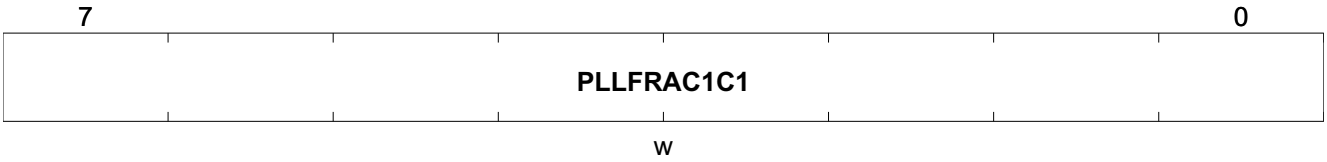
A_PLLFRAC0C1	Offset	Reset Value
PLL Fractional Division Ratio Register 0 Channel 1	$06C_H$	$F3_H$



Field	Bits	Type	Description
PLLFRAC0C1	7:0	w	**Synthesizer channel frequency value (21 bits, bits 7:0), fractional division ratio for Channel 1** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: $F3_H$

PLL Fractional Division Ratio Register 1 Channel 1

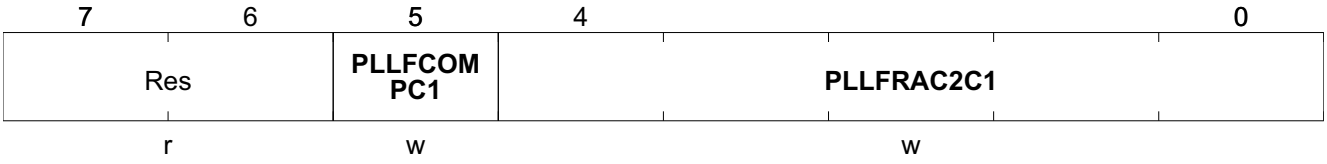
A_PLLFRAC1C1	Offset	Reset Value
PLL Fractional Division Ratio Register 1 Channel 1	$06D_H$	07_H



Field	Bits	Type	Description
PLLFRAC1C1	7:0	w	**Synthesizer channel frequency value (21 bits, bits 15:8), fractional division ratio for Channel 1** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 07_H

PLL Fractional Division Ratio Register 2 Channel 1

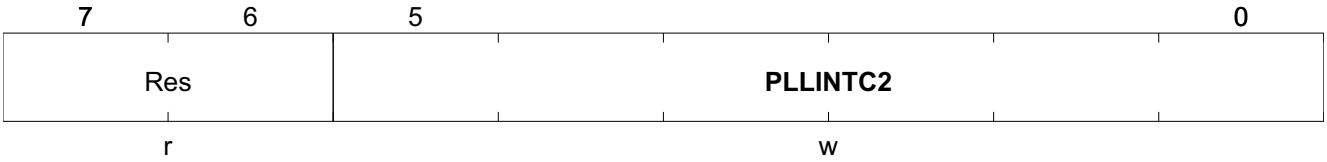
A_PLLFRAC2C1	Offset	Reset Value
PLL Fractional Division Ratio Register 2 Channel 1	**$06E_H$**	**09_H**



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
PLLFCOMPC1	5	w	**Fractional Spurii Compensation enable for Channel 1** 0_B Disabled 1_B Enabled Reset: 0_H
PLLFRAC2C1	4:0	w	**Synthesizer channel frequency value (21 bits, bits 20:16), fractional division ratio for Channel 1** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 09_H

PLL MMD Integer Value Register Channel 2

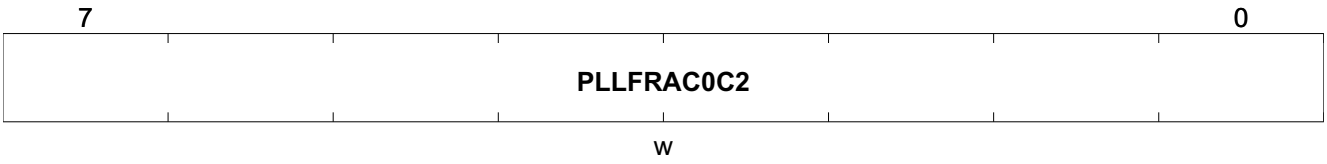
A_PLLINTC2	Offset	Reset Value
PLL MMD Integer Value Register Channel 2	**$06F_H$**	**13_H**



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
PLLINTC2	5:0	w	**SDPLL Multi Modulus Divider Integer Offset value for Channel 2** PLLINT(5:0) = dec2hex(INT(f_LO / f_XTAL)) Reset: 13_H

PLL Fractional Division Ratio Register 0 Channel 2

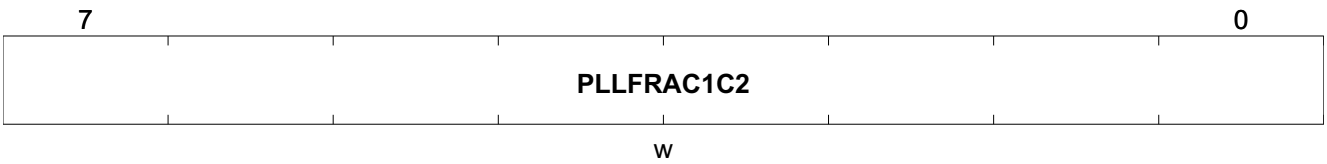
A_PLLFRAC0C2	Offset	Reset Value
PLL Fractional Division Ratio Register 0 Channel 2	**070_H**	**$F3_H$**



Field	Bits	Type	Description
PLLFRAC0C2	7:0	w	**Synthesizer channel frequency value (21 bits, bits 7:0), fractional division ratio for Channel 2** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: $F3_H$

PLL Fractional Division Ratio Register 1 Channel 2

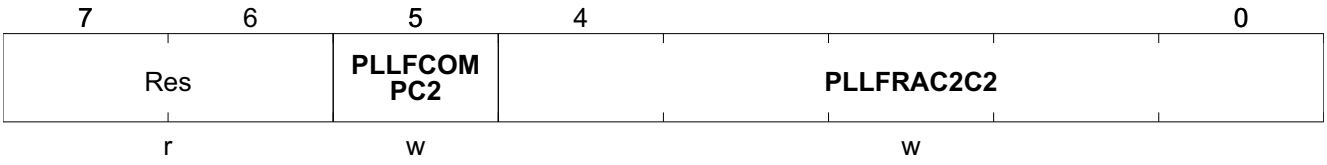
A_PLLFRAC1C2	Offset	Reset Value
PLL Fractional Division Ratio Register 1 Channel 2	**071_H**	**07_H**



Field	Bits	Type	Description
PLLFRAC1C2	7:0	w	**Synthesizer channel frequency value (21 bits, bits 15:8), fractional division ratio for Channel 2** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 07_H

PLL Fractional Division Ratio Register 2 Channel 2

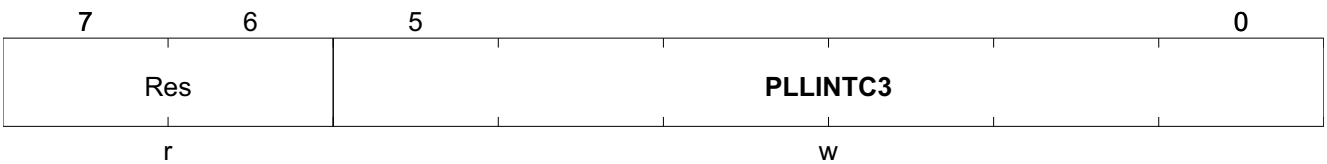
A_PLLFRAC2C2	Offset	Reset Value
PLL Fractional Division Ratio Register 2 Channel 2	**072_H**	**09_H**



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
PLLFCOMPC2	5	w	**Fractional Spurii Compensation enable for Channel 2** 0_B Disabled 1_B Enabled Reset: 0_H
PLLFRAC2C2	4:0	w	**Synthesizer channel frequency value (21 bits, bits 20:16), fractional division ratio for Channel 2** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 09_H

PLL MMD Integer Value Register Channel 3

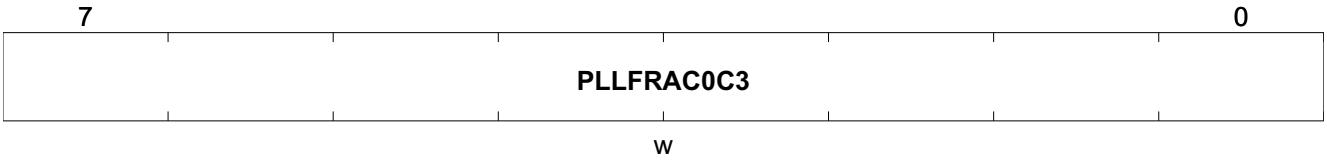
A_PLLINTC3	Offset	Reset Value
PLL MMD Integer Value Register Channel 3	**073_H**	**13_H**



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
PLLINTC3	5:0	w	**SDPLL Multi Modulus Divider Integer Offset value for Channel 3** PLLINT(5:0) = dec2hex(INT(f_LO / f_XTAL)) Reset: 13_H

PLL Fractional Division Ratio Register 0 Channel 3

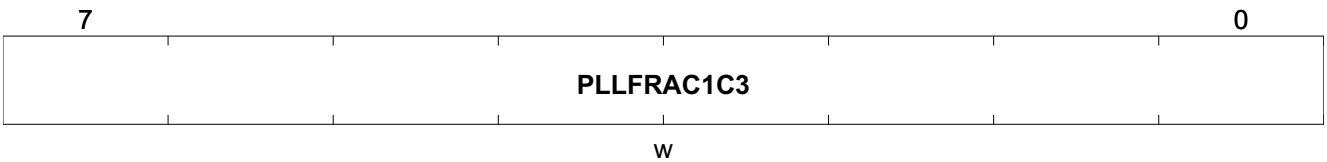
A_PLLFRAC0C3	Offset	Reset Value
PLL Fractional Division Ratio Register 0 Channel 3	**074_H**	**$F3_H$**



Field	Bits	Type	Description
PLLFRAC0C3	7:0	w	**Synthesizer channel frequency value (21 bits, bits 7:0), fractional division ratio for Channel 3** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: $F3_H$

PLL Fractional Division Ratio Register 1 Channel 3

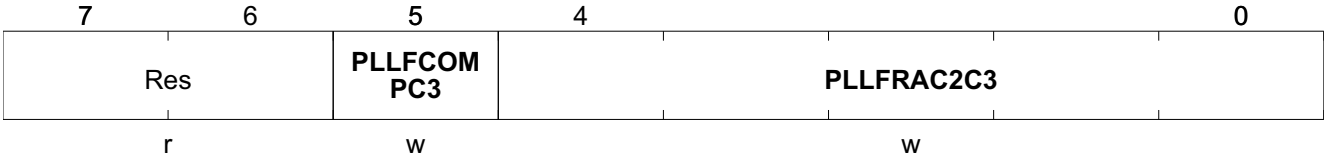
A_PLLFRAC1C3	Offset	Reset Value
PLL Fractional Division Ratio Register 1 Channel 3	**075_H**	**07_H**



Field	Bits	Type	Description
PLLFRAC1C3	7:0	w	**Synthesizer channel frequency value (21 bits, bits 15:8), fractional division ratio for Channel 3** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 07_H

PLL Fractional Division Ratio Register 2 Channel 3

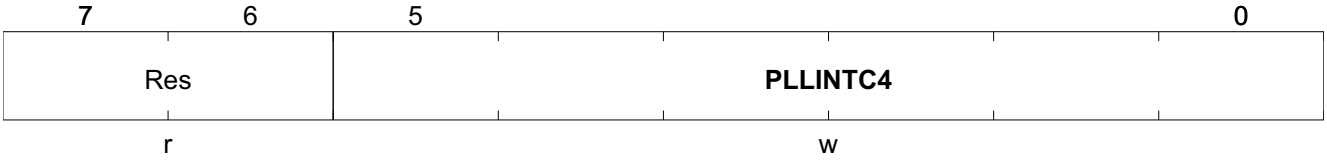
A_PLLFRAC2C3	Offset	Reset Value
PLL Fractional Division Ratio Register 2 Channel 3	076_H	09_H



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
PLLFCOMPC3	5	w	**Fractional Spurii Compensation enable for Channel 3** 0_B Disabled 1_B Enabled Reset: 0_H
PLLFRAC2C3	4:0	w	**Synthesizer channel frequency value (21 bits, bits 20:16), fractional division ratio for Channel 3** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 09_H

PLL MMD Integer Value Register Channel 4

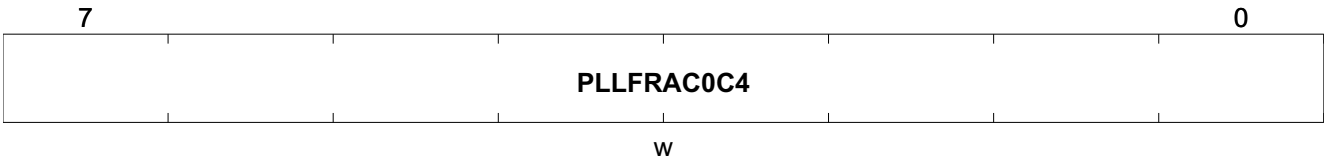
A_PLLINTC4	Offset	Reset Value
PLL MMD Integer Value Register Channel 4	077_H	13_H



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
PLLINTC4	5:0	w	**SDPLL Multi Modulus Divider Integer Offset value for Channel 4** PLLINT(5:0) = dec2hex(INT(f_LO / f_XTAL)) Reset: 13_H

PLL Fractional Division Ratio Register 0 Channel 4

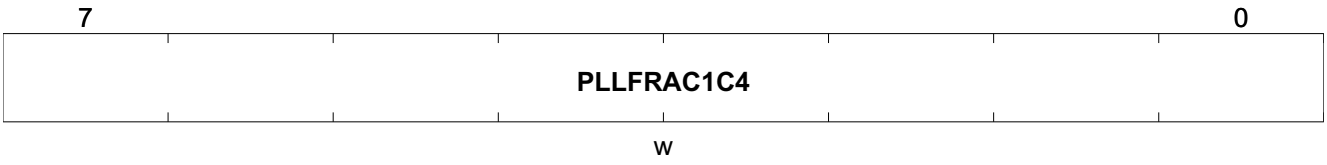
A_PLLFRAC0C4	Offset	Reset Value
PLL Fractional Division Ratio Register 0 Channel 4	078_H	$F3_H$



Field	Bits	Type	Description
PLLFRAC0C4	7:0	w	**Synthesizer channel frequency value (21 bits, bits 7:0), fractional division ratio for Channel 4** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: $F3_H$

PLL Fractional Division Ratio Register 1 Channel 4

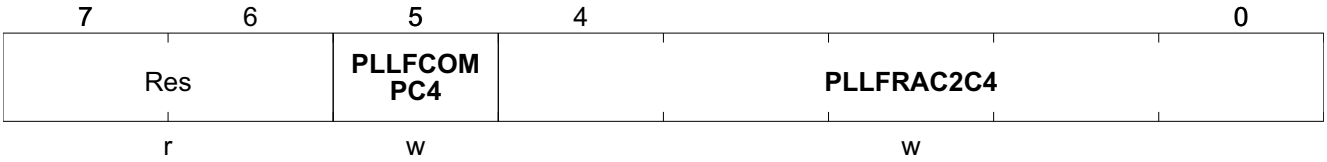
A_PLLFRAC1C4	Offset	Reset Value
PLL Fractional Division Ratio Register 1 Channel 4	079_H	07_H



Field	Bits	Type	Description
PLLFRAC1C4	7:0	w	**Synthesizer channel frequency value (21 bits, bits 15:8), fractional division ratio for Channel 4** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 07_H

PLL Fractional Division Ratio Register 2 Channel 4

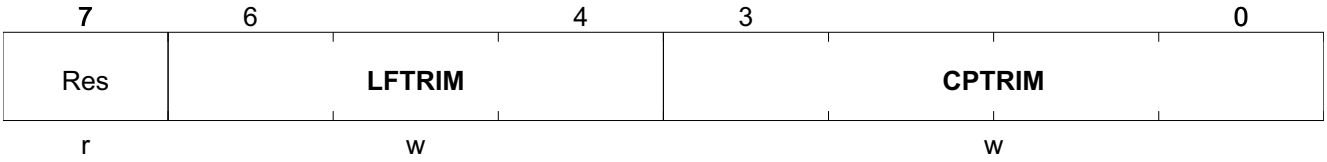
A_PLLFRAC2C4	Offset	Reset Value
PLL Fractional Division Ratio Register 2 Channel 4	$07A_H$	09_H



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
PLLFCOMPC4	5	w	**Fractional Spurii Compensation enable for Channel 3** 0_B Disabled 1_B Enabled Reset: 0_H
PLLFRAC2C4	4:0	w	**Synthesizer channel frequency value (21 bits, bits 20:16), fractional division ratio for Channel 3** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 09_H

PLL Bandwidth Selection Register for RX Mode

A_RXPLLBW	Offset	Reset Value
PLL Bandwidth Selection Register for RX Mode	**$07B_H$**	**$0C_H$**



Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H
LFTRIM	6:4	w	**PLL LF Trim value in RX mode** 000_B Rz = 9,94 kOhm, R4 = 3,92 kOhm 001_B Rz = 10,48 kOhm, R4 = 4,06 kOhm 010_B Rz = 11,38 kOhm, R4 = 4,44 kOhm 011_B Rz = 13,46 kOhm, R4 = 5,24 kOhm 100_B Rz = 15,26 kOhm, R4 = 6,04 kOhm 101_B Rz = 18,8 kOhm, R4 = 7,36 kOhm 110_B Rz = 26,64 kOhm, R4 = 10,6 kOhm 111_B Rz = 37,4 kOhm, R4 = 14,7 kOhm Reset: 0_H

Field	Bits	Type	Description
CPTRIM	3:0	w	**Charge Pump Current trimming in RX mode** Min: 0_H = 5uA Max F_H = 80uA Step: 5uA Reset: C_H

PLL Bandwidth Selection Register for TX Mode

A_TXPLLBW	Offset	Reset Value
PLL Bandwidth Selection Register for TX Mode	**$07C_H$**	**27_H**

7	6	4	3	0
Res	LFTRIM		CPTRIM	
r	w		w	

Field	Bits	Type	Description
Res	7	r	**for future use** Reset: 0_H
LFTRIM	6:4	w	**PLL LF Trim value in TX mode** 000_B Rz = 9,94 kOhm, R4 = 3,92 kOhm 001_B Rz = 10,48 kOhm, R4 = 4,06 kOhm 010_B Rz = 11,38 kOhm, R4 = 4,44 kOhm 011_B Rz = 13,46 kOhm, R4 = 5,24 kOhm 100_B Rz = 15,26 kOhm, R4 = 6,04 kOhm 101_B Rz = 18,8 kOhm, R4 = 7,36 kOhm 110_B Rz = 26,64 kOhm, R4 = 10,6 kOhm 111_B Rz = 37,4 kOhm, R4 = 14,7 kOhm Reset: 2_H
CPTRIM	3:0	w	**Charge Pump Current trimming in TX mode** Min: 0_H = 5uA Max F_H = 80uA Step: 5uA Reset: 7_H

PLL Startup Time Register

A_PLLTST	Offset	Reset Value
PLL Startup Time Register	**$07D_H$**	**$5B_H$**

7	6	5	3	2	0
VACRES		TXPLLTST		RXPLLTST	
w		w		w	

Field	Bits	Type	Description
VACRES	7:6	w	**VCO Autocalibration resolution** 00_B 14,6 MHz (not recommended) 01_B 7,3 MHz 10_B 4,4 MHz 11_B not used Reset: 1_H
TXPLLTST	5:3	w	**PLL Startup Time for TX Mode** Tst = (TXPLLTST * 8 + 11) * 64/Fsys Reset: 3_H
RXPLLTST	2:0	w	**PLL Startup Time for RX Mode** Tst = (RXPLLTST * 8 + 11) * 64/Fsys Reset: 3_H

Antenna Switch Configuration Register

A_ANTSW	Offset	Reset Value
Antenna Switch Configuration Register	$07E_H$	22_H

7	6	5	4	3	2	1	0
RXON2_INP	RXON2_INN	RXON2_EXSW1	RXON2_EXSW2	RXON1_INP	RXON1_INN	RXON1_EXSW1	RXON1_EXSW2
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RXON2_INP	7	w	**LNA INP switch configuration in RX mode if antenna 2 selected** 0_B Internal LNA switch open 1_B Internal LNA switch closed Reset: 0_H
RXON2_INN	6	w	**LNA INN switch configuration in RX mode if antenna 2 selected** 0_B Internal LNA switch open 1_B Internal LNA switch closed Reset: 0_H
RXON2_EXSW1	5	w	**External antenna switch 1 configuration in RX mode if antenna 2 selected** 0_B Level Low on PPx pin 1_B Level High on PPx pin Reset: 1_H

Field	Bits	Type	Description
RXON2_EXSW2	4	w	**External antenna switch 2 configuration in RX mode if antenna 2 selected** 0_B Level Low on PPx pin 1_B Level High on PPx pin Reset: 0_H
RXON1_INP	3	w	**LNA INP switch configuration in RX mode if antenna 1 selected** 0_B Internal LNA switch open 1_B Internal LNA switch closed Reset: 0_H
RXON1_INN	2	w	**LNA INN switch configuration in RX mode if antenna 1 selected** 0_B Internal LNA switch open 1_B Internal LNA switch closed Reset: 0_H
RXON1_EXSW1	1	w	**External antenna switch 1 configuration in RX mode if antenna 1 selected** 0_B Level Low on PPx pin 1_B Level High on PPx pin Reset: 1_H
RXON1_EXSW2	0	w	**External antenna switch 2 configuration in RX mode if antenna 1 selected** 0_B Level Low on PPx pin 1_B Level High on PPx pin Reset: 0_H

ADR Start/Freeze Configuration Register

A_ADRSFCFG	Offset	Reset Value
ADR Start/Freeze Configuration Register	**$07F_H$**	**00_H**

7	6	5	4	3	2	1	0
Res		**ADRUNFREEZE**		**ADRFREEZE**		**ADRSTART**	
r		w		w		w	

Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
ADRUNFREEZE	5:4	w	**ADR Unfreeze Configuration** 00_B No Unfreeze 01_B Unfreeze on NOT RSSI Event 10_B Unfreeze on NOT Signal Recognition Event 11_B Unfreeze on NOT Symbol Synchronization Reset: 0_H

Field	Bits	Type	Description
ADRFREEZE	3:2	w	**ADR Freeze Configuration** 00_B Stay ON 01_B Freeze on RSSI Event + Delay (A_AFCAGCADRD) 10_B Freeze on Signal Recognition Event + Delay (A_AFCAGCADRD) 11_B Freeze on Symbol Synchronization + Delay (A_AFCAGCADRD) Reset: 0_H
ADRSTART	1:0	w	**ADR Start Configuration** 00_B OFF 01_B Direct ON 10_B Start on RSSI event 11_B Start on Signal Recognition event Reset: 0_H

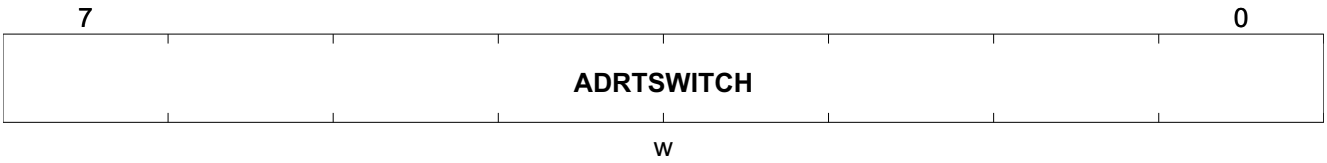
ADR Timeout Configuration Register 0

A_ADRTCFG0	Offset	Reset Value
ADR Timeout Configuration Register 0	**080_H**	**40_H**

Field	Bits	Type	Description
ADRTSEARCH	7:0	w	**ADR search timeout division factor (bits 7:0)** Resolution = Fsys/40/4 Reset: 40_H

ADR Timeout Configuration Register 1

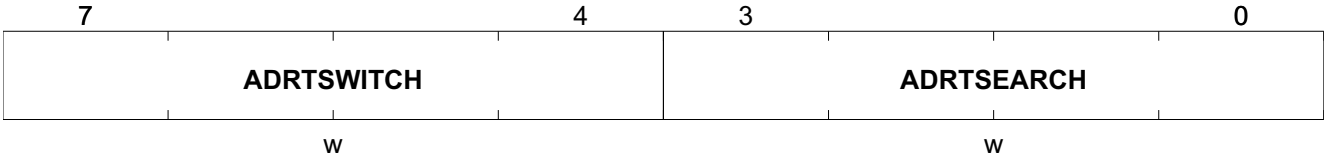
A_ADRTCFG1	Offset	Reset Value
ADR Timeout Configuration Register 1	**081_H**	**40_H**



Field	Bits	Type	Description
ADRTSWITCH	7:0	w	**ADR switch timeout division factor (bits 7:0)** Resolution = Fsys/40/4 Reset: 40_H

ADR Timeout Configuration Register 2

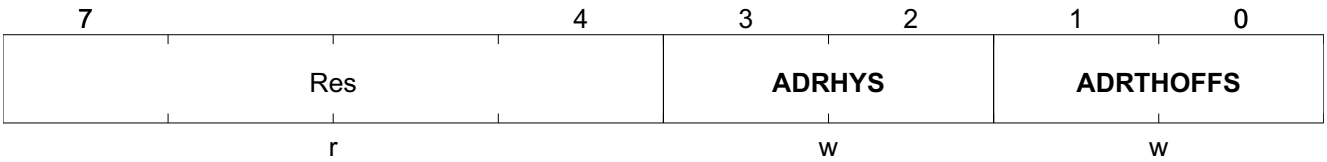
A_ADRTCFG2	Offset	Reset Value
ADR Timeout Configuration Register 2	**082_H**	**00_H**



Field	Bits	Type	Description
ADRTSWITCH	7:4	w	**ADR switch timeout division factor (bits 11:8)** Resolution = Fsys/40/4 Reset: 0_H
ADRTSEARCH	3:0	w	**ADR search timeout division factor (bits 11:8)** Resolution = Fsys/40/4 Reset: 0_H

ADR Threshold Register 0

A_ADRTHR0	Offset	Reset Value
ADR Threshold Register 0	**083_H**	**05_H**

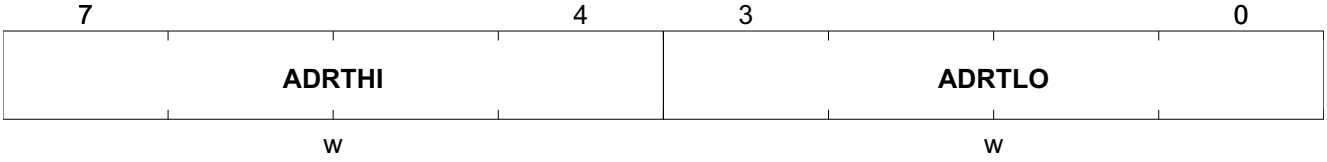


Field	Bits	Type	Description
Res	7:4	r	**for future use** Reset: 0_H

Field	Bits	Type	Description
ADRHYS	3:2	w	**ADR Threshold Hysteresis** 00_B 3.2 dB 01_B 6.4 dB 10_B 9.6 dB 11_B 12.8 dB Reset: 1_H
ADRTHOFFS	1:0	w	**ADR Threshold Offset** 00_B 12.8 dB 01_B 25.6 dB 10_B 38.4 dB 11_B 51.2 dB Reset: 1_H

ADR Threshold Register 1

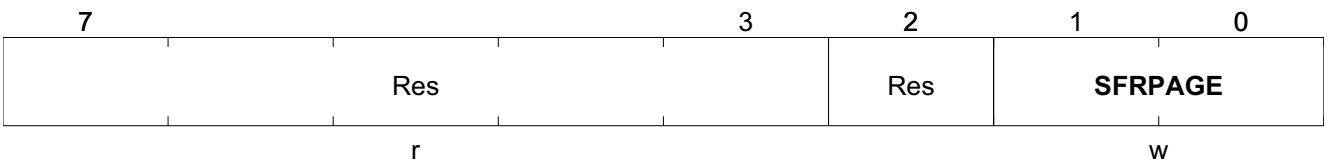
A_ADRTHR1	Offset	Reset Value
ADR Threshold Register 1	**084_H**	**84_H**



Field	Bits	Type	Description
ADRTHI	7:4	w	**ADR High Threshold [dB]** ADR High Threshold = A_ADRCFG.ADRTHOFFS + 12.8 + ADRTHI*3.2 Reset: 8_H
ADRTLO	3:0	w	**ADR Low Threshold [dB]** ADR Low Threshold = A_ADRCFG.ADRTHOFFS + ADRTLO*3.2 Reset: 4_H

Special Function Register Page Register

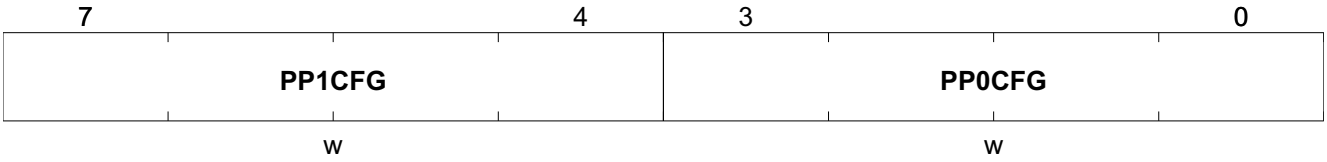
SFRPAGE	Offset	Reset Value
Special Function Register Page Register	**$0A0_H$**	**00_H**



Field	Bits	Type	Description
Res	7:3	r	**for future use** Reset: 00_H
SFRPAGE	1:0	w	**Selection of Register Page File (Configuration A..D) for SPI communication** 00_B Page 0 (Config. A, start address: 000_H) 01_B Page 1 (Config. B, start address: 100_H) 10_B Page 2 (Config. C, start address: 200_H) 11_B Page 3 (Config. D, start address: 300_H) Reset: 0_H

PP0 and PP1 Configuration Register

PPCFG0	Offset	Reset Value
PP0 and PP1 Configuration Register	**$0A1_H$**	**50_H**

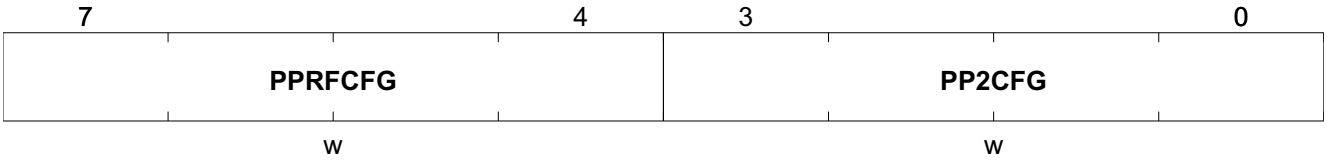


Field	Bits	Type	Description
PP1CFG	7:4	w	**Port Pin 1 Output Signal Selection** 0000_B CLK_OUT 0001_B RX_RUN 0010_B NINT 0011_B ANT_EXTSW1 0100_B ANT_EXTSW2 0101_B DATA 0110_B DATA_MATCHFIL 0111_B LOW 1000_B CH_DATA 1001_B CH_STR 1010_B RXD 1011_B RXSTR 1100_B TXSTR 1101_B HIGH 1110_B n.u. 1111_B TRISTATE Reset: 5_H

Field	Bits	Type	Description
PP0CFG	3:0	w	**Port Pin 0 Output Signal Selection** 0000_B CLK_OUT 0001_B RX_RUN 0010_B NINT 0011_B ANT_EXTSW1 0100_B ANT_EXTSW2 0101_B DATA 0110_B DATA_MATCHFIL 0111_B LOW 1000_B CH_DATA 1001_B CH_STR 1010_B RXD 1011_B RXSTR 1100_B TXSTR 1101_B HIGH 1110_B n.u. 1111_B TRISTATE Reset: 0_H

PP2 and PPRF Configuration Register

PPCFG1	Offset	Reset Value
PP2 and PPRF Configuration Register	$0A2_H$	$F2_H$



Field	Bits	Type	Description
PPRFCFG	7:4	w	**Port Pin RF Output Signal Selection** 0000_B n.u. 0001_B RX_RUN 0010_B NINT 0011_B ANT_EXTSW1 0100_B ANT_EXTSW2 0101_B DATA 0110_B DATA_MATCHFIL 0111_B LOW 1000_B CH_DATA 1001_B CH_STR 1010_B RXD 1011_B RXSTR 1100_B TXSTR 1101_B HIGH 1110_B n.u. 1111_B TRISTATE Reset: F_H
PP2CFG	3:0	w	**Port Pin 2 Output Signal Selection** 0000_B CLK_OUT 0001_B RX_RUN 0010_B NINT 0011_B ANT_EXTSW1 0100_B ANT_EXTSW2 0101_B DATA 0110_B DATA_MATCHFIL 0111_B LOW 1000_B CH_DATA 1001_B CH_STR 1010_B RXD 1011_B RXSTR 1100_B TXSTR 1101_B HIGH 1110_B n.u. 1111_B TRISTATE Reset: 2_H

PPx Port Configuration Register

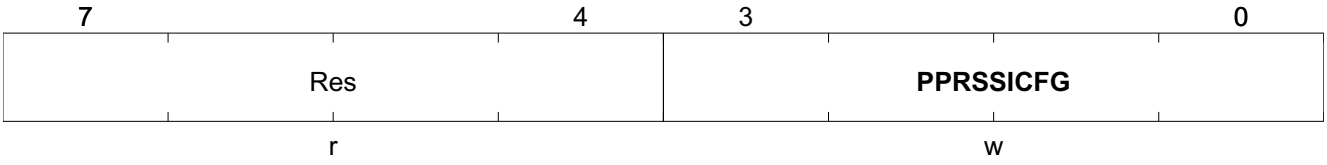
PPCFG2	Offset	Reset Value
PPx Port Configuration Register	**$0A3_H$**	**00_H**

7	6	5	4	3	2	1	0
PPRFHPPEN	PP2HPPEN	PP1HPPEN	PP0HPPEN	PPRFINV	PP2INV	PP1INV	PP0INV
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PPRFHPPEN	7	w	**PPRF High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP2HPPEN	6	w	**PP2 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP1HPPEN	5	w	**PP1 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP0HPPEN	4	w	**PP0 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PPRFINV	3	w	**PPRF Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H
PP2INV	2	w	**PP2 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H
PP1INV	1	w	**PP1 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H
PP0INV	0	w	**PP0 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H

PPRF_RSSI Configuration Register

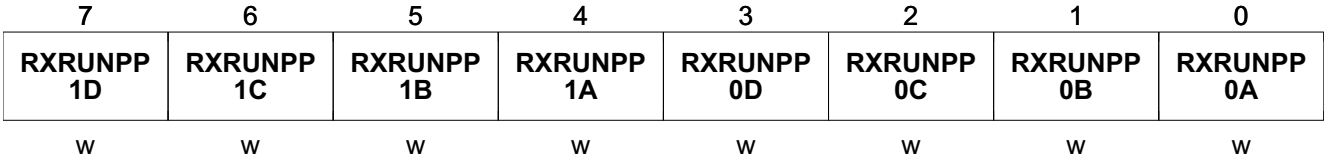
PPCFG3	Offset	Reset Value
PPRF_RSSI Configuration Register	$0A4_H$	$0F_H$



Field	Bits	Type	Description
Res	7:4	r	**for future use** Reset: 0_H
PPRSSICFG	3:0	w	**Port Pin PPRF_RSSI Output Signal Selection** 0000_B n.u. 0001_B RX_RUN 0010_B NINT 0011_B ANT_EXTSW1 0100_B ANT_EXTSW2 0101_B DATA 0110_B DATA_MATCHFIL 0111_B LOW 1000_B CH_DATA 1001_B CH_STR 1010_B RXD 1011_B RXSTR 1100_B TXSTR 1101_B HIGH 1110_B n.u. 1111_B TRISTATE Reset: F_H

RX RUN Configuration Register 0

RXRUNCFG0	Offset	Reset Value
RX RUN Configuration Register 0	**$0A5_H$**	**FF_H**



Field	Bits	Type	Description
RXRUNPP1D	7	w	**RXRUN Active Level on PP1 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H

Field	Bits	Type	Description
RXRUNPP1C	6	w	**RXRUN Active Level on PP1 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP1B	5	w	**RXRUN Active Level on PP1 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP1A	4	w	**RXRUN Active Level on PP1 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0D	3	w	**RXRUN Active Level on PP0 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0C	2	w	**RXRUN Active Level on PP0 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0B	1	w	**RXRUN Active Level on PP0 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0A	0	w	**RXRUN Active Level on PP0 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H

RX RUN Configuration Register 1

RXRUNCFG1	Offset	Reset Value
RX RUN Configuration Register 1	**$0A6_H$**	**FF_H**

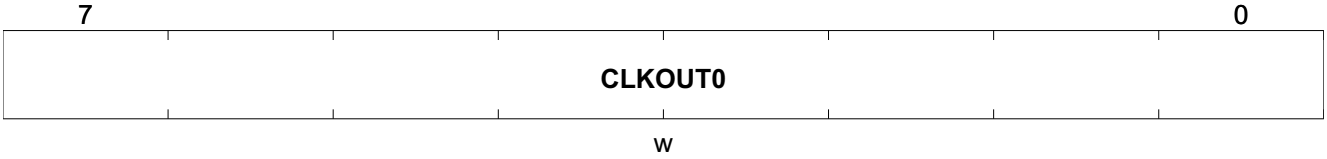
7	6	5	4	3	2	1	0
RXRUNPP 3D	**RXRUNPP 3C**	**RXRUNPP 3B**	**RXRUNPP 3A**	**RXRUNPP 2D**	**RXRUNPP 2C**	**RXRUNPP 2B**	**RXRUNPP 2A**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RXRUNPP3D	7	w	**RXRUN Active Level on PP3 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H

Field	Bits	Type	Description
RXRUNPP3C	6	w	**RXRUN Active Level on PP3 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP3B	5	w	**RXRUN Active Level on PP3 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP3A	4	w	**RXRUN Active Level on PP3 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2D	3	w	**RXRUN Active Level on PP2 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2C	2	w	**RXRUN Active Level on PP2 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2B	1	w	**RXRUN Active Level on PP2 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2A	0	w	**RXRUN Active Level on PP2 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H

Clock Divider Register 0

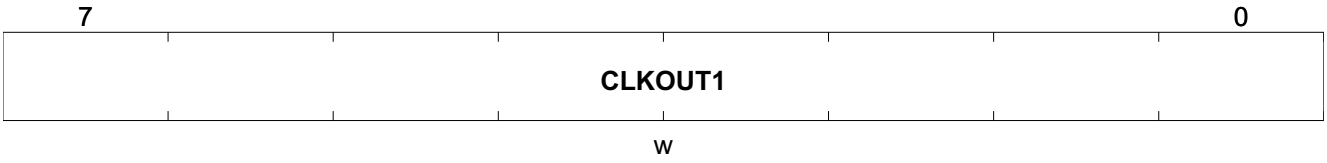
CLKOUT0	Offset	Reset Value
Clock Divider Register 0	**$0A7_H$**	**$0B_H$**



Field	Bits	Type	Description
CLKOUT0	7:0	w	**Clock Out Divider: CLKOUT(19:0) = CLKOUT2(MSB) & CLKOUT1 & CLKOUT0(LSB)** Min: 00002h = Clock divided by 2*2 Max: FFFFFh = Clock divided by ((2^20)-1)*2 Reg. value 00000h = Clock divided by (2^20)*2 Reset: $0B_H$

Clock Divider Register 1

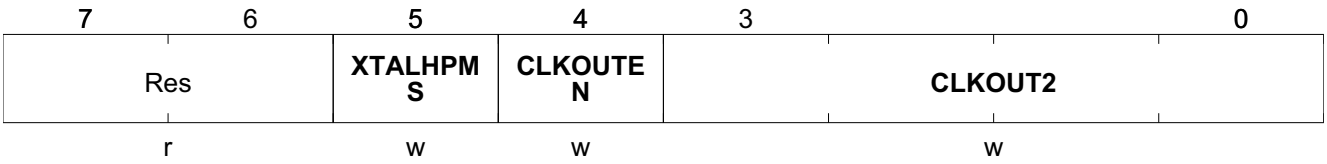
CLKOUT1	Offset	Reset Value
Clock Divider Register 1	**$0A8_H$**	**00_H**



Field	Bits	Type	Description
CLKOUT1	7:0	w	**Clock Out Divider: CLKOUT(19:0) = CLKOUT2(MSB) & CLKOUT1 & CLKOUT0(LSB)** Min: 00002h = Clock divided by 2*2 Max: FFFFFh = Clock divided by ((2^20)-1)*2 Reg. value 00000h = Clock divided by (2^20)*2 Reset: 00_H

Clock Divider Register 2

CLKOUT2	Offset	Reset Value
Clock Divider Register 2	**$0A9_H$**	**10_H**



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H

Field	Bits	Type	Description
XTALHPMS	5	w	**XTAL High Precision Mode in Sleep Mode** 0_B Disabled 1_B Enabled Reset: 0_H
CLKOUTEN	4	w	**CLK_OUT Enable** 0_B Disabled 1_B Enable programmable clock output Reset: 1_H
CLKOUT2	3:0	w	**Clock Out Divider: CLKOUT(19:0) = CLKOUT2(MSB) & CLKOUT1 & CLKOUT0(LSB)** Min: 00002h = Clock divided by 2*2 Max: FFFFFh = Clock divided by ((2^20)-1)*2 Reg. value 00000h = Clock divided by (2^20)*2 Reset: 0_H

Antenna Switch Configuration Register

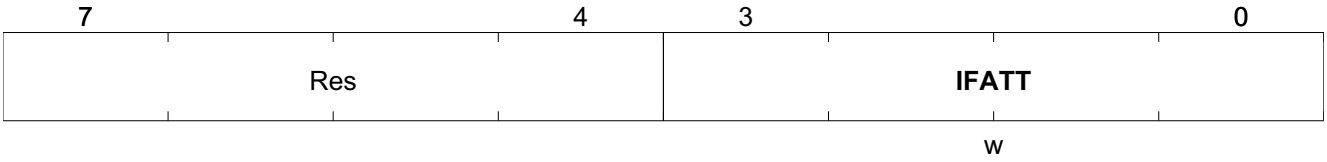
ANTSW	Offset	Reset Value
Antenna Switch Configuration Register	$0AA_H$	$1D_H$

7	6	5	4	3	2	1	0
Res				TX_INP	TX_INN	TX_EXSW1	TX_EXSW2
				w	w	w	w

Field	Bits	Type	Description
TX_INP	3	w	**LNA INP switch configuration in TX mode** 0_B Internal LNA switch open 1_B Internal LNA switch closed Reset: 1_H
TX_INN	2	w	**LNA INN switch configuration in TX mode** 0_B Internal LNA switch open 1_B Internal LNA switch closed Reset: 1_H
TX_EXSW1	1	w	**External antenna switch 1 configuration in TX mode** 0_B Level Low on PPx pin 1_B Level High on PPx pin Reset: 0_H
TX_EXSW2	0	w	**External antenna switch 2 configuration in TX mode** 0_B Level Low on PPx pin 1_B Level High on PPx pin Reset: 1_H

RF Control Register

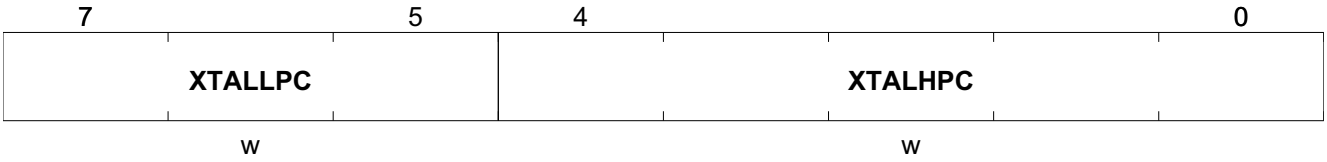
RFC	Offset	Reset Value
RF Control Register	$0AB_H$	$E7_H$



Field	Bits	Type	Description
IFATT	3:0	w	**Adjust IF attenuation from LNA_IN to IF_OUT (Double-Down Conversion / Single-Down Conversion)** 0000_B 0 dB / n.u. 0001_B 0.8 dB / n.u. 0010_B 1.6 dB / n.u. 0011_B 2.4 dB / n.u. 0100_B 3.2 dB / 0 dB 0101_B 4.0 dB / 0.8 dB 0110_B 4.8 dB / 1.6 dB 0111_B 5.6 dB / 2.4 dB 1000_B 6.4 dB / 3.2 dB 1001_B 7.2 dB / 4.0 dB 1010_B 8.0 dB / 4.8 dB 1011_B 8.8 dB / n.u. 1100_B 9.6 dB / n.u. 1101_B 10.4 dB / n.u. 1110_B 11.2 dB / n.u. 1111_B 12.0 dB / n.u. Reset: 7_H

XTAL Coarse Calibration Register

XTALCAL0	Offset	Reset Value
XTAL Coarse Calibration Register	$0AE_H$	90_H



Field	Bits	Type	Description
XTALLPC	7:5	w	**XTAL Low Precision Mode Capacitor Value** Min 0h: 0pF Max 7h: 7pF Reset: 4_H
XTALHPC	4:0	w	**XTAL High Precision Mode Capacitor Value** Min 00h: 0pF Value 01h: 1pF Max 18h: 24pF higher values than 18h are automatically mapped to 24pF Reset: 10_H

XTAL Fine Calibration Register

XTALCAL1	Offset	Reset Value
XTAL Fine Calibration Register	$0AF_H$	00_H

7	6	5	4	3	2	1	0
Res				XTALSWF3	XTALSWF2	XTALSWF1	XTALSWF0
r				w	w	w	w

Field	Bits	Type	Description
Res	7:4	r	**for future use** Reset: 0_H
XTALSWF3	3	w	**Connect 500 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H
XTALSWF2	2	w	**Connect 250 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H
XTALSWF1	1	w	**Connect 125 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H
XTALSWF0	0	w	**Connect 62.5 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H

RSSI Configuration Register

RSSICFG	Offset	Reset Value
RSSI Configuration Register	$0B0_H$	10_H

7	6	5	3	2	1	0
Res	Res	AGCDGC		Res		RSSIMONEN
	r	w				w

Field	Bits	Type	Description
Res	6	r	**for future use** Reset: 0_H
AGCDGC	5:3	w	**AGC Digital RSSI Gain Correction Tuning** 000_B 14.5 dB 001_B 15.0 dB 010_B 15.5 dB 011_B 16.0 dB 100_B 16.5 dB 101_B 17.0 dB 110_B 17.5 dB 111_B 18.0 dB Reset: 2_H
RSSIMONEN	0	w	**Enable Buffer for RSSI pin** 0_B Disabled 1_B Enabled Reset: 0_H

ADC Input Selection Register

ADCINSEL	Offset	Reset Value
ADC Input Selection Register	$0B1_H$	00_H

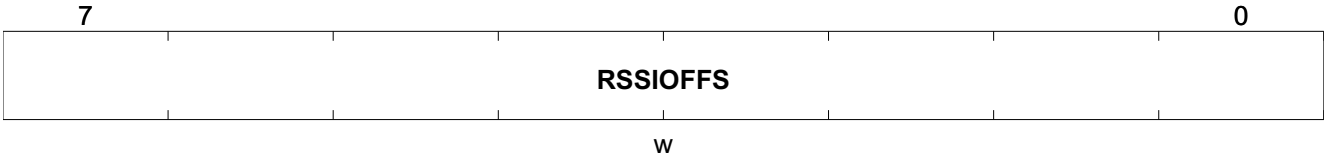
7	3	2	0
Res		ADCINSEL	
r		w	

Field	Bits	Type	Description
Res	7:3	r	**for future use** Reset: 00_H

Field	Bits	Type	Description
ADCINSEL	2:0	w	**ADC Input Selection** 000_B RSSI 001_B Temperature 010_B VDDD / 2 011_B n.u. 100_B n.u. 101_B n.u. 110_B n.u. 111_B n.u. Reset: 0_H

RSSI Offset Register

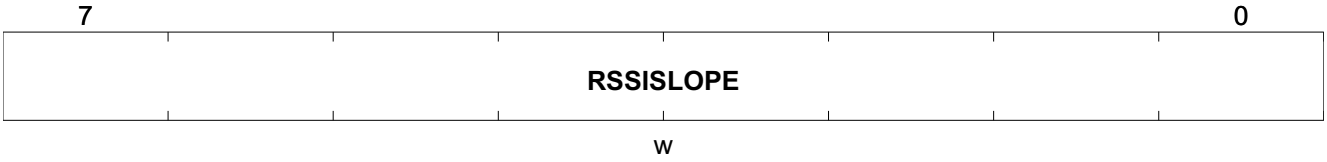
RSSIOFFS	Offset	Reset Value
RSSI Offset Register	**$0B2_H$**	**80_H**



Field	Bits	Type	Description
RSSIOFFS	7:0	w	**RSSI Offset Compensation Value** Min: 00h= -256 Max: FFh= 254 Reset: 80_H

RSSI Slope Register

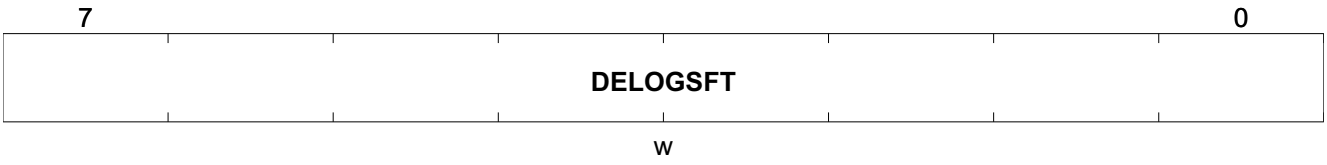
RSSISLOPE	Offset	Reset Value
RSSI Slope Register	**$0B3_H$**	**80_H**



Field	Bits	Type	Description
RSSISLOPE	7:0	w	**RSSI Slope Compensation Value (Multiplication Value)** Multiplication Factor = RSSISLOPE * 2^-7 Min: 00h= 0.0 Max: FFh= 1.992 Reset: 80_H

DELOG Shift Register

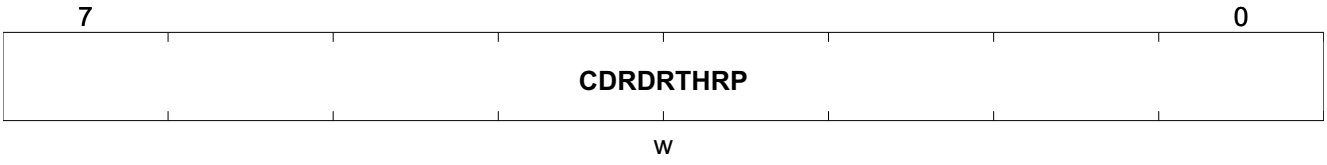
DELOGSFT	Offset	Reset Value
DELOG Shift Register	**$0B4_H$**	**00_H**



Field	Bits	Type	Description
DELOGSFT	7:0	w	**DELOG Shift Value (2's complement)** Range -128/+ 127 Reset: 00_H

CDR Data Rate Acceptance Positive Threshold Register

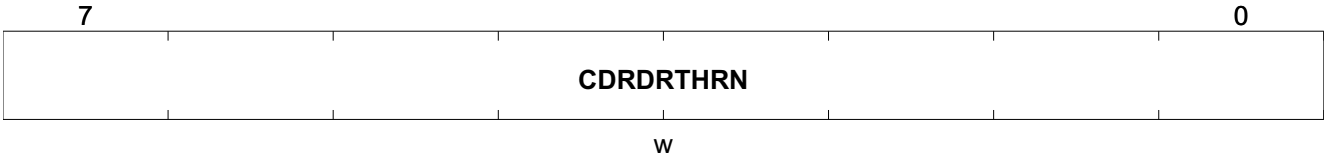
CDRDRTHRP	Offset	Reset Value
CDR Data Rate Acceptance Positive Threshold Register	**$0B5_H$**	**$1E_H$**



Field	Bits	Type	Description
CDRDRTHRP	7:0	w	**Data Rate Acceptance Positive Threshold Value** This feature can be turned on with *_CDRRI.DRLIMEN. Higher the value, more percent of the datarate is tolerated. Default => 10% Reset: $1E_H$

CDR Data Rate Acceptance Negative Threshold Register

CDRDRTHRN	Offset	Reset Value
CDR Data Rate Acceptance Negative Threshold Register	$0B6_H$	23_H



Field	Bits	Type	Description
CDRDRTHRN	7:0	w	**Data Rate Acceptance Negative Threshold Value** This feature can be turned on with *_CDRRI.DRLIMEN. Higher the value, more percent of the datarate is tolerated. Default => 10% Reset: 23_H

Interrupt Mask Register 0

IM0	Offset	Reset Value
Interrupt Mask Register 0	$0B7_H$	00_H

7	6	5	4	3	2	1	0
IMEOMB	IMMIDFB	IMFSYNCB	IMWUB	IMEOMA	IMMIDFA	IMFSYNCA	IMWUA
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
IMEOMB	7	w	**Mask Interrupt on "End of Message" for Configuration B** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMMIDFB	6	w	**Mask Interrupt on "Message ID Found" for Configuration B** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMFSYNCB	5	w	**Mask Interrupt on "Frame Sync" for Configuration B** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Field	Bits	Type	Description
IMWUB	4	w	**Mask Interrupt on "Wake-up" for Configuration B** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMEOMA	3	w	**Mask Interrupt on "End of Message" for Configuration A** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMMIDFA	2	w	**Mask Interrupt on "Message ID Found" for Configuration A** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMFSYNCA	1	w	**Mask Interrupt on "Frame Sync" for Configuration A** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMWUA	0	w	**Mask Interrupt on "Wake-up" for Configuration A** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Interrupt Mask Register 1

IM1	Offset	Reset Value
Interrupt Mask Register 1	**$0B8_H$**	**00_H**

7	6	5	4	3	2	1	0
IMEOMD	**IMMIDFD**	**IMFSYNCD**	**IMWUD**	**IMEOMC**	**IMMIDFC**	**IMFSYNCC**	**IMWUC**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
IMEOMD	7	w	**Mask Interrupt on "End of Message" for Configuration D** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMMIDFD	6	w	**Mask Interrupt on "Message ID Found" for Configuration D** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMFSYNCD	5	w	**Mask Interrupt on "Frame Sync" for Configuration D** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Field	Bits	Type	Description
IMWUD	4	w	**Mask Interrupt on "Wake-up" for Configuration D** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMEOMC	3	w	**Mask Interrupt on "End of Message" for Configuration C** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMMIDFC	2	w	**Mask Interrupt on "Message ID Found" for Configuration C** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMFSYNCC	1	w	**Mask Interrupt on "Frame Sync" for Configuration C** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMWUC	0	w	**Mask Interrupt on "Wake-up" for Configuration C** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Interrupt Mask Register 2

IM2	Offset	Reset Value
Interrupt Mask Register 2	**$0B9_H$**	**00_H**

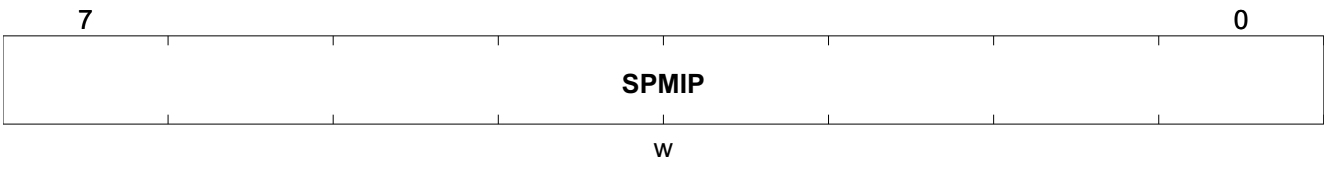
7	6	5	4	3	2	1	0
IMTXE	**IMTXR**	**IMTXDS**	**IMTXAF**	**IMTXAE**	**IMTXEMPTY**	**IMSYSRDY**	**IMRXAF**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
IMTXE	7	w	**Mask Interrupt on "TX Error"** PLL out of lock or VAC error 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMTXR	6	w	**Mask Interrupt on "TX Ready"** The PLL calibration is finalized and the transmitter is now ready to start the transmission. 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Field	Bits	Type	Description
IMTXDS	5	w	**Mask Interrupt on "TX Data Strobe"** New data request in transparent TX mode if baudrate synchronization enabled 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMTXAF	4	w	**Mask Interrupt on "TX FIFO Almost Full"** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMTXAE	3	w	**Mask Interrupt on "TX FIFO Almost Empty"** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMTXEMPTY	2	w	**Mask Interrupt on "TX FIFO Empty"** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMSYSRDY	1	w	**Mask Interrupt on "System Ready"** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMRXAF	0	w	**Mask Interrupt on "RX FIFO Almost Full"** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Self Polling Mode Idle Periods Register

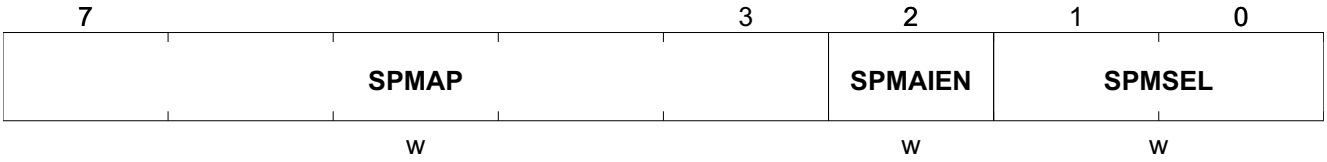
SPMIP	Offset	Reset Value
Self Polling Mode Idle Periods Register	**$0BA_H$**	**01_H**



Field	Bits	Type	Description
SPMIP	7:0	w	**Self Polling Mode Idle Periods value** Min: 01h = 1 (Master) Period Max: FFh = 255 (Master) Periods Reg. value 00h = 256 (Master) Periods Reset: 01_H

Self Polling Mode Control Register

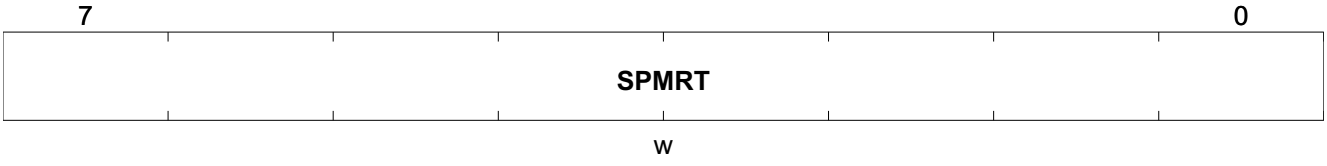
SPMC	Offset	Reset Value
Self Polling Mode Control Register	$0BB_H$	08_H



Field	Bits	Type	Description
SPMAP	7:3	w	**Self Polling Mode Active Periods value** Min: 01h = 1 (Master) Period Max: 1Fh = 31(Master) Periods Reg. value 00h = 32 (Master) Periods Reset: 01_H
SPMAIEN	2	w	**Self Polling Mode Active Idle Enable** 0_B Disabled 1_B Enabled Reset: 0_H
SPMSEL	1:0	w	**Self Polling Mode Selection** 00_B Constant On/Off (COO) 01_B Fast Fall Back to Sleep (FFB) 10_B Mixed Mode (MM, Combination of Const On/Off and Fast Fall Back to Sleep for different Configurations: COO, FFB, FFB, FFB) 11_B Permanent Wake Up Search (PWUS) Reset: 0_H

Self Polling Mode Reference Timer Register

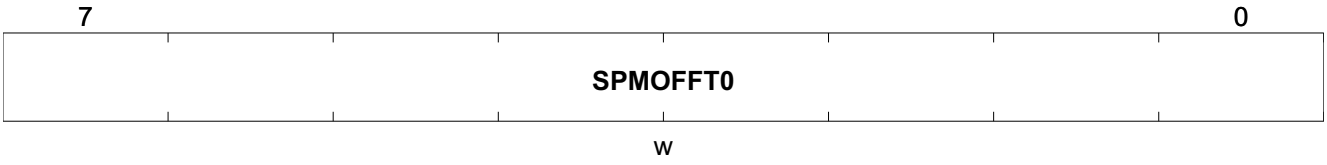
SPMRT	Offset	Reset Value
Self Polling Mode Reference Timer Register	$0BC_H$	01_H



Field	Bits	Type	Description
SPMRT	7:0	w	**Self Polling Mode Reference Timer value** The output of this timer is used as input for the On/Off Timer Incoming Periodic Time = 64 / fsys Output Periodic Time = TRT = (64 * SPMRT) / fsys Min: 01h = (64*1) / fsys Max: 00h = (64 * 256) / fsys Reset: 01_H

Self Polling Mode Off Time Register 0

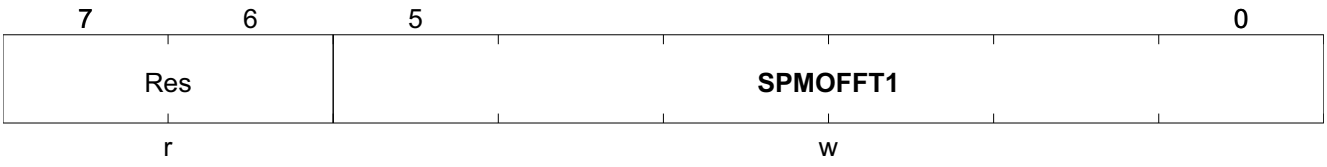
SPMOFFT0	Offset	Reset Value
Self Polling Mode Off Time Register 0	**$0BD_H$**	**01_H**



Field	Bits	Type	Description
SPMOFFT0	7:0	w	**Self Polling Mode Off Time value: SPMOFFT(13:0) = SPMOFFT1(MSB) & SPMOFFT0(LSB)** Off -Time = TRT * SPMOFFT Min: 0001h = 1 * TRT Reg.Value 3FFFh = 16383 * TRT Max: 0000h = 16384 * TRT Reset: 01_H

Self Polling Mode Off Time Register 1

SPMOFFT1	Offset	Reset Value
Self Polling Mode Off Time Register 1	**$0BE_H$**	**00_H**

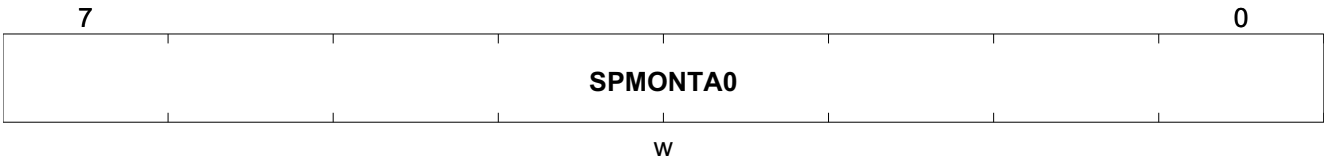


Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H

Field	Bits	Type	Description
SPMOFFT1	5:0	w	**Self Polling Mode Off Time value: SPMOFFT(13:0) = SPMOFFT1(MSB) & SPMOFFT0(LSB)** Off -Time = TRT * SPMOFFT Min: 0001h = 1 * TRT Reg.Value 3FFFh = 16383 * TRT Max: 0000h = 16384 * TRT Reset: 00_H

Self Polling Mode On Time Config A Register 0

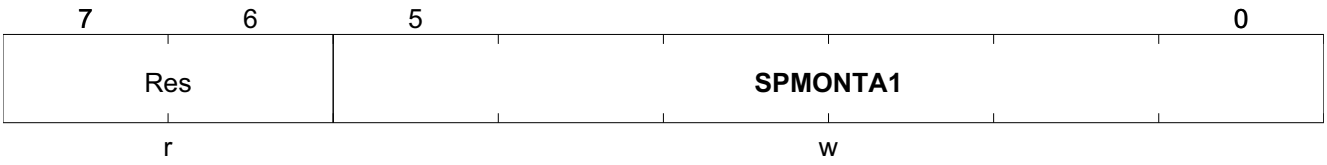
SPMONTA0	Offset	Reset Value
Self Polling Mode On Time Config A Register 0	**$0BF_H$**	**01_H**



Field	Bits	Type	Description
SPMONTA0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTA(13:0) = SPMONTA1(MSB) & SPMONTA0(LSB)** On-Time = TRT *SPMONTA Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config A Register 1

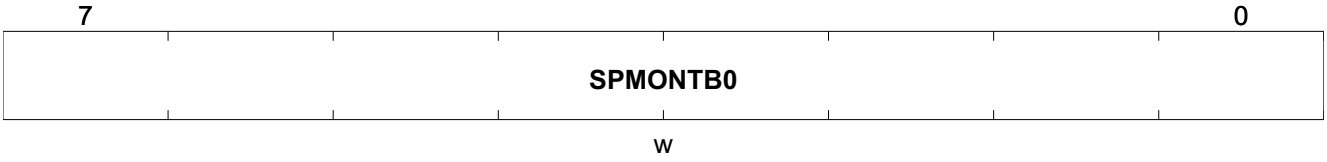
SPMONTA1	Offset	Reset Value
Self Polling Mode On Time Config A Register 1	**$0C0_H$**	**00_H**



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
SPMONTA1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTA(13:0) = SPMONTA1(MSB) & SPMONTA0(LSB)** On-Time = TRT *SPMONTA Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

Self Polling Mode On Time Config B Register 0

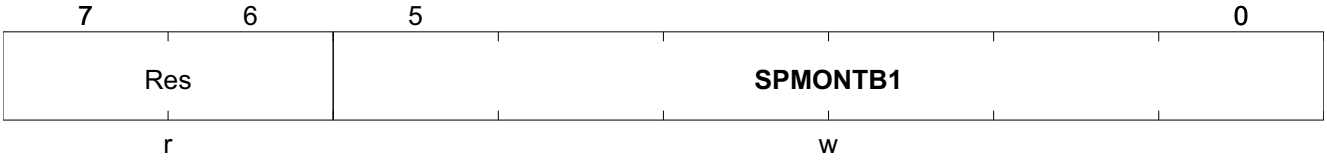
SPMONTB0	Offset	Reset Value
Self Polling Mode On Time Config B Register 0	**$0C1_H$**	**01_H**



Field	Bits	Type	Description
SPMONTB0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTB(13:0) = SPMONTB1(MSB) & SPMONTB0(LSB)** On-Time = TRT *SPMONTB Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config B Register 1

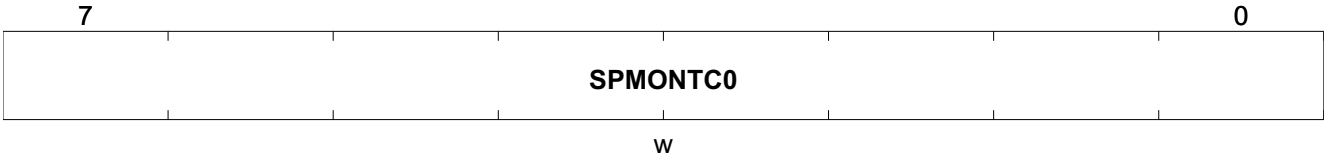
SPMONTB1	Offset	Reset Value
Self Polling Mode On Time Config B Register 1	**$0C2_H$**	**00_H**



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
SPMONTB1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTB(13:0) = SPMONTB1(MSB) & SPMONTB0(LSB)** On-Time = TRT *SPMONTB Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

Self Polling Mode On Time Config C Register 0

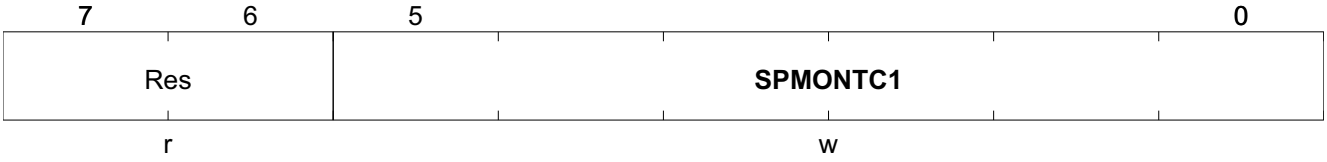
SPMONTC0	Offset	Reset Value
Self Polling Mode On Time Config C Register 0	**$0C3_H$**	**01_H**



Field	Bits	Type	Description
SPMONTC0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTC(13:0) = SPMONTC1(MSB) & SPMONTC0(LSB)** On-Time = TRT *SPMONTC Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config C Register 1

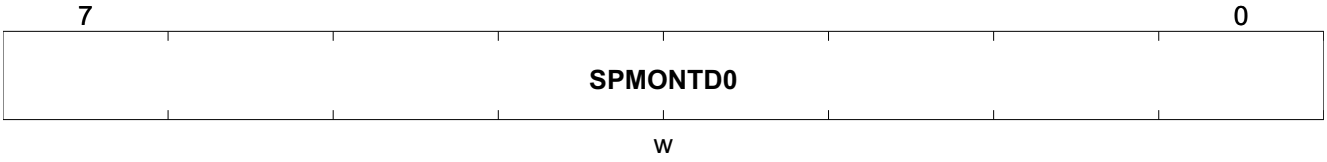
SPMONTC1	Offset	Reset Value
Self Polling Mode On Time Config C Register 1	**$0C4_H$**	**00_H**



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
SPMONTC1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTC(13:0) = SPMONTC1(MSB) & SPMONTC0(LSB)** On-Time = TRT *SPMONTC Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

Self Polling Mode On Time Config D Register 0

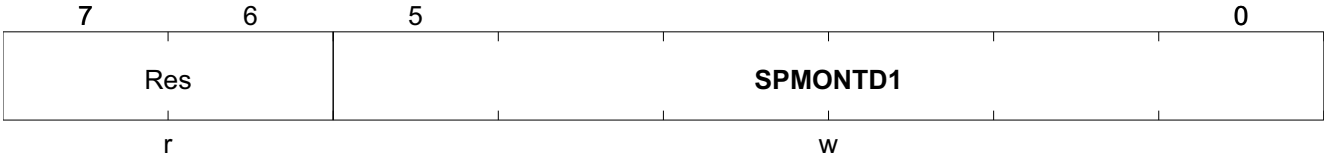
SPMONTD0	Offset	Reset Value
Self Polling Mode On Time Config D Register 0	**$0C5_H$**	**01_H**



Field	Bits	Type	Description
SPMONTD0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTD(13:0) = SPMONTD1(MSB) & SPMONTD0(LSB)** On-Time = TRT *SPMONTD Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config D Register 1

SPMONTD1	Offset	Reset Value
Self Polling Mode On Time Config D Register 1	**$0C6_H$**	**00_H**



Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
SPMONTD1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTD(13:0) = SPMONTD1(MSB) & SPMONTD0(LSB)** On-Time = TRT *SPMONTD Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

External Processing Command Register

EXTPCMD	Offset	Reset Value
External Processing Command Register	**$0C7_H$**	**00_H**

7	6	5	4	3	2	1	0
ADRMANUF	**AGCMANUF**	**AFCMANUF**	**ADRMANF**	**AGCMANF**	**AFCMANF**	**EXTTOTIM**	**EXTWUEOM**
wc	wc	wc	wc	wc	wc	wc	wc

Field	Bits	Type	Description
ADRMANUF	7	wc	**ADR Manual Unfreeze** 0_B Inactive 1_B Active Reset: 0_H
AGCMANUF	6	wc	**AGC Manual Unfreeze** 0_B Inactive 1_B Active Reset: 0_H
AFCMANUF	5	wc	**AFC Manual Unfreeze** 0_B Inactive 1_B Active Reset: 0_H
ADRMANF	4	wc	**ADR Manual Freeze** 0_B Inactive 1_B Active Reset: 0_H
AGCMANF	3	wc	**AGC Manual Freeze** 0_B Inactive 1_B Active Reset: 0_H

Field	Bits	Type	Description
AFCMANF	2	wc	**AFC Manual Freeze** 0_B Inactive 1_B Active Reset: 0_H
EXTTOTIM	1	wc	**Force TOTIM signal** 0_B no external TOTIM signal forced 1_B external TOTIM signal forced Reset: 0_H
EXTWUEOM	0	wc	**Force Wakeup / EOM signal** 0_B no external Wakeup / EOM signal forced 1_B external Wakeup / EOM signal forced Reset: 0_H

TX Control Register

TXC	Offset	Reset Value
TX Control Register	$0C8_H$	01_H

7	6	5	4	3	2	1	0
TXSTART	TXPLLINIT	INITTXFIFO	TXBDRSYNCT	TXMODE	TXTOIDLE	TXENDFIFO	TXFAILSAFE
wc	wc	wc	w	w	w	w	w

Field	Bits	Type	Description
TXSTART	7	wc	**TX start bit** Used in Start bit mode 0_B TX not started 1_B TX started Reset: 0_H
TXPLLINIT	6	wc	**TX PLL init at channel change** Only possible out of "TX idle" and "TX ready" states 0_B TX and PLL not initialized 1_B TX and PLL initialized Reset: 0_H
INITTXFIFO	5	wc	**Init the TX FIFO** 0_B No TX FIFO init 1_B TX FIFO init Reset: 0_H
TXBDRSYNCT	4	w	**Synchronization with baudrate generator in Transparent mode** Encoder can be activated in this mode as well 0_B Disabled 1_B Enabled Reset: 0_H

Field	Bits	Type	Description
TXMODE	3	w	**Transmission start selection** 0_B Direct mode with TXFIFO (TXFIFO not empty) 1_B Start bit mode with TXFIFO (TXSTART = 1) Reset: 0_H
TXTOIDLE	2	w	**Go to IDLE after TX** In IDLE state PA and PLL are switched off 0_B Wait for new transmission 1_B Go to IDLE after TX finished Reset: 0_H
TXENDFIFO	1	w	**Finish TX with FIFO empty** Used to change power, modulation, data rate, encoding,... 0_B TX continues after FIFO empty (waiting for FIFO not empty or Start bit) 1_B TX finished with FIFO empty Reset: 0_H
TXFAILSAFE	0	w	**Enable Failsafe mechanism in TX mode** 0_B Disabled 1_B Enabled Reset: 1_H

RX Control Register

RXC	Offset	Reset Value
RX Control Register	**$0C9_H$**	**84_H**

7	6	5	4	3	2	1	0
Res	**INITPLL HOLD**	**EOM2NCF G**	**TOTIM2N CH**	**INITRXF IFO**	**FSINITR XFIFO**	**RXFIFOL K**	**HOLD**
	w	w	w	w	w	w	w

Field	Bits	Type	Description
INITPLLHOLD	6	w	**Init PLL after coming from HOLD (required at channel change).** This requires an additional Channel Hop Time before initialization of the Digital Receiver. 0_B No init of PLL 1_B Init of PLL Reset: 0_H
EOM2NCFG	5	w	**Continue with next Configuration in Self Polling Mode after EOM detected in Run Mode Self Polling** 0_B Continue with Configuration A in Self Polling Mode 1_B Continue with next Configuration in Self Polling Mode Reset: 0_H

Field	Bits	Type	Description
TOTIM2NCH	4	w	**Continue with next RF channel in Self Polling Mode after TOTIM detected in Run Mode Self Polling. In case of single RF channel application this means "continue with next Configuration" instead of "continue with next RF channel".** 0_B Continue with Configuration A in Self Polling Mode 1_B Continue with next RF channel in Self Polling Mode Reset: 0_H
INITRXFIFO	3	w	**Initialization of the RX FIFO at Cycle Start** This Initialization of the RX FIFO can be configured in both Run Mode Slave and Self Polling Mode. In Run Mode Slave this happens at the beginning. In Self Polling Mode the initialization is done after Wake up found (switching from Self Polling Mode to Run Mode Self Polling). 0_B Initialization disabled 1_B Initialization enabled Reset: 0_H
FSINITRXFIFO	2	w	**Initialization of the RX FIFO at Frame Start** 0_B Initialization disabled 1_B Initialization enabled Reset: 1_H
RXFIFOLK	1	w	**Lock Data in RX FIFO at EOM** 0_B RX FIFO lock is disabled 1_B RX FIFO lock is enabled at EOM Reset: 0_H
HOLD	0	w	**Holds the chip in the Register Configuration state (only in Run Mode Slave)** 0_B Normal Operation 1_B Jump into the Register Config state Hold Reset: 0_H

Chip Mode Control Register

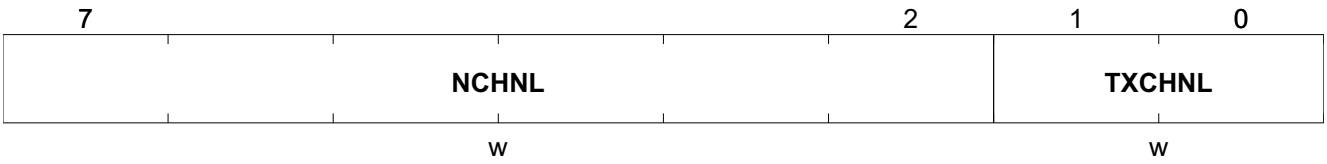
CMC	Offset	Reset Value
Chip Mode Control Register	$0CA_H$	10_H

7	6	5	4	3	2	1	0
INITMCU	SDOHPPEN	DSLEEPEN	ENBOD	MCS		MSEL	
wc	w	w	w	w		w	

Field	Bits	Type	Description
INITMCU	7	wc	**Init the MCU (go to VREG_EN state). Used to re-enter the same mode selected by the MSEL bit.** Note: Not recommended for SLEEP mode re-entering. 0_B No MCU init 1_B Init MCU Reset: 0_H
SDOHPPEN	6	w	**SDO High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
DSLEEPEN	5	w	**Deep Sleep Mode enable** Deep Sleep Mode entered only if Sleep Mode selected with MSEL bits 0_B Disabled 1_B Enabled Reset: 0_H
ENBOD	4	w	**Enable brown out detector** 0_B Disabled 1_B Enabled Reset: 1_H
MCS	3:2	w	**Multi Configuration Selection (Run Mode Slave / Self Polling Mode / Transmit)** 00_B Config A / Config A / Config A 01_B Config B / Config A + B / Config B 10_B Config C / Config A + B + C / Config C 11_B Config D / Config A + B + C + D / Config D Reset: 0_H
MSEL	1:0	w	**Operating Mode Selection** 00_B Sleep Mode 01_B Self Polling Mode 10_B Run Mode Slave 11_B Transmit Mode Reset: 0_H

TX Channel Configuration Register

TXCHNL	Offset	Reset Value
TX Channel Configuration Register	$0CB_H$	00_H



Field	Bits	Type	Description
NCHNL	7:2	w	**Channel offset number (N)** TX frequency = base channel + N * offset 000000_B Selected TX base channel (N = 0) 001111_B N Reset: 00_H
TXCHNL	1:0	w	**TX base channel selection** Defines the base of the channel frequency for the selected configuration (CMC.MCS) 00_B Channel 1 01_B Channel 2 10_B Channel 3 11_B Channel 4 Reset: 0_H

PLL Configuration Register

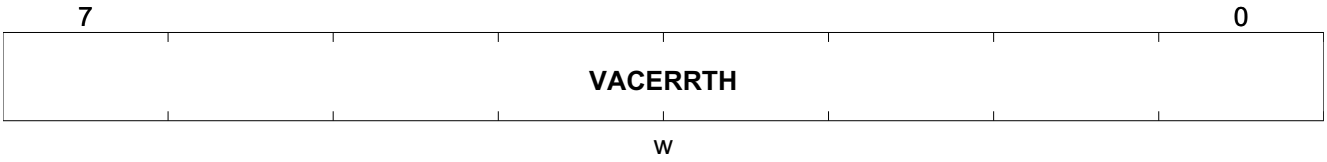
PLLCFG	Offset	Reset Value
PLL Configuration Register	$0CC_H$	28_H

7	6	5	4	3	0
Res		VCOCCUREN	PLLLDEN	PLLLDTHR	
r		w	w	w	

Field	Bits	Type	Description
Res	7:6	r	**for future use** Reset: 0_H
VCOCCUREN	5	w	**Enable VCO constant current** 0_B Disabled 1_B Enabled Reset: 1_H
PLLLDEN	4	w	**Enable PLL lock detector** 0_B Disabled 1_B Enabled Reset: 0_H
PLLLDTHR	3:0	w	**PLL lock detector threshold** Defines the threshold for the error counter (0 = allways error detected) Reset: 8_H

VCO Autocalibration Error Threshold

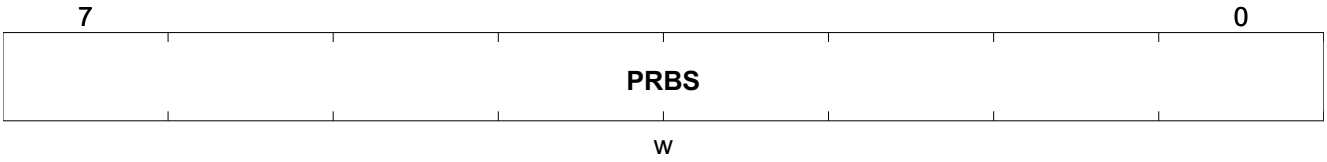
VACERRTH	Offset	Reset Value
VCO Autocalibration Error Threshold	$0CD_H$	00_H



Field	Bits	Type	Description
VACERRTH	7:0	w	**VCO Autocalibration Error Threshold** Value 00_H : disabled Reset: 00_H

PRBS Starting Value Register

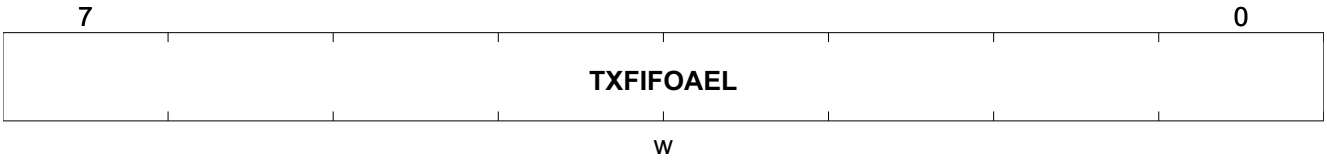
PRBS	Offset	Reset Value
PRBS Starting Value Register	$0CE_H$	50_H



Field	Bits	Type	Description
PRBS	7:0	w	**PRBS Starting Value** Only used if Data scrambling is enabled Reset: 50_H

TX FIFO Almost Empty Level Register

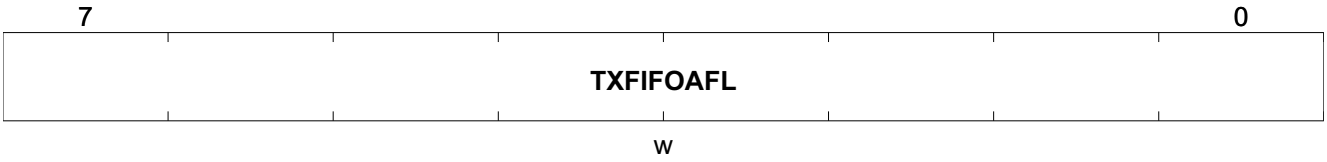
TXFIFOAEL	Offset	Reset Value
TX FIFO Almost Empty Level Register	$0CF_H$	00_H



Field	Bits	Type	Description
TXFIFOAEL	7:0	w	**TX FIFO Almost Empty Level** Reset: 00_H

TX FIFO Almost Full Level Register

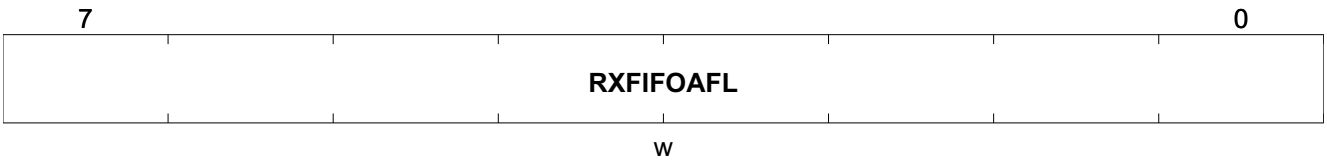
TXFIFOAFL	Offset	Reset Value
TX FIFO Almost Full Level Register	**$0D0_H$**	**00_H**



Field	Bits	Type	Description
TXFIFOAFL	7:0	w	**TX FIFO Almost Full Level** Value represents the distance to the upper boundary of the TX FIFO Reset: 00_H

RX FIFO Almost Full Level Register

RXFIFOAFL	Offset	Reset Value
RX FIFO Almost Full Level Register	**$0D1_H$**	**00_H**



Field	Bits	Type	Description
RXFIFOAFL	7:0	w	**RX FIFO Almost Full Level** Value represents the distance to the upper boundary of the RX FIFO Reset: 00_H

PLL Status Register

PLLSTAT	Offset	Reset Value
PLL Status Register	**$0D2_H$**	**00_H**

7	6	5	4				0
TXFIFOERR	VACERR	LOCKDETERR	VCORANGE				
rc	rc	rc	r				

Field	Bits	Type	Description
TXFIFOERR	7	rc	**TXFIFO Error** 0_B TXFIFO OK 1_B TXFIFO Error Reset: 0_H
VACERR	6	rc	**VAC error** 0_B VAC OK 1_B VAC failed Reset: 0_H
LOCKDETERR	5	rc	**PLL lock error** 0_B PLL locked 1_B PLL not locked Reset: 0_H
VCORANGE	4:0	r	**VCO Range selected by VCO Autocalibration Routine** Reset: 00_H

Interrupt Status Register 2

IS2	Offset	Reset Value
Interrupt Status Register 2	$0D3_H$	FF_H

7	6	5	4	3	2	1	0
TXE	TXR	TXDS	TXAF	TXAE	TXEMPTY	SYSRDY	RXAF
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
TXE	7	rc	**Interrupt Request by "TX Error" (Reset event sets all Bits to 1)** PLL out of lock or VAC error 0_B Not detected 1_B Detected Reset: 1_H
TXR	6	rc	**Interrupt Request by "TX Ready" (Reset event sets all Bits to 1)** The PLL calibration is finalized and the transmitter is now ready to start the transmission. 0_B Not detected 1_B Detected Reset: 1_H

Field	Bits	Type	Description
TXDS	5	rc	**Interrupt Request by "TX Data Strobe" (Reset event sets all Bits to 1)** New data request in transparent TX mode if baudrate synchronization enabled 0_B Not detected 1_B Detected Reset: 1_H
TXAF	4	rc	**Interrupt Request by "TX FIFO Almost Full" (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
TXAE	3	rc	**Interrupt Request by "TX FIFO Almost Empty" (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
TXEMPTY	2	rc	**Interrupt Request by "TX FIFO Empty" (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
SYSRDY	1	rc	**Interrupt Request by "System Ready" (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
RXAF	0	rc	**Interrupt Request by "RX FIFO Almost Full" (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H

Interrupt Status Register 0

IS0	Offset	Reset Value
Interrupt Status Register 0	$0D4_H$	FF_H

7	6	5	4	3	2	1	0
EOMB	MIDFB	FSYNCB	WUB	EOMA	MIDFA	FSYNCA	WUA
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
EOMB	7	rc	**Interrupt Request by "End of Message" from Configuration B (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
MIDFB	6	rc	**Interrupt Request by "Message ID Found" from Configuration B (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
FSYNCB	5	rc	**Interrupt Request by "Frame Sync" from Configuration B (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
WUB	4	rc	**Interrupt Request by "Wake Up" from Configuration B (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
EOMA	3	rc	**Interrupt Request by "End of Message" from Configuration A (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
MIDFA	2	rc	**Interrupt Request by "Message ID Found" from Configuration A (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
FSYNCA	1	rc	**Interrupt Request by "Frame Sync" from Configuration A (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
WUA	0	rc	**Interrupt Request by "Wake Up" from Configuration A (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H

Interrupt Status Register 1

IS1	Offset	Reset Value
Interrupt Status Register 1	$0D5_H$	FF_H

7	6	5	4	3	2	1	0
EOMD	MIDFD	FSYNCD	WUD	EOMC	MIDFC	FSYNCC	WUC
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
EOMD	7	rc	**Interrupt Request by "End of Message" from Configuration D (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
MIDFD	6	rc	**Interrupt Request by "Message ID Found" from Configuration D (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
FSYNCD	5	rc	**Interrupt Request by "Frame Sync" from Configuration D (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
WUD	4	rc	**Interrupt Request by "Wake Up" from Configuration D (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
EOMC	3	rc	**Interrupt Request by "End of Message" from Configuration C (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
MIDFC	2	rc	**Interrupt Request by "Message ID Found" from Configuration C (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
FSYNCC	1	rc	**Interrupt Request by "Frame Sync" from Configuration C (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H

Field	Bits	Type	Description
WUC	0	rc	**Interrupt Request by "Wake Up" from Configuration C (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H

RF PLL Actual Channel and Configuration Register

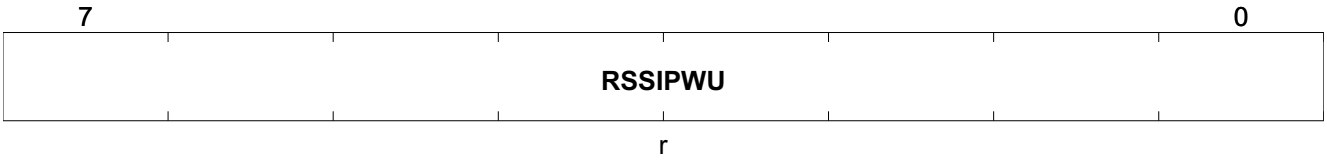
RFPLLACC	Offset	Reset Value
RF PLL Actual Channel and Configuration Register	**$0D6_H$**	**00_H**

7	6	5	4	3	2	1	0
PLDLEN		**RMSPACFG**		**RMSPAC**		**SPMAC**	
r		r		r		r	

Field	Bits	Type	Description
PLDLEN	7:6	r	**Payload Data Length stored at TSI detection of the next message, PLDLEN(9:0) = RFPLLACC.PLDLEN(MSB) & PLDLEN(LSB).** Cleared with INIT RX FIFO Min. 000h = 0 bits received Max. 3FFh = 1023 bits received Reset: 0_H
RMSPACFG	5:4	r	**RF PLL Run Mode Self Polling Actual Configuration** 00_B Configuration A 01_B Configuration B 10_B Configuration C 11_B Configuration D Reset: 0_H
RMSPAC	3:2	r	**RF PLL Run Mode Self Polling Actual Channel** Only valid after the first EOM Interrupt 00_B Data in FIFO belong to Channel 1 01_B Data in FIFO belong to Channel 2 10_B Data in FIFO belong to Channel 3 11_B Data in FIFO belong to Channel 4 Reset: 0_H
SPMAC	1:0	r	**RF PLL Self Polling Mode Actual Channel** Only valid after the first Wake-up Interrupt 00_B Wake Up was found from Channel 1 01_B Wake Up was found from Channel 2 10_B Wake Up was found from Channel 3 11_B Wake Up was found from Channel 4 Reset: 0_H

Wakeup Peak Detector Readout Register

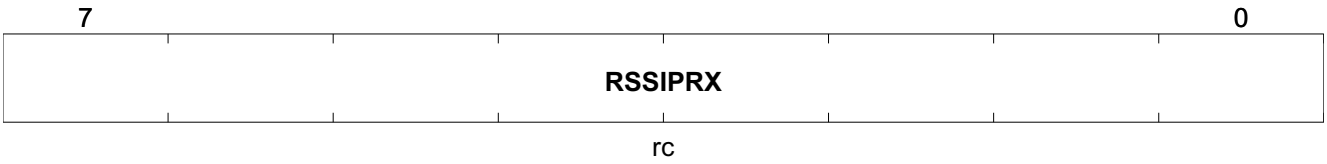
RSSIPWU	Offset	Reset Value
Wakeup Peak Detector Readout Register	$0D7_H$	00_H



Field	Bits	Type	Description
RSSIPWU	7:0	r	**Peak Detector Level at Wakeup** Set at every WU event and also set at the end of every configuration/channel cycle within a Self Polling period. Cleared at Reset only. Reset: 00_H

RSSI Peak Detector Readout Register

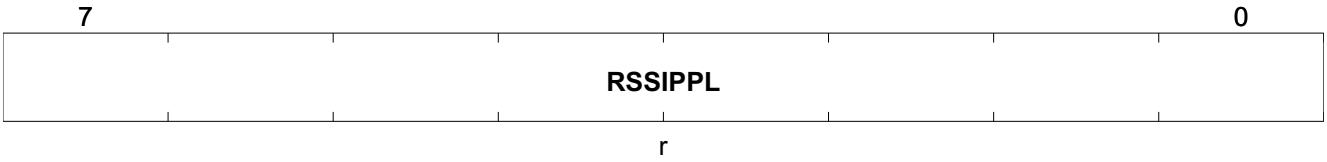
RSSIPRX	Offset	Reset Value
RSSI Peak Detector Readout Register	$0D8_H$	00_H



Field	Bits	Type	Description
RSSIPRX	7:0	rc	**RSSI Peak Level during Receiving** Tracking is active when Digital Receiver is enabled Set at higher peak levels than stored Cleared at Reset and SPI read out Reset: 00_H

RSSI Payload Peak Detector Readout Register

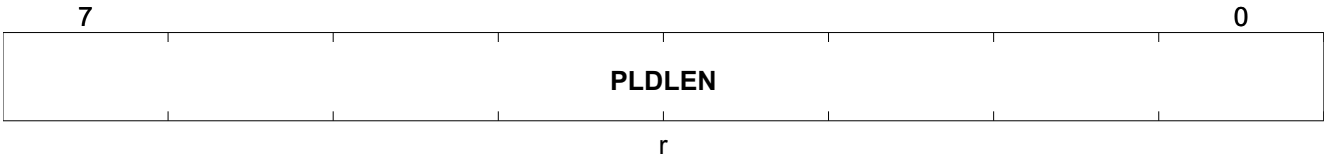
RSSIPPL	Offset	Reset Value
RSSI Payload Peak Detector Readout Register	$0D9_H$	00_H



Field	Bits	Type	Description
RSSIPPL	7:0	r	**RSSI Peak Level during Payload** Tracking starts after FSYNC + PKBITPOS Set at every EOM Cleared at the Reset only Reset: 00_H

Payload Data Length Register

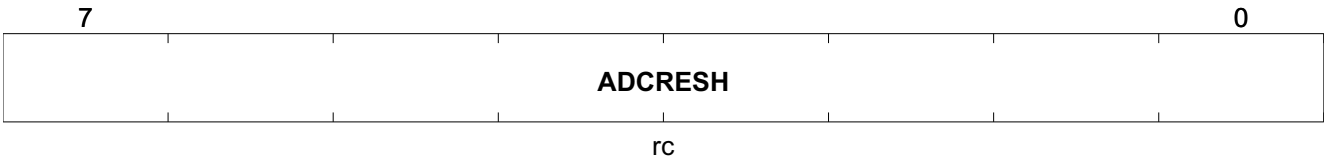
PLDLEN	Offset	Reset Value
Payload Data Length Register	**$0DA_H$**	**00_H**



Field	Bits	Type	Description
PLDLEN	7:0	r	**Payload Data Length stored at TSI detection of the next message, PLDLEN(9:0) = RFPLLACC.PLDLEN(MSB) & PLDLEN(LSB).** Cleared with INIT FIFO Min. 000h = 0 bits received Max. 3FFh = 1023 bits received Reset: 00_H

ADC Result High Byte Register

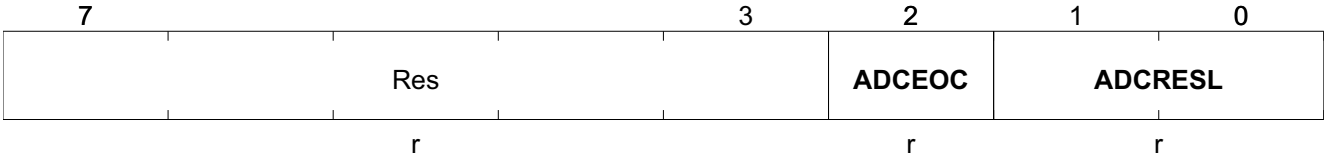
ADCRESH	Offset	Reset Value
ADC Result High Byte Register	**$0DB_H$**	**00_H**



Field	Bits	Type	Description
ADCRESH	7:0	rc	**ADC Result Value ADCRES(9:0) = ADCRESH(7:0) & ADCRESL(1:0)** Note: RC for control signal generation only, no clear Reset: 00_H

ADC Result Low Byte Register

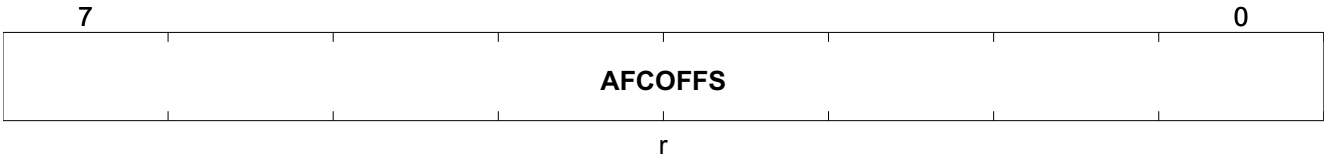
ADCRESL	Offset	Reset Value
ADC Result Low Byte Register	**$0DC_H$**	**00_H**



Field	Bits	Type	Description
Res	7:3	r	**for future use** Reset: 00_H
ADCEOC	2	r	**ADC End of Conversion detected** 0_B not detected 1_B detected Reset: 0_H
ADCRESL	1:0	r	**ADC Result Value ADCRES(9:0) = ADCRESH(7:0) & ADCRESL(1:0)** Reset: 0_H

AFC Offset Read Register

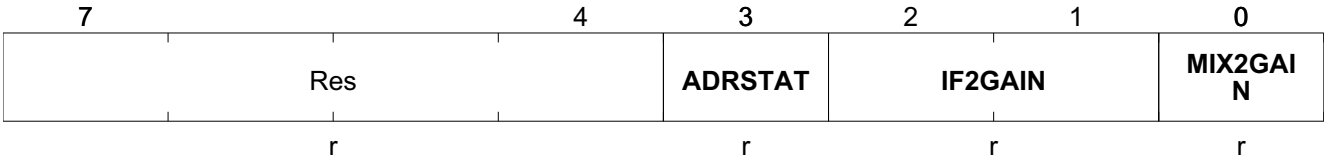
AFCOFFSET	Offset	Reset Value
AFC Offset Read Register	**$0DD_H$**	**00_H**



Field	Bits	Type	Description
AFCOFFS	7:0	r	**Readout of the Frequency Offset found by AFC (AFC loop filter output).** Value is in signed representation. Frequency resolution is 2.68 kHz/digit Output can be limited by x_AFCLIMIT register Update rate is 548 kHz Reset: 00_H

AGC and ADR Readout Register

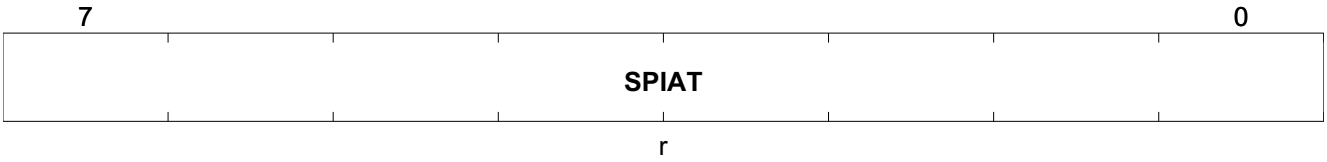
AGCADRR	Offset	Reset Value
AGC and ADR Readout Register	**$0DE_H$**	**00_H**



Field	Bits	Type	Description
Res	7:4	r	**for future use** Reset: 0_H
ADRSTAT	3	r	**ADR Status - selected antenna** 0_B Antenna 1 selected 1_B Antenna 2 selected Reset: 0_H
IF2GAIN	2:1	r	**AGC IF2 Gain Readout** 00_B 0 dB 01_B -15 dB 10_B -30 dB 11_B n.u. Reset: 0_H
MIX2GAIN	0	r	**AGC MIX2 Gain Readout** 0_B 0 dB 1_B -15 dB Reset: 0_H

SPI Address Tracer Register

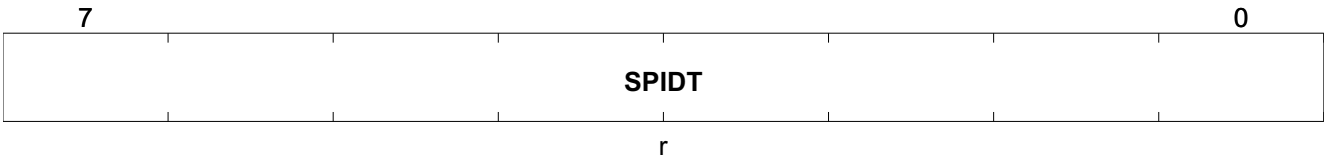
SPIAT	Offset	Reset Value
SPI Address Tracer Register	**$0DF_H$**	**00_H**



Field	Bits	Type	Description
SPIAT	7:0	r	**SPI Address Tracer, Readout of the last address of a SFR Register written by SPI** Reset: 00_H

SPI Data Tracer Register

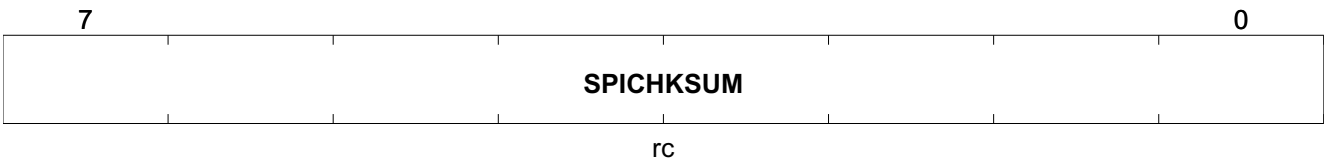
SPIDT	Offset	Reset Value
SPI Data Tracer Register	**$0E0_H$**	**00_H**



Field	Bits	Type	Description
SPIDT	7:0	r	**SPI Data Tracer, Readout of the last written data to a SFR Register by SPI** Reset: 00_H

SPI Checksum Register

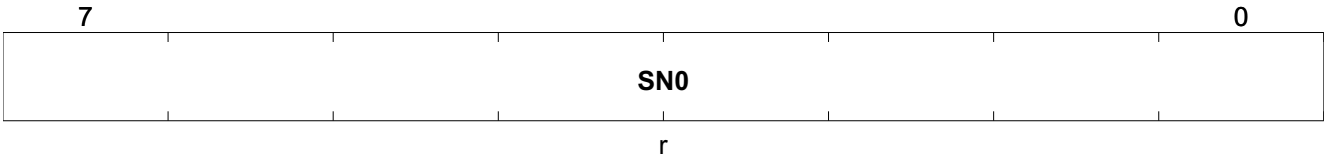
SPICHKSUM	Offset	Reset Value
SPI Checksum Register	**$0E1_H$**	**00_H**



Field	Bits	Type	Description
SPICHKSUM	7:0	rc	**SPI Checksum Readout** Reset: 00_H

Serial Number Register 0

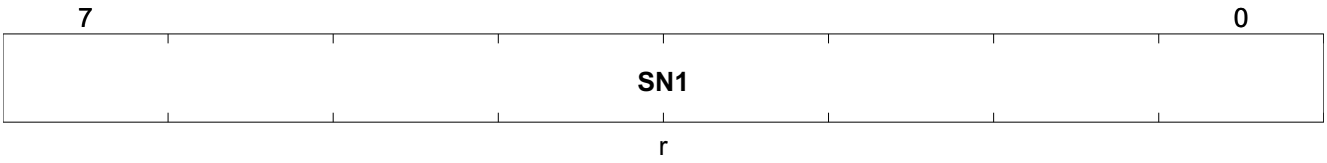
SN0	Offset	Reset Value
Serial Number Register 0	$0E2_H$	00_H



Field	Bits	Type	Description
SN0	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

Serial Number Register 1

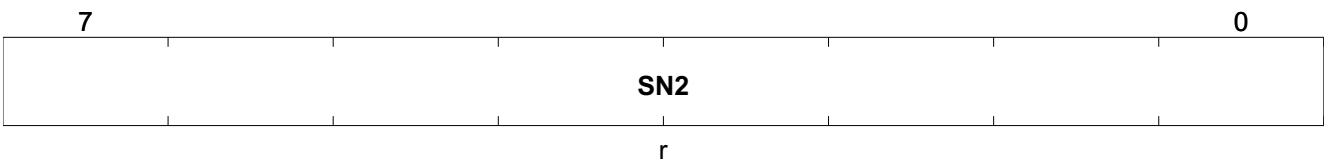
SN1	Offset	Reset Value
Serial Number Register 1	$0E3_H$	00_H



Field	Bits	Type	Description
SN1	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

Serial Number Register 2

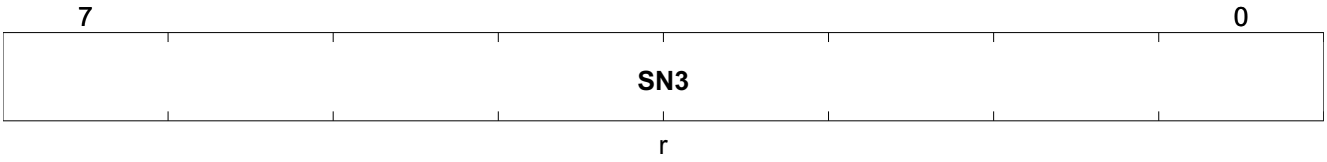
SN2	Offset	Reset Value
Serial Number Register 2	$0E4_H$	00_H



Field	Bits	Type	Description
SN2	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

Serial Number Register 3

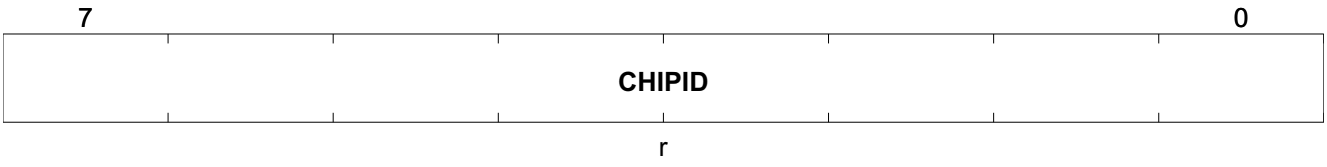
SN3	Offset	Reset Value
Serial Number Register 3	**$0E5_H$**	**00_H**



Field	Bits	Type	Description
SN3	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

Chip ID Register

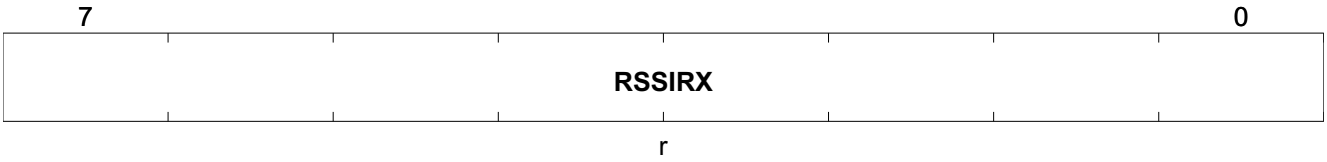
CHIPID	Offset	Reset Value
Chip ID Register	**$0E6_H$**	**00_H**



Field	Bits	Type	Description
CHIPID	7:0	r	**CHIP ID** Reset: 00_H

RSSI Readout Register

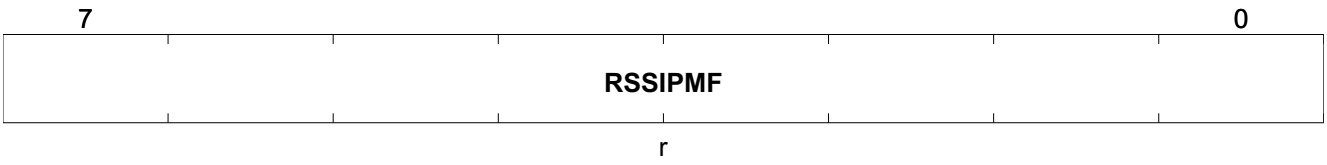
RSSIRX	Offset	Reset Value
RSSI Readout Register	**$0E7_H$**	**00_H**



Field	Bits	Type	Description
RSSIRX	7:0	r	**RSSI value after averaging over 4 samples** Reset: 00_H

RSSI Peak Memory Filter Readout Register

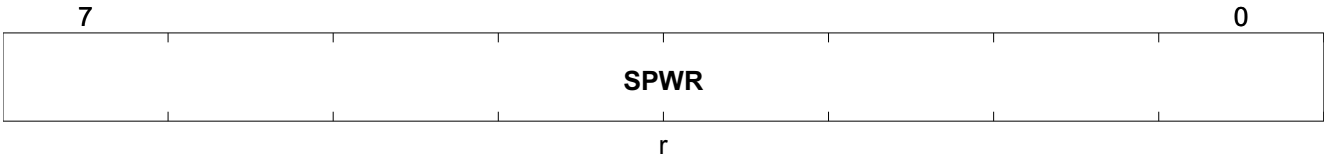
RSSIPMF	Offset	Reset Value
RSSI Peak Memory Filter Readout Register	**$0E8_H$**	**00_H**



Field	Bits	Type	Description
RSSIPMF	7:0	r	**RSSI Peak Memory Filter Level** Reset: 00_H

Signal Power Readout Register

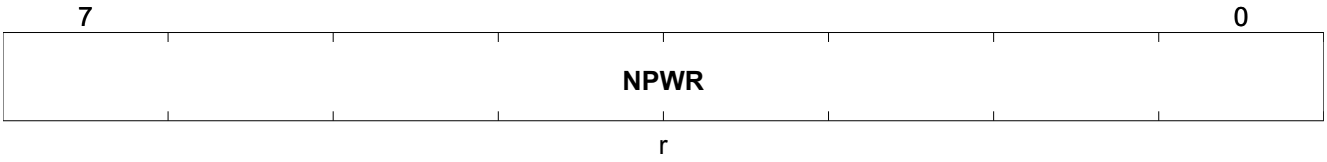
SPWR	Offset	Reset Value
Signal Power Readout Register	**$0E9_H$**	**00_H**



Field	Bits	Type	Description
SPWR	7:0	r	**Signal Power** The register contains the actual signal power which should be used to calculate the value of x_SIGDET0, x_SIGDET1 and x_SIGDETLO registers Reset: 00_H

Noise Power Readout Register

NPWR	Offset	Reset Value
Noise Power Readout Register	**$0EA_H$**	**00_H**



Field	Bits	Type	Description
NPWR	7:0	r	**FSK Noise Power** The register contains the actual noise power which should be used to calculate the value for the x_NDTHRES register Reset: 00_H

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