TC1796

32-Bit Single-Chip Microcontroller

Delta BC-to-BE Step

Microcontrollers

Never stop thinking

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Page	Subjects (major changes since last revision)
2	References to actual documents updated.

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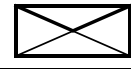

Table of Contents

1 Introduction

This document describes functional differences and improvements of the TC1796 BE-Step in comparison to the previous B-Steps, especially the BC-Step.

The referenced documents to this addendum are located at the Internet page:

- www.infineon.com/tc1796
- TC1796 System Units User's Manual (Vol.1), V2.0, July 2007
- TC1796 Peripheral Units User's Manual (Vol.2), V2.0, July 2007
- TC1796 Data Sheet V0.7, March 2006

1.1 Functional Improvements/DIfferences

This section summarizes the functional differences and improvements of the TC1796 BE-Step.

1.1.1 RTID Register

In the TC1796 BE-Step the reset value of register RTID = 0000 0300_H.

1.1.2 PCP

The erratum PCP_TC.029 "Possible corruption of CPPN value when a nested channel is restarted" has been fixed in the BE-Step.

1.1.3 Pads

This section summarizes all pad related changes and improvements.

- The ESD strength based on human body model of the BC-Step will be improved in the BE-Step. Detailed parameters are defined in the Data Sheet for the BE-Step.
- The erratum PWR_TC.P009 "Power up behavior" with the problem: "High cross current at OCDS L2 ports during power up" is fixed in the BE-Step. Therefore, also the constraints for the power up sequence as defined in the data sheet can be relaxed concerning the OCDS trace pins.
- Up to the BC-Step, the input pads with spike filter functionality $\overline{\text{PORST}}$, $\overline{\text{HDRST}}$, and $\overline{\text{NMI}}$ have no hysteresis. In the BE-Step these three input pads have a built-in hysteresis.
- The JTAG module clock input TCLK and the JTAG module reset/enable input $\overline{\text{TRST}}$ have a weak pull-down device active during reset ($\overline{\text{PORST}}$ = 0). Caused by this change, the pad test feature for pins TCLK and $\overline{\text{TRST}}$ (bits SCU_PTDAT2.TRST and SCU_PTDAT2.TCK) is no more supported. This means, the two bits 3 and 4 in register SCU_PTDAT2 are "rh" bits.
- In the BE-Step, the eight LVDS MSC Clock and Data output pads of the BE-Step are set into a high-impedance state if they are disabled by SCU_CON.LCDEN = 0.

- In the BE-Step, the driver strength of class A1 and A2 pads have been improved. This especially affects the test conditions for the output low voltage V_{OLA} and output high voltage V_{OHA}. The detailed test condition values for I_{OL} and I_{OH} are defined in the Data Sheet for the BE-Step.

1.1.4 SCU Control Register

In the TC1796 BE-Step it is possible that f_{OSC} remains connected to the PLL even if a PLL loss-of-lock failure is detected. This feature is controlled by the new bit OSCDISCDIS in the SCU_CON register. **Figure 1-1** shows the changes of the CGU of the BE-Step (in the red circle). The changes in registers SCU_CON and PLL_CLC are also documented on the next pages.

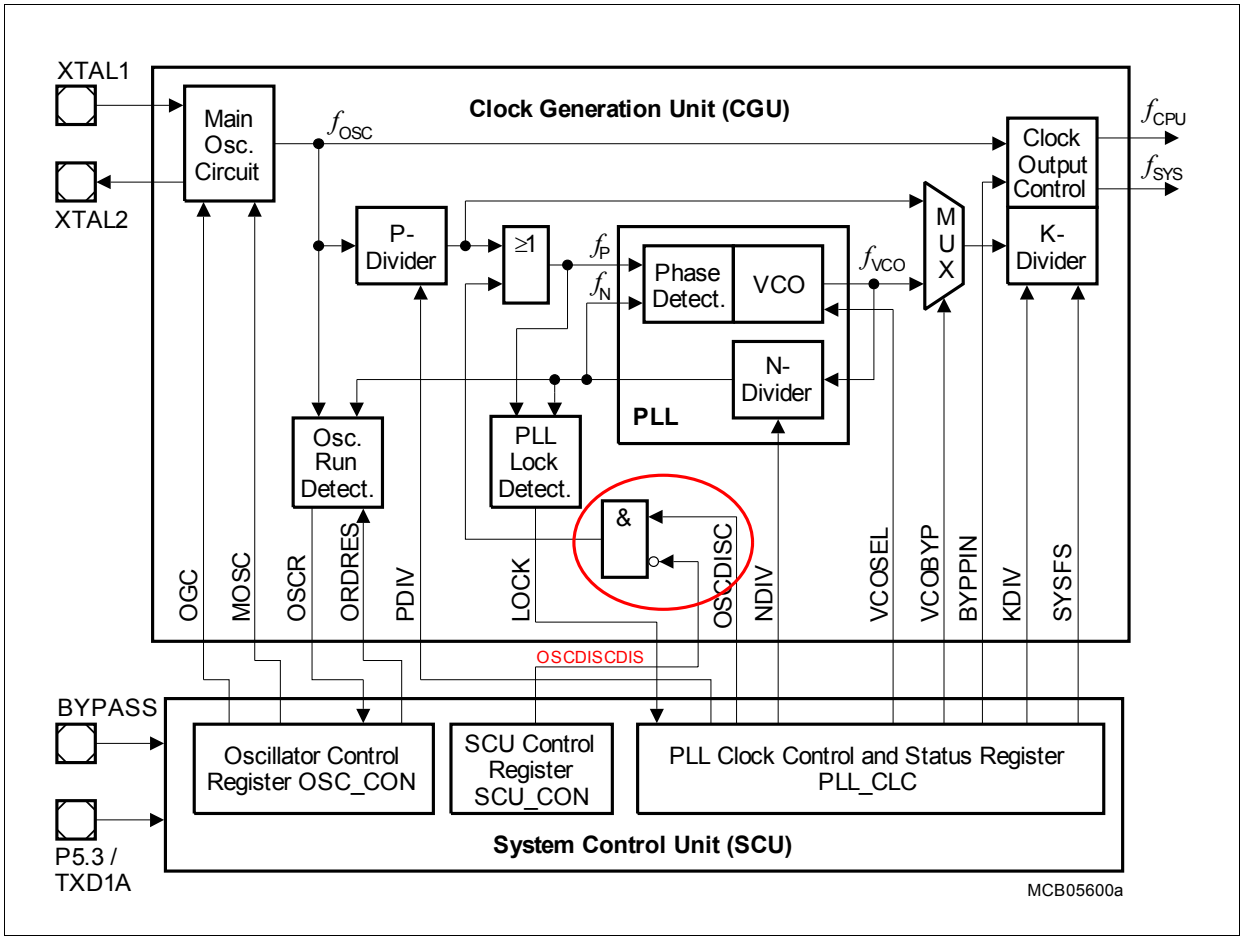

Figure 1-1 PLL Block Diagram

SCU_CON
SCU Control Register **($F0000050_H$)** **Reset Value: $FF00\ 0002_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ONE								ZERO			OSCDISCDIS	GIN1S		SSC0PDR	SLSPDR
rw								rw			rw	rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				RPARAV	LDEN	DTSON	0		AN7TM	NMIEN	EPUD	CSGEN	CSOEN	CSEEN	FIEN
r				rw	rw	rw	r		rw	rws	rw	rw	rw	rw	rw

Field	Bits	Type	Description
OSCDISCDIS	20	rw	**Oscillator Disconnect Disable** This bit is used to disable the control of PLL_CLC.OCSDISC in a PLL loss-of-lock case. 0 In case of a PLL loss-of-lock the oscillator clock f_{OSC} is controlled by bit PLL_CLC.OCSDISC (default after reset) 1 In case of a PLL loss-of-lock the oscillator clock f_{OSC} is always connected to the PLL even in a PLL loss-of-lock case.
ZERO	[23:21]	rw	**Spare 0 Control Bits**

PLL_CLC
PLL Clock Control Register (F0000040$_H$) Reset Values: see

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		BYP PIN	0				OSC DISC	0	NDIV						
r		rh	r				rwh	r	rw						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIV			0	KDIV				VCOSEL		VCO BYP	0		SYS FS	RES LD	LO CK
rw			r	rw				rw		rw	r		rw	rwh	rh

Field	Bits	Type	Description
OSCDISC	24	rwh	**Oscillator Disconnect** This bit is used to disconnect the divided f_{OSC} clock from the PLL in order to avoid unstable operation due to noise or sporadic clock pulses coming from the oscillator circuit while the PLL is still trying to lock to invalid clock pulses. The functionality of this bit can be disabled by setting SCU_CON.OSCDISCDIS to 1. 0 Oscillator clock f_{OSC} is connected to the PLL. 1 Oscillator clock f_{OSC} is disconnected from the PLL (default after reset) This bit is set by hardware if a PLL loss-of-lock failure is detected.

1.1.5 EBU

The erratum EBU_TC.019 “Burst Mode signals delayed longer than specified” has been fixed in the BE-Step.

1.1.6 ADC

The erratum ADC_TC.035 “AN7 test mode does not work” has been fixed in the BE-Step.

The erratum ADC_TC.039 “ADC reference voltage restrictions” has been fixed in the BE-Step.

The erratum ADC_TC.033 “Wrong CHCON register might be used by inserted conversion” has been fixed in the BE-Step.

1.1.7 FADC

The erratum FADC_TC.008 “VFAREF reliability issue” has been fixed in the BE-Step.

1.1.8 Single Scan Chain Mode (SSCM)

The SSCM is a test mode which is especially implemented in the BE-Step for analysis purposes. In SSCM, all device internal scan chains are concatenated to one single chain. This configuration allows to access the scan chains with a minimum number of external pins. This section describes the hardware requirements for a system that allows use of the SSCM for in-system diagnostics.

Entering Single Scan Chain Mode

The SSCM is entered if the following signals are applied during the rising edge of $\overline{\text{PORST}}$.

- $\overline{\text{NMI}}$ = 0
- TMS = 0
- BYPASS = 1
- $\overline{\text{TESTMODE}}$ = 0
- P10.[3:0] / HWCFG[3:0] = 0100_B

Note that the pins $\overline{\text{TESTMODE}}$, BYPASS, and $\overline{\text{NMI}}$ are forced to their non-default states. All the pins mentioned in the list above must be permanently driven when the SSCM is active.This must be regarded during board design.

Device State in Single Scan Chain Mode

When the TC1796 is in SSCM, the pins/modules are in the following states:

- P0 to P9 I/O pins: high impedance state
- EBU pins: high impedance state
- Trace pins: high impedance state
- LVDS pins: switched off
- Dedicated SSC pins: high impedance state
- $\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$: high impedance state
- TSTRES: high impedance input
- $\overline{\text{HDRST}}$: drives 0
- XTAL1: drive through mode, not used during SSCM
- Analog inputs AN[43:0]: not selected
- CPU & Peripheral modules: logic connected together in single scan chain

Pins used to control the SSCM

The following device pins of the TC1796 must be accessible during SSCM for in-system diagnostics.

- $\overline{\text{TRST}}$: JTAG reset input
- TDI: Scan chain enable
- TCK: Scan chain clock, used for shift and capture
- TMS: Scan chain input
- TDO: Scan chain output

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