Recommendations for Printed Circuit Board Assembly of Infineon TSLP/TSSLP/TSNP Packages

Additional Information

June 2010

Table of Contents

1 Package Description

Infineon's PG-TSLP/PG-TSSLP (Plastic Green Thin (Super) Small Leadless Package, **Figure 1**) and PG-TSNP (Plastic Green Thin Small Non-leaded Package, **Figure 2**) are green, small, leadless/non-leaded packages. They are preferred packages for space- and weight-limited applications such as cellular phones and digital cameras.

PG-TSLP/PG-TSSLP packages provide an Electroless Ni/Immersion Au (ENIG) finish. PG-TSNP packages provide an electroplated pure Sn finish.

Features

- Smallest xyz-package dimension for diodes/transistors
- Pb-free package
- Halogen-free package
- Environmentally friendly packing due to paper tape
- Flexible package platform with rapid tooling of new package sizes
- Flip-chip or wire-bond interconnection
- Possibility of multi-chip packages
- Possibility of cavity packages
- Better electrical performance for Radio Frequency (RF) applications
- Better thermal performance by comparison to standard discrete packages

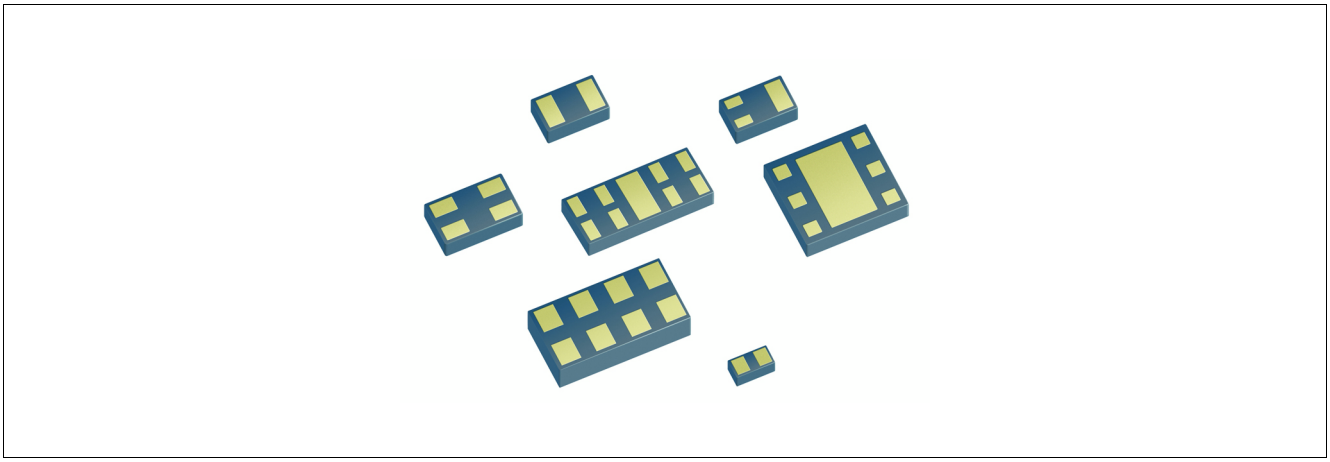

Figure 1 Some of IFX's TSLP/TSSLP Packages with Typical ENIG Plating

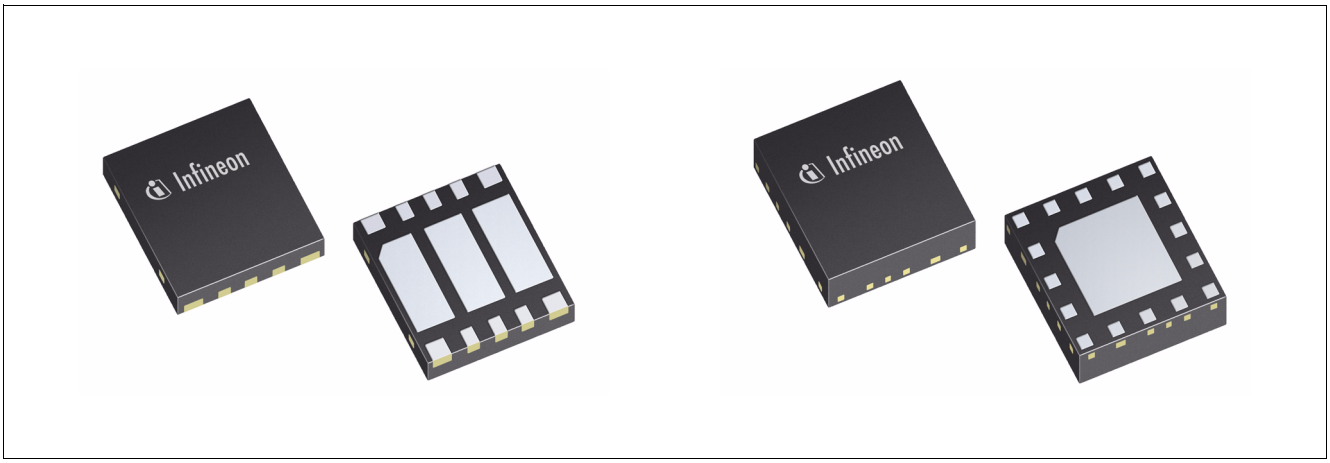

Figure 2 TSNP-11 and TSNP-16 Packages with Pure Sn Plating

2 Package Handling

2.1 ESD Protective Measurement

Semiconductor devices are normally Electrostatic Discharge Sensitive Devices (ESDSs) requiring specific precautionary measures regarding handling and processing. Discharging of electrostatically charged objects over an Integrated Circuit (IC) can be caused by human touch or by processing tools, resulting in high-current and/or high-voltage pulses that can damage or even destroy sensitive semiconductor structures. On the other hand, ICs may also be charged during processing. If discharging takes place too quickly (“hard” discharge), it may cause load pulses and damage, too. ESD protective measures must therefore prevent contact with charged parts as well as electrostatic charging of the ICs. Protective measures against ESD must be taken during handling, processing, and the packing of ESDS. A few hints are provided below on handling and processing.

2.1.1 ESD Protective Measures in the Workplace

- Standard marking of ESD-protected areas
- Access controls, with wrist strap and footwear testers
- Air conditioning
- Dissipative and grounded floor
- Dissipative and grounded working and storage areas
- Dissipative chairs
- Earth (“ground”) bonding points for wrist straps
- Trolleys or carts with dissipative surfaces and wheels
- Suitable shipping and storage containers
- No sources of electrostatic fields

2.1.2 Equipment for Personnel

- Dissipative/conductive footwear or heel straps
- Suitable smocks
- Wrist straps with safety resistors
- Gloves or finger cots that are ESD-tested (with specified volume resistivity)

Regular training of staff to avoid ESD failures using this equipment is recommended.

2.1.3 Production Installations and Processing Tools

- Machine and tool parts made of dissipative or metallic materials
- No materials having thin insulating layers for sliding tracks
- All parts reliably connected to ground potential
- No potential difference between individual machine and tool parts
- No sources of electrostatic fields

Detailed information on ESD protective measures may be obtained from the ESD Specialist through Area Sales Offices. Our recommendations are based on the internationally applicable standards IEC 61340-5-1 and ANSI/ESD S2020.

2.2 Packing of Components

Various packing types are available for feeding components in an automatic pick-and-place machine (tape-and-reel, trays,…) and surrounding bags and boxes to prevent damage during transportation or storage, depending on component and customer needs. Please refer to product and package specifications (**http://www.infineon.com/packages**) and our sales department to get information about what packing is available for a given product.

The following standards dealing with packing may be applicable for a given package and packing;
IFX packs according to the IEC 60286-* series:

IEC 60286-3	Packaging of components for automatic handling - Part 3: Packaging of Surface-Mount Devices (SMDs) or components on continuous tapes
IEC 60286-4	Packaging of components for automatic handling - Part 4: Stick magazines for dual-in-line packages
IEC 60286-5	Packaging of components for automatic handling - Part 5: Matrix trays

Moisture Sensitive SMDs are packed according to IPC/JEDEC J-STD-033*:
Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

Other references

ANSI/EIA-481-*	Standards Proposal No. 5048, Proposed Revision of ANSI/EIA-481-B 8 mm through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling (if approved, to be published as ANSI/EIA-481-C)
EIA-726	8 mm Punched & Embossed Carrier Taping of Surface Mount Components for Automatic Handling of Devices Generally Smaller than 2.0 mm x 1.2 mm
EIA-747	Adhesive Backed Punched Plastic Carrier Taping of Singulated Bare Die and Other Surface Mount Components for Automatic Handling of Devices Generally Less than 1.0 mm Thick
EIA/IS-763	Bare Die and Chip Scale Packages Taped in 8 mm & 12 mm Carrier Tape for Automatic Handling
EIA-783	Guideline Orientation Standard for Multi-Connection Package (Design Rules for Tape and Reel Orientation)

2.3 Moisture Sensitive Components / MSL Classification (Moisture Sensitivity Level)

For moisture-sensitive packages, it is necessary to control the moisture content of the components. Penetration of moisture into the package molding compound is generally caused by exposure to ambient air. In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. Thus it is necessary to dry moisture-sensitive components, seal them in a Moisture-Barrier Bag (MBB), and only remove them immediately prior to board assembly to the Printed Circuit Board (PCB). The permissible time (from opening the MBB until the final soldering process) during which a component can remain outside the MBB is a measure of the sensitivity of the component to ambient humidity (Moisture Sensitivity Level, MSL). The most commonly applied standard IPC/JEDEC J-STD-033* defines eight different MSLs (see **Table 1**). Please refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains information about the MSL of our products. IPC/JEDEC-J-STD-20 specifies the maximum reflow temperature that shall not be exceeded during board assembly at the customer’s facility.

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSL, or the humidity indicator card indicates too much moisture after opening an MBB, the components have to be baked prior to the assembly process. Please refer to IPC/JEDEC J-STD-033* for details. Baking a package too often can cause solderability problems due to oxidation and/or intermetallic growth. In addition, packing material (e.g. trays, tubes, reels, and tapes) may not withstand higher baking temperatures. Please refer to imprints/labels on the product packing to determine allowable maximum temperature.

Table 1 Moisture Sensitivity Levels (according to IPC/JEDEC J-STD-033*)

Level	Floor Life (out of MBB)	
	Time	**Conditions**
1	Unlimited	≤ 30°C / 85% RH[1)]
2	1 year	≤ 30°C / 60% RH[1)]
2a	4 weeks	≤ 30°C / 60% RH[1)]
3	168 hours	≤ 30°C / 60% RH[1)]
4	72 hours	≤ 30°C / 60% RH[1)]
5	48 hours	≤ 30°C / 60% RH[1)]
5a	24 hours	≤ 30°C / 60% RH[1)]
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C / 60% RH[1)]

1) RH = Relative Humidity

2.4 Storage and Transportation Conditions

Improper transportation and unsuitable storage of components can lead to a number of problems during subsequent processing, such as poor solderability, delamination, and package-cracking effects.

These standards should be taken into account:

IEC 60721-3-0 Classification of environmental conditions: Part 3:
Classification of groups of environmental parameters and their severities; introduction

IEC 60721-3-1 Classification of environmental conditions: Part 3:
Classification of groups of environmental parameters and their severities; Section 1: Storage

IEC 60721-3-2 Classification of environmental conditions: Part 3:
Classification of groups of environmental parameters and their severities; Section 2: Transportation

IEC 61760-2 Surface mounting technology - Part 2:
Transportation and storage conditions of surface mounting devices (SMD) - Application guide

IEC 62258-3 Semiconductor Die Products - Part 3:
Recommendations for good practise in handling, packing and storage

ISO 14644-1 Clean rooms and associated controlled environments Part 1:
Classification of airborne particulates

Table 2 Overview over General Storage Conditions

Product	Condition for Storing
Wafer/Die	N2 or MBB (IEC 62258-3)
Component - moisture sensitive	MBB[1)] (JEDEC J-STD-033*)
Component - not moisture sensitive	1K2 (IEC 60721-3-1)

1) MBB = Moisture Barrier Bag

Maximum storage time:

The conditions to be complied with in order to ensure problem-free processing of active and passive components are described in standard IEC 61760-2.

Internet links to standards institutes:

American National Standards Institute (ANSI) (http://webstore.ansi.org/)

Electronics Industries Alliance (EIA) (http://www.eia.org)

Association Connecting Electronics Industries (IPC) (http://www.ipc.org/)

2.5 Handling Damage and Contaminations

Automatic or manual handling of components in or out of the component packing may cause mechanical damage to package balls and/or body.

Any contamination applied to component or packing may cause or induce processes that (together with other factors) may lead to a damaged device. The most critical issues are:

- Solderability problems
- Corrosion
- Electrical shorts (due conductive particles)

2.6 Component Solderability

The sufficiently thick and wettable metal surfaces (final plating) or solder depots/balls of most semiconductor packages assure good solderability, even after a long storage time. **Note that the cut edges of the pins should be ignored in any assessment of solderability.** Suitable methods for the assessment of solderability can be derived from JESD22B 102 or IEC60068-2-58.

Both PG-TSLP/TSSLP components with ENIG plating and PG-TSNP components with Sn plating are compatible with Pb-containing and Pb-free soldering.

3 Printed Circuit Board (PCB)

3.1 General Remarks

A PCB's design and construction are key factors for achieving a high reliability of the solder joints. Some areas and mounting positions on a board are more critical regarding reliability (for example, the region around or at the opposite PCB side of RF frames, connectors and packages). If possible, try to avoid mounting bigger packages in these areas; it's better to mount small devices there such as TSLP/TSSLP/TSNP packages. Large packages increase the PCB stiffness and this may lead to a lower reliability compared to standardized board-level reliability tests.

3.2 PCB Pad Design

The solder pads have to be designed to assure optimum manufacturability and reliability. Two basic types of solder pads are commonly used:

- "Solder mask defined" (SMD) pad: The copper pad is larger than the solder mask opening above this pad. Thus the land area is defined by the opening in the solder mask.

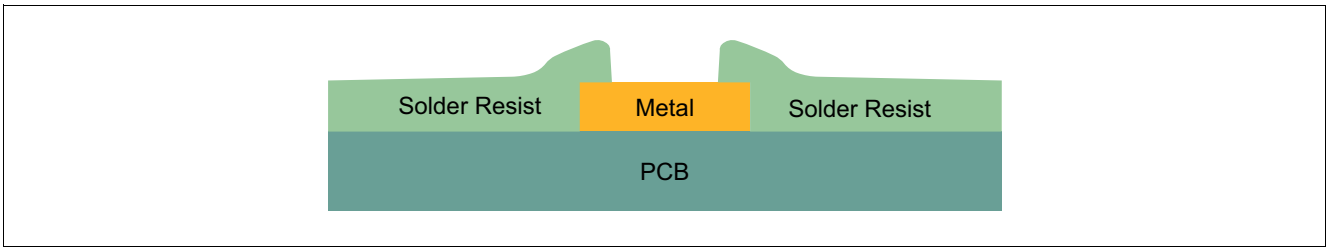

Figure 3 SMD Pad

- "Non-Solder-Mask Defined" (NSMD) pad: Around each copper pad there is solder-mask clearance. It is necessary to specify the dimensions and tolerances of the solder-mask clearance so that no overlapping of the solder pad by solder mask occurs (depending on PCB manufacturers' tolerances, 75 µm is a widely used value). For Because NSMD pads provide more space for routing and result in a higher solder joint reliability, NSMD type is recommended for the solder pads on the PCB. In addition, the side walls of the lands are wetted by the solder, which results in less stress concentration.

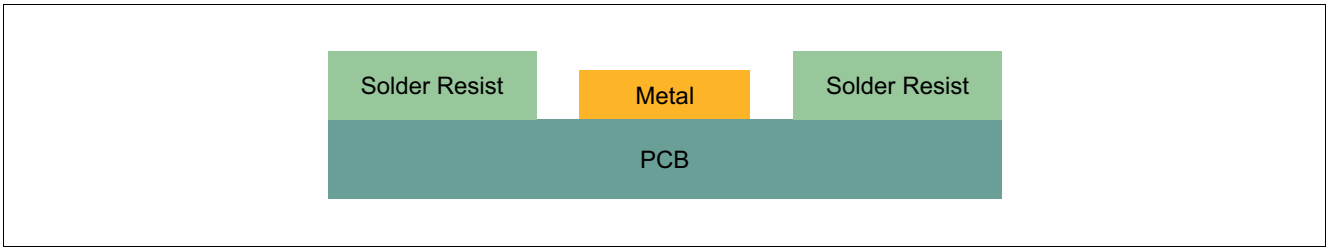

Figure 4 NSMD Pad

For small TSLP/TSSLP/TSNP packages and small pitches, another option of NSMD pads can be used. The solder mask opening can be larger than the outline of the package. This helps to prevent the tilting of devices when the solder mask is thicker than the height of the copper pad plus the solder joint.

Using both SMD and NSMD pads for one component is not recommended. Heavy misalignment between solder mask and board pads can lead to unbalanced wettable surfaces and solder joints.

The copper pad (NSMD) and solder-mask openings (SMD) dimensions that have been determined by Infineon to be the best solutions for each type of package are published in the package data base on Infineon's homepage:

http://www.infineon.com/cms/en/product/technology/packages/

After choosing a certain package family (TSLP/TSSLP/TSNP) and a specific TSLP/TSSLP/TSNP-package, board and stencil recommendations are available (please refer to the "downloads" listed under each package).

In general to avoid tilted devices, bigger pads of the package are divided up in smaller pads on the PCB. If possible, small pads are slightly expanded to have better printability.

To improve thermal and RF performance, the PCB design may include vias. The vias serve to conduct the heat and/or RF-signals into deeper layers of the board. Depending on the package size, various numbers of vias are possible. Especially for small packages, the vias should not be placed under the device. If this is not possible, the vias should be covered by solder resist or should be plugged to avoid filling them with solder, which may cause voiding and a smaller stand-off.

Microvias can also improve thermal and RF performance. They can be placed inside the solder pads and therefore are a preferred solution. Be aware that their flatness has to be sufficient, because deep dips inside the pads may cause solder joint voiding.

In TSLP/TSNPs with exposed pads, we recommend only using NSMD pads in combination with microvias 0.1 mm in diameter, or SMD pads in combination with vias 0.2 mm in diameter. Recommendations for via locations can be found in the component specific board pad layout.

If it is intended to use the TSNP as a drop-in-solution for TSLP in the same product (e.g. TSNP-16-1 as a substitute for TSLP-16-1), typically they can be used on the same product PCB. The board layout does not have to be changed. In some cases it might be necessary to change the stencil layout to adapt it to the needs of both packages.

3.3 Pad Surfaces

The solder pads have to be easy for the solder paste to wet. In general, all finishes are well-proven for SMT assembly, but the quality of the plating/finish is more important for fine-pitch applications in particular. Because of the uneven surface of Hot Air Solder Leveling (HASL) finish, Pb-free or Pb-containing HASL is less preferred for assembly (especially for pitches < 0.65 mm) compared to completely “flat” platings such as Cu-OSP (OSP: Organic Solderability Preservative) or electroless Sn or NiAu.

From a package point of view, it is difficult to recommend a certain PCB pad finish that will always meet all requirements. The choice of finish also depends strongly on board design, pad geometry, all components on the board, and process conditions, and must be chosen depending on the specific needs of the customer.

Infineon’s internal tests have shown that electroless Sn and Cu-OSP are suitable and reliable platings.

Table 3 Typical PCB Pad Finishes

Finish	Typ. Layer Thickness [µm]	Properties	Concerns
HASL (SnAg) *(Hot Air Leveling)*	> 5	low cost, widely used, know-how in fabrication	uneven surface, formation of humps, flatness of single pads has to be good for fine pitch applications
Electroless Sn	0.3 - 1.2	solder joint consists only of copper and solder, no further metal is added to the solder joint	long-term stability of protection may be a concern, baking of PCB may be critical
Electroless Ag	0.2 - 0.5	solder joint consists only of copper and solder, no further metal is added to the solder joint	long-term stability of protection may be a concern, baking of PCB may be critical
Electroless Ni / Immersion Au *(ENIG)*	3 - 7 / 0.05 - 0.15	good solderability protection, high shear force values	expensive, concerns about brittle solder joints
Galvanic Ni/Au	> 3 / 0.1 - 2	only for thicker layers, typically used for connectors	expensive, not recommended for solder pads
OSP *(Organic Solderability Preservatives)*	1	low cost, simple, fast and automated fabrication	must be handled carefully to avoid damaging the OSP; long-term stability not as good as other coatings; in case of double-sided assembly only suitable with inert gas during reflow

4 PCB Assembly

4.1 Solder Stencil

The solder paste is applied onto the PCB metal pads by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB. For TSLP/TSNP packages, stencils 80-120 µm thick are recommended. For TSSLP and some TSLP and TSNP packages that have small pads, stencils 100 µm thick or less should be used. Please consider the area-ratio which describes feasible stencil thicknesses in relation to the aperture sizes used.

The sizes and shapes of the tested apertures are published in the package database on Infineon's homepage:

http://www.infineon.com/cms/en/product/technology/packages/

After choosing a certain package family (TSLP/TSSLP/TSNP) and a specific TSLP/TSSLP/TSNP-package, board and stencil recommendations are available (please refer to the "downloads" listed under each package).

To ensure uniform and high solder paste transfer to the PCB, laser-cut (mostly made from stainless steel) or electroformed stencils (nickel) are preferred. Generally rounded corners of the apertures (radius ~ 50 µm) can be supportive for the paste release.

Please note that the given aperture sizes are typically tested for stencils 100 µm thick. Other stencil thicknesses, the described "drop-in-solution" in **Chapter 3.2**, or customer-specific processes/materials could make it necessary to marginally adjust the given layouts.

4.2 Solder Paste

Solder paste consists of solder alloy and a flux system. Normally the volume is split into about 50% alloy and 50% flux. In terms of mass, this means approx. 90 wt% alloy and 10 wt% flux system. The flux system's function is to remove the contamination from the solder joints during the soldering process. The capability of removing contamination is given by the respective activation level. The solder paste metal alloy has to be of Pb-containing eutectic or near-eutectic composition (SnPb or SnPbAg) or Pb-free composition (SnAgCu whereas Ag 3-4%, Cu 0.5-1%). A "no-clean" solder paste is preferred, because cleaning under the soldered TSLP/TSSLP/TSNP may be difficult. The paste must be suitable for printing the solder stencil aperture dimensions; Type 3 paste should be sufficient. Solder paste is sensitive to age, temperature and humidity. Please comply with the handling recommendations of the paste manufacturer.

4.3 Component Placement

TSLP/TSSLP/TSNP packages have to be placed accurately according to their geometry. Positioning the packages by hand is not recommended.

Component placement accuracies of ±50 µm are obtained with modern automatic component-placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or additionally on individual mounting positions (local fiducials). They are detected by a vision system immediately before the mounting process. Recognition of the packages is performed by a special vision system, enabling correct centering of the complete package.

The maximum tolerable misplacement of the components is 35% of the metal pad width on the PCB. Consequently, for example for the P-TSLP-3-1, the device-pad-to-PCB-pad misalignment has to be less than 70 µm to assure a robust mounting process.

Also higher misplacement can result in well-soldered devices, but may result in a higher defect rate. In this case, the self-centering effect during reflow can align the package to the board pads. Only the customer can decide after consideration of his/her special processes and materials whether the self-centering effect can be used to tolerate a higher misplacement rate.

The following remarks are important:

- Especially on large boards, local fiducials close to the device can compensate PCB tolerances.
- Due to the fact that the outer dimensions of TSLP/TSSLP/TSNP packages are very accurate (±50 µm) an alignment according to the outline is no problem. Of course it is also possible to use the lead (component pad) recognition capabilities of the placement system.
- To ensure the identification of the packages by the vision system, adequate lighting as well as the correct choice of the measuring modes are necessary.
- Too much placement force can squeeze out solder paste and causes solder joint shorts or beading. On the other hand, not enough placement force can cause insufficient contact between package and solder paste, which can result in open solder joints or badly centered packages.

4.4 Soldering

Soldering determines the yield and quality of assembly fabrication to a very large extent. Generally all standard reflow soldering processes, including

- vapor phase
- forced convection
- infrared (with restrictions)

and typical temperature profiles are suitable for board assembly of the TSLP/TSSLP/TSNP. Wave soldering is not possible. In the reflow process, each solder joint has to be exposed to temperatures above solder liquidus (temperature at which the solder is fully molten) for a sufficient time to get the optimum solder-joint quality, whereas overheating the PCB with its components has to be avoided. Please refer to the bar-code label on the packing for the peak package-body temperature. When using infrared ovens without convection, special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB, especially on large, complex boards with different thermal masses of the components, including those under the TSLP/TSSLP/TSNP. The most highly recommended process is forced convection reflow. Nitrogen atmosphere can generally improve solder-joint quality, but is normally not necessary for soldering SnPb metal alloys.

The temperature profile of a reflow process is one of the most important factors of the soldering process. The temporal progression of the temperature profile is divided into several phases, each with a special function. **Figure 5** shows a general forced-convection reflow profile for soldering TSLP/TSSLP/TSNP packages. **Table 4** shows an example of the key data of such a solder profile for Pb-containing and for Pb-free alloys. The single parameters are influenced by various facts, not only by the package. It is essential to follow the solder-paste manufacturers' application notes, too. Additionally, most PCBs contain more than one package type and therefore the reflow profile has to be matched to the requirements of all components and materials. We recommend measuring the solder joints' temperatures by thermocouples under the respective packages. It has to be considered that components with large thermal masses don't heat up at the same speed as lightweight components, and the position and the surrounding of the package on the PCB, as well as the PCB thickness, can influence the solder-joint temperature significantly. Therefore no concrete temperature profile can be given.

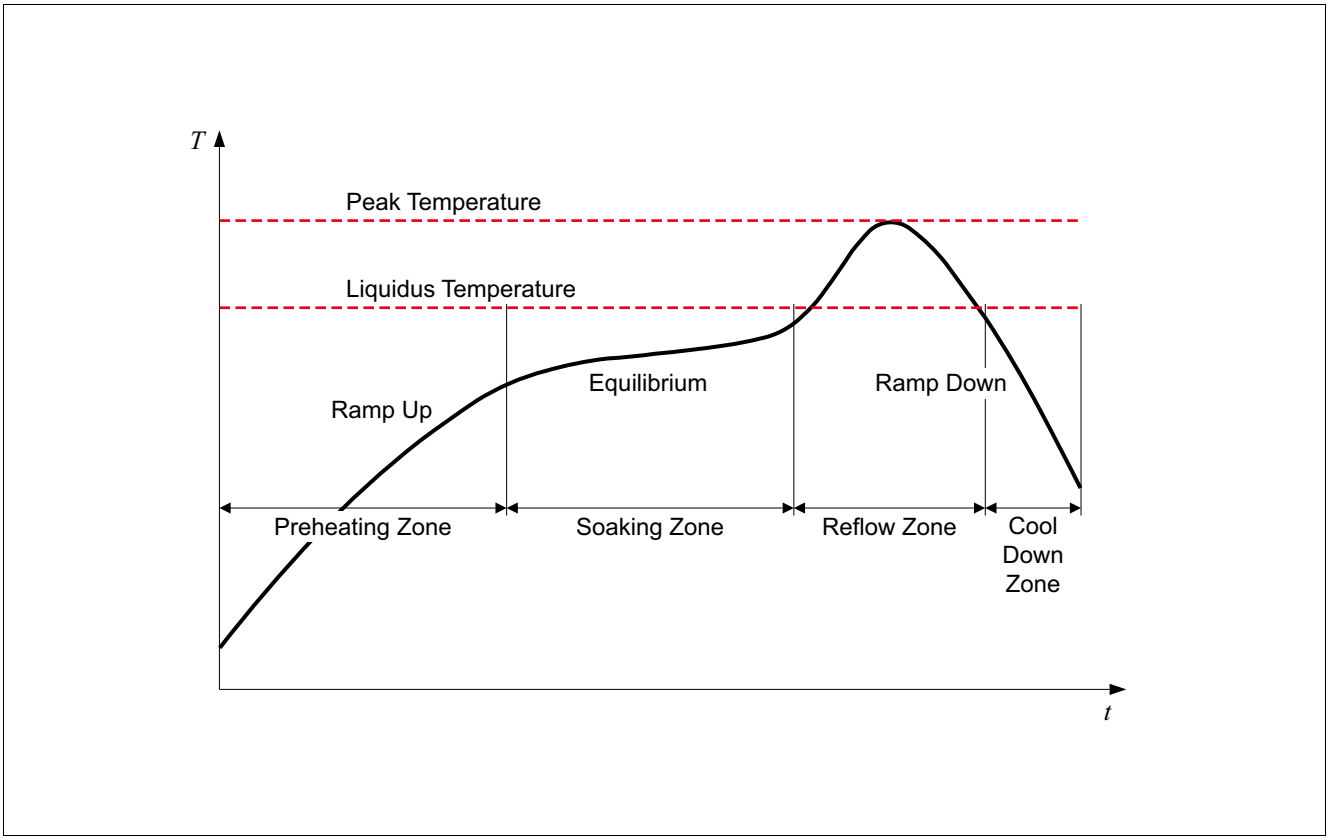

Figure 5 General Forced Convection Reflow Solder Profile

Table 4 Example for the Key Data of a Forced Convection Reflow Solder Profile

Parameter	Pb-containing Alloy (SnPb or SnPbAg)	Pb-free Alloy (SnAgCu)	Main Requirements From
Preheating rate	2.5 K/s	2.5 K/s	Flux system (Solder paste)
Soaking temperature	140 - 170°C	140 - 170°C	Flux system (Solder paste)
Soaking time	80 s	80 s	Flux system (Solder paste)
Peak temperature	225°C	245°C	Alloy (Solder paste)
Reflow time over liquidus	60 s	60 s	Alloy (Solder paste)
Cool down rate	2.5 K/s	2.5 K/s	

4.5 Double-Sided Assembly

TSLP/TSSLP/TSNP packages are generally suitable for mounting on double-sided PCBs. That means that in a first step, one side of the PCB is fitted with components and soldered. Afterwards the second side of the PCB is fitted with components and soldered again.

5 Cleaning

After the reflow soldering process, some flux residues can be found around the solder joints. If a “no-clean” solder paste has been used for solder paste printing, the flux residues usually don’t have to be removed after the soldering process. Be aware that cleaning under a TSLP/TSSLP/TSNP package is difficult because of the small gap between the package and the PCB, and is therefore not recommended. Whether or not the solder joints have to be cleaned, however, the cleaning method (e.g. ultrasonic, spray or vapor cleaning) and solution have to be selected by considering the packages to be cleaned, the flux used in the solder paste (rosin-based, water-soluble, etc.), and the environmental and safety aspects. Removing or drying of even small residues of the cleaning solution should also be done very thoroughly. Contact the solder-paste manufacturer for recommended cleaning solutions.

6 Inspection

A visual inspection of the solder joints with conventional AOI (Automatic Optical Inspection) systems is limited to the outer surface of the solder joints. In most cases, these are visible and can be judged by looking at them from the side (not from the top like most of the AOI systems). However, optical inspections are not usually very successful. Only big misplacement errors and wrong polarity can be checked.

Even in case of TSNPs with fully exposed copper at the package edges, the success of an AOI will be limited, because the exposed copper (resulting in the TSNP singulation process) is not necessarily wetted by the solder during reflow.

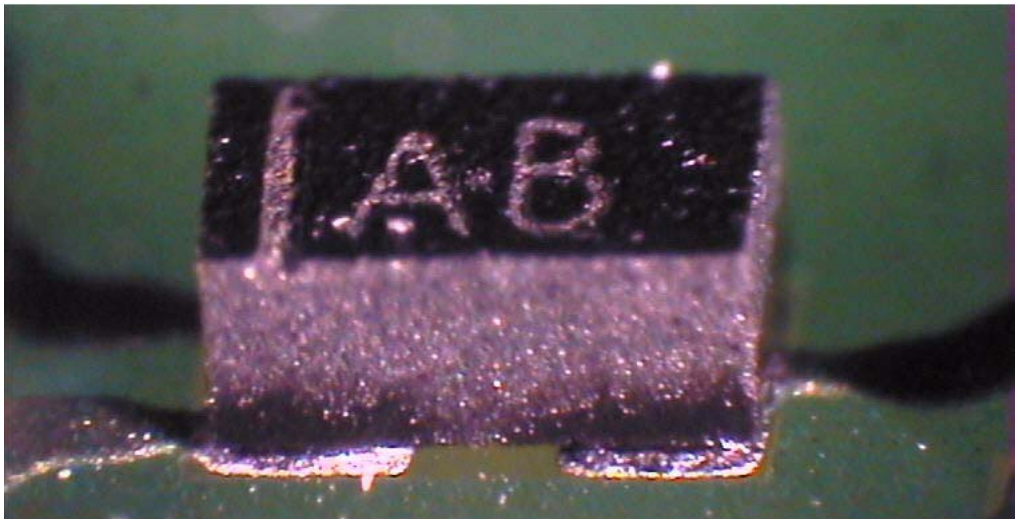

Figure 6 Typical Side View of TSLP Solder Joints

The only reasonable method for efficient inline control is the implementation of AXI (Automatic X-ray Inspection) systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspecting, controlling, analysing, and data transfer routines. These systems quite reliably enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray. For the acceptability of electronic assemblies, please refer also to the IPC-A-610D standard.

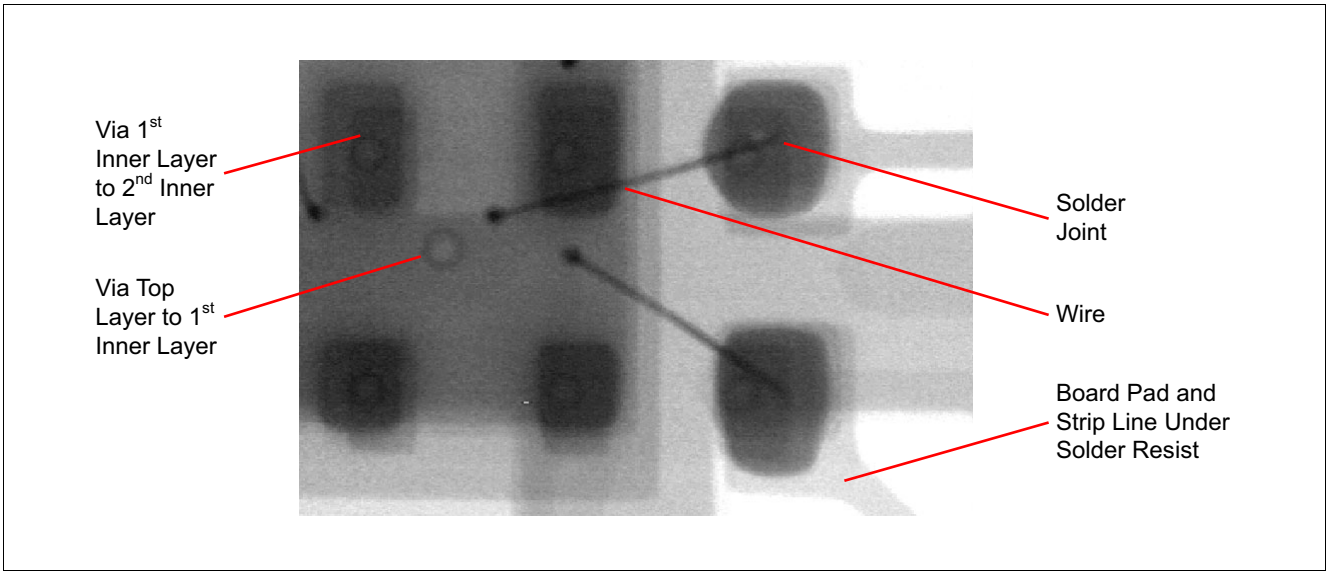

Figure 7 Typical X-ray Image of a Soldered TSLP.
Visible are solder joints, wires (dark structures), board pads (under solder resist) and trip lines (light structures). The round structures are vias (from the top to the first inner layer or from the first inner layer to the second inner layer).

Cross sectioning of a soldered package as well as dye penetrant analysis can serve as tools for sample monitoring only, due to their destructive character. However, they help to get an idea about the quality of the solder joint, intermetallic compounds, and voids.

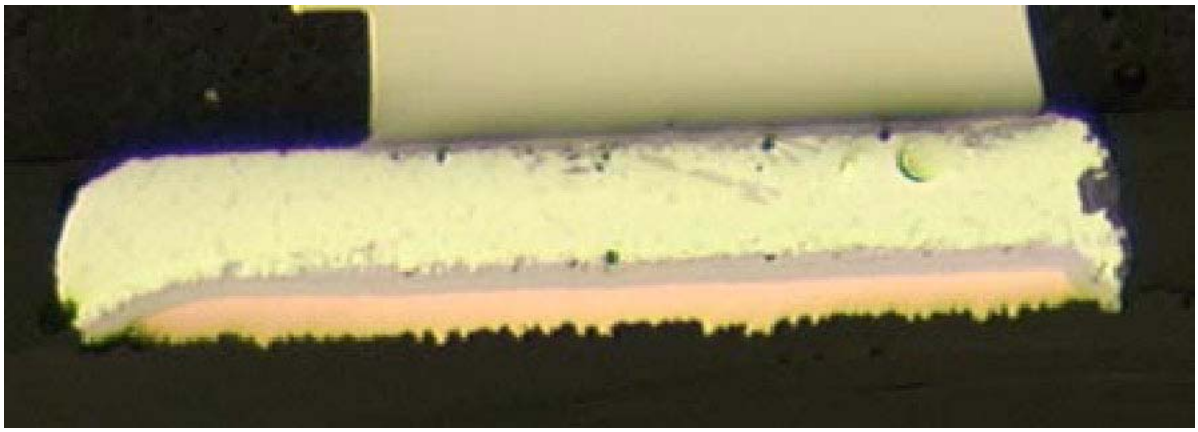

Figure 8 Cross Section of a TSLP Solder Joint (Pb-free)

Pb-free solder joints look different from SnPb solder joints. SnPb joints have a bright and shiny surface; a dull surface is an indicator of an insufficient solder joint. Pb-free solder joints don't have this bright surface. Pb-free solder joints are dull and grainy. These surface properties are caused by the irregular solidification of the solder, as the solder alloys used are not exactly eutectic (like the 63Sn37Pb solder alloy). This means that SnAgCu-solders don't have a melting point but a melting range of some degrees. Although Pb-free solder joints have this dull surface, this does not mean that Pb-free joints are of lower quality or weaker than the SnPb joints. This characteristic makes it necessary to teach the inspection personnel what these new Pb-free joints look like, and/or to adjust optical inspection systems to handle Pb-free solder joints properly.

7 Rework

If a defective component is detected after board assembly, the device can be removed and replaced by a new one. Due to possible damage while removing the component, a desoldered component should not be reused. Nevertheless, desoldering the old component (if analysis afterwards is planned) and resoldering of the new component has to be done very thoroughly. Repair of single solder joints is not possible.

7.1 Tooling

The rework process is commonly done on special rework equipment. There are a lot of systems available on the market, and for processing these packages, the equipment should fulfill the following requirements:

- *Heating*: Hot air heat transfer to the package and PCB is strongly recommended. Temperature and air flow for heating the device should be controlled. With freely programmable temperature profiles (e.g. by PC controller), it is possible to adapt the profiles to different package sizes and thermal masses. PCB preheating from the underside is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but infrared heating should be used only for augmenting the hot air flow from the upside. Nitrogen can be used instead of air.
- *Vision system*: The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of package to PCB, a split optic should be used. Microscope magnification and resolution should be appropriate for the pitch of the device.
- *Moving and additional tools*: The device should be relocatable on the whole PCB area. Placement accuracy better than ±50 µm is recommended. The system should have the capability of removing solder residues from PCB pads (special vacuum tools).

7.2 Device Removal

If a defective component is going to be sent back to the supplier, no further defects must be introduced to the device during its removal from the PCB, because this may hinder the supplier's failure analysis. The following recommendations should be followed:

- *Moisture*: Depending on its MSL, the package may have to be dried before removal. If the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly, the PCB has to be dried according to the recommendations (**Chapter 2.3**); otherwise too much moisture may have been accumulated and damage may occur (popcorn effect).
- *Temperature profile*: During the soldering process, it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (**Chapter 4.4**).
- *Mechanics*: Be careful not to apply high mechanical forces for removal. Otherwise, failure analysis of the package can be impossible, and/or the PCB can be damaged. For large packages, pipettes (vacuum nozzles) can be used. Pipettes are implemented on most rework systems.

7.3 Site Redressing

Standard process: After removing the defective component, the pads on the PCB have to be cleaned to remove solder residues. Before placing a new component, solder paste should be applied to each PCB pad by printing (special micro stencil) or dispensing. Only no-clean solder paste should be used.

Special process: For low pin count (<10), small TSLP/TSSLP packages, the following procedure can be used. After removing the defective component, the remaining solder on the pads can checked for coplanarity and contamination. If the solder residues are uniform and clean, some flux can be applied by dispensing or with a brush. Only no-clean solder flux should be used. Generally the resulting solder joint is lower in quality, and its quality has to be assessed according to the customer's reliability requirements.

7.4 Reassembly and Reflow

After preparing the site, the package can be placed onto the PCB. The maximum applied pick&place force should not exceed the force applied during standard board assembly.

It is also possible to position the package exactly above the PCB pads, at a height just above the pads so that there is no contact between the package and the PCB. The package is then dropped into the printed or dispensed solder paste depot (zero-force placement).

During the soldering process, it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (**Chapter 4.4**). Investigation has shown that if distance, time, and airflow are properly controlled, an air temperature of 300°C can be used, for example, without violating the maximum allowed reflow profile.

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