Wireless Control and Tire Pressure Monitoring ICs

RF Design Verification Guidelines

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Revision History	
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1 Introduction

This document gives guidelines for RF Design Review and Verification of designs based on Infineon's Wireless Control and TPMS integrated circuits. It covers all application segments such as automotive, industrial and consumer electronics and provides best-practice aspects and checklists for exhaustive system verification in the customer application. Even if some of the hints may sound like common sense or just a good engineering practice, they are still included as reminder.

This document has applications of Infineon Wireless Control and TPMS Wireless IC products in its focus: receivers (RX), transmitters (TX) and transceivers (TRX) – some of them with integrated temperature, acceleration and pressure sensors and microcontrollers – however, current guideline version is narrowed to general and RF aspects – sensor and μC aspects will follow later.

This document can help you in following design phases:

- Verification plan definition
- Schematics design and review
- PCB layout design and review
- Firmware/Software/Hardware co-verification and Design-For-Test (DfT)
- System verification, validation and sign-off
- Design issue/problem detection, localization, debugging and fixing
- Definition of production test

First chapter concentrates on general RF design issues, then RX, TX and TRX applications are addressed respectively.

Disclaimer & Limitations: this document is provided on an "as-is/best-effort" basis and contains detailed, but still generic and design-independent guidelines, thus it can only extend and by no means replace an obligatory design-specific customer-defined verification plan. Thus there is no liability of Infineon resulting from following this guidelines whatsoever.

This guideline does not include any lifetime or environmental test recommendations nor detailed references to regulations - it is the sole responsibility of the system designer and consequently manufacturer to satisfy its customer's requirements and all relevant/applicable standards and regulations.

2 Common Aspects for RX, TX or TRX

- For ICs providing unique serial number (SN), include the SN in the measurement protocols to ensure traceability.

2.1 Power Supply

Clean and stable power supply is essential for good RF applications. Following characteristics must be specified, designed and verified in the application over the full specified range of environmental and operating conditions incl. margins:

- Supply voltage: check all supply & regulated voltages in all functional modes (variation vs. temperature and application supply voltage). Supply voltage must remain within the specified (min-max) range for all devices under all circumstances. Lower operating voltage than "min" may cause performance loss (blocking, linearity, phase noise, output power) or even overall malfunction (due to analog operating point or logic threshold shift). Higher operating voltage than "max" may cause an overall malfunction (due to analog operating point or logic threshold shift), electrical breakdown or product lifetime impact due to higher currents (electromigration), higher dissipation (thermal stress) or overvoltage stress (V_T drift over lifetime) – the list of effects being not exhaustive.
- Supply voltage stability: consider and check load and line regulation of all regulators (external and internal). Do not load on-chip regulators with external loads, except explicitly allowed.
- Regulator stability: take care about capacitive (decoupling caps!) and inductive (wiring!) loads when designing supply circuitry. Use only recommended capacitor values and types (=ESR) for regulator

decoupling and place capacitors as close as possible to input/output pins. Violation of these rules may cause regulator instability (=oscillations with arbitrary load-dependent amplitude and frequency) causing in turn probably sensitivity loss and blocking performance loss (LO spurious mixing) for RX circuits and unwanted TX spurious emissions.

- Supply RF and noise decoupling: DC power supply must be ripple-free. Take care and verify that **no external RF and noise sources** (EMC) can penetrate into the DC supply network i.e. use feed-through capacitors and ferrite beads. Specifically for TX circuits generating on-board RF currents, voltages and fields make sure there is no "backscatter" from RF output matching or antenna circuits to supply distribution network. Design for low-ohmic and wideband-low-impedance supply network and test that. To achieve wideband low-impedance behavior use different capacitor values in parallel (high-C || low-L= 100nF || 1 nF || 100 pF). All circuitry generating large current surges (CMOS digital, line drivers) must be locally decoupled to reduce switching noise on supply. Avoid switching regulators – if required in the application, try to implement types with constant switching frequency or apply linear regulators at the output. In that case check explicitly in the application behavior of RX and TX at RF + around the designed switching frequency **and** its harmonics.
- Supply and GND distribution and layout: supply and ground lines must be low-ohmic and have low-impedance (low L), i.e. corresponding PCB track width. Use large ground planes and - if possible – inner layers. Avoid ground loops, i.e. contamination of sensitive (input) ground nodes with shared return path for high-current (RF or switching) outputs. Use star topology (common ground) for ground and supply line connection. Use split ground (digital + analog + RF) topology in general. Provide galvanic isolation where feasible. Avoid using **PCB vias** in supply and ground distribution – if you must have them, use several multiple vias in parallel to reduce the parasitic R an L.
- Supply crosstalk: Take care that any wire or PCB trace approaching $\lambda/4$ length, independently of its original "purpose" (i.e. even GND or supply), starts to behave like antenna and either emit or receive the RF signal over large distances with high efficiency. Also pure capacitive or inductive crosstalk may contaminate either supply, if routed in parallel with large signal tracks, or sensitive input (RX antenna) or reference (XOSC) signals may become contaminated from a noisy supply line.
- Supply switches: in some applications, it is required to cut-off the supply lines to subcircuits using discrete supply switches (transistors). Take care to design for low-ohmic and low-impedance solution (R_{dson}) over all supply, temperature and load conditions and verify that.

2.2 Crystal Oscillator

Crystal oscillators (XOSC) are used in considered applications as:

a) RF reference sources for RX (for local oscillator) and TX (for modulator) PLLs and
b) clock sources for digital circuits

It is thus essential for a XOSC to provide:

a) fast startup behavior
b) clean signal: no spurious=discrete single-line spectrum & low phase noise
c) frequency accuracy and stability

As every oscillator, it consists of resonator circuitry and an on-chip amplifier for energy loss compensation to fulfill and sustain the oscillation criteria. However, the resonator circuitry includes not only the quartz crystal itself, but also possible external and on-chip pulling (tuning) capacitors and unavoidable LC parasitics (L and C of PCB tracks, pins, IC, XTAL, caps etc). It is thus essential to verify all XOSC parameters in the final design, since there is large influence of all components on the final performance. Additionally, crosstalk via supply, ground or surrounding signal lines, as well as intercepted RF fields from outside will contaminate the XOSC output signal, which might cause no troubles for digital circuits, but become critical for output PLL signals.

- Verify crystal oscillator startup time and oscillation margin in the final design (most probably no automated tests possible). Take care that **oscillation margin** depends on complete circuit incl. PCB. Too low oscillation margin can cause XOSC malfunction with marginal crystals (higher R), leading to no oscillation or parasitic oscillation at some arbitrary frequency.
- For quartz crystals not explicitly recommended by IFX (product datasheet + recommended XTAL list on IFX homepage) contact XTAL manufacturer for design review and approval.

- Keep all XOSC lines as short and as shielded as possible to avoid EMC issues due to coupling with external disturbers. Check the EMC performance of your XOSC design.

2.3 SPI/I2C Communication

The integrity of the chip configuration and thus your design's functionality and performance depends on error-free SPI or I2C communication between the host µC and IC.

- Keep the bus length as short as possible: long bus lines will induce substantial capacitive load (high current spikes in the drivers ➔ high digital noise, higher current consumption and lower max. data rate) and increase the crosstalk probability.
- Bus communication routines (SPI, I2C) and data transfer (Tx ⇔ Host) are verified during this phase, as well as timing.
- Use SPI tracking or checksum registers (not available in all products) in your application and in the verification test to validate the bus implementation (FW and electrical) in an endurance (loop) test. You may want to apply EMC stress during this test.
- Implement bus communication timing compliant with datasheet requirements and verify that.

2.4 ESD Performance

- Check ESD performance (especially on sensitive nodes e.g. antenna connection, battery connection)

3 Receiver Verification Guidelines

RX verification is related to reception performance and functional verification of the whole subsystem including properly configured RF hardware with Infineon IC and system host with firmware. The closer the HW and SW configuration is to your final product, the higher is the confidence level. These tests should be performed in a controlled environment, i.e. in an **RF chamber**, to exclude unwanted interference and to ensure repeatability. Following verification tests should be done by the customer on the final hardware (typically using an automated test environment):

- Verify all parameters specified by your customer(s) first (e.g. OEM).
- Verify receiver sensitivity over all relevant parameter tolerances, e.g. using **multidimensional sweep** tests over:
  - Data rate
  - FSK deviation / ASK modulation depth (modulation index)
  - RF frequency offset between transmitter (TX) and receiver (RX) unit
  - Temperature
  - Bi-phase duty-cycle
  - Supply voltage
- In case several air-interface protocols must be supported, all must be tested using multidimensional sweep.
- In case an external LNA is used, check for **unconditional stability** and pay special attention to large signal behavior (IIP3).
- Apply Missed Message Rate (MMR) tests, where same TX frame is sent in the loop, repeatedly (e.g. 10000-times) at a "good" RF level (e.g. -80dBm) and finally all transmissions must be received correctly (BER/MER ~ 0). This test is very helpful for verification of SelfPollingMode (SPM) use-cases and functionality and timing constraints check.
- Apply False Alarm Rate (FAR) tests (especially for SPM use-cases), where no transmission is initiated, and therefore no Wake-up is expected during SPM (e.g. use NINT source Wake-up)
  - unwanted wake-up in noise may block reception of following wanted frame
  - increased FAR leads to increased average current consumption
- Verify reception over desired dynamic range of receive RF power level over all relevant parameters (incl. larger RF levels up to expected max. input power)
- Verify EMC performance
  - Radiated emissions:
    a) Identify relevant regulations
    b) Perform own measurements

    - c) Go for certification
  - Immunity:
    - a) Identify relevant EMI sources inside and outside of the application circuit
    - b) Measure the performance
    - c) Go for certification
- Verify general fulfillment of all regional regulations (FCC, ETSI, others)
- Verify behavior in presence of interfering/jamming signals (also known as “blocker measurements” or blocking performance):
  - Perform blocking performance measurement over input frequency to check all filtering components from antenna to demodulator (e.g. SAW, ceramic filter, BPF…)
  - Measure adjacent channel rejection for multichannel applications/systems
  - Check blocking performance at known strong external interference sources (e.g. LTE, TV…)
  - Check blocking performance at all **image** frequencies, use high-side/low-side LO injection to “escape” strong known interferers
  - Source of interference can also be the own application (host) µC or other critical components on the PCB generating strong discrete signals or fields
- Always log in parallel as many system parameters as possible to catch any irregularity (e.g. current consumption)
- If transmitter system is also exactly known at the RX design time or designed in parallel, it is recommended to use the final TX design (i.e. keyfob, remote control or TPMS sensor device) and perform the TX+RX joint system tests with corner (worst-case) and typical cases

4 Transmitter Verification Guidelines

TX verification is related to RF transmit performance (modulation quality, phase noise, spectral purity, occupied bandwidth, output power, power consumption) and functional verification of the whole subsystem including properly configured RF hardware with Infineon product and system host with firmware. Again, the closer the HW and SW configuration is to your final product, the higher is the resulting confidence level.
Following verification tests should be done by the customer on the final hardware (typically using an automated test environment):

- Verify first all parameters specified by your customer(s) (OEM).
- Check Transmit Frequency Variation over: temperature, supply voltage.
- Verify transmit time duty cycle (-> FCC Part 15D).
- Measure relevant transmission signal quality:
  - Phase noise performance vs. PLL BW settings
  - TX spurious, in-band noise
  - Eye Diagram or Constellation diagram (for GFSK, MSK ➔ filter settings) vs. PLL BW
  - Max./min. deviation, zero-crossing jitter, Inter-symbol-interference, occupied bandwidth with worst-case modulation
- Output TX Power Variation over: temperature, supply voltage
- PA Output Power vs. PA power settings to find optimum number of PA stages / optimum load impedance.
- PA Efficiency over: temperature, supply voltage.
- Verify the worst case voltage swing (peak voltage) on the PA output pin (mismatch, high supply voltage).
- Coarse check of harmonics and radiated power (consider influence of antenna; do not rely only on “ideal” 50 Ohm broadband measurement).
- Verify EMC performance
  - Radiated emissions:
    - a) Identify relevant regulations
    - b) Perform own measurements
    - c) Go for certification
  - Immunity:
    - a) Identify relevant EMI sources inside and outside of the application circuit
    - b) Measure the performance
    - c) Go for certification

- Verify general fulfillment of all regional regulations (FCC, ETSI, …):
  - Consult and understand the specific regulation. This is a necessary but not sufficient condition for success of undergoing work.
  - DUT tested under “most unfavorable” conditions (from regulatory viewpoint)
  - Example (test case): level of unintentional transmissions (harmonics & intermodulation products) under maximum supply voltage and low temperature conditions ➔ yields max. radiated power. Note: according ETSI &FCC rules, the “adverse” conditions shall be declared by commissioner. Test shall pass ETSI EN 300-220 and/or FCC Part 15D.
- Check influence of variation of external components e.g. matching network tolerances (capacitors, coils) on PA efficiency and harmonics.
- Check influence of antenna detuning (impedance variations) due to environment variations (e.g. hand-effect for remotes/keyfobs, different mounting locations):
- PA efficiency, harmonics.
- Pulling effect (feedback to PLL/VCO) and distortion of transmit spectrum, freq. accuracy.
- Measure and collect the production tolerances (e.g. Pout, center frequency) over higher quantities and:
  - Center the configuration parameters and
  - Identify parameters requiring trimming/calibration procedures
- Early overall transmission test with application receiver: if possible BER and MER - if receiver system is also exactly known at the TX design time or designed in parallel, it is recommended to use the final RX design and perform the TX+RX joint system tests with corner (worst-case) and typical cases.

5 Transceiver Verification Guidelines

For transceiver-based designs, all points relevant for RX and TX have to be addressed first. Still there are some additional points which need to be considered:

- Verify all desired operation modes of the application and the transition between the modes, especially turnover time (RX ➔ TX, TX ➔ RX).
- Check max power ratings of RF filter stages (e.g. SAW) and RF switches for TX operation
- For symmetric systems, perform functional tests with two systems in a face-2-face configuration and operate the system in the corner (worst case) configurations
- For asymmetric systems setup the test case with proper peer equipment and operate the system in the corner (worst case) configuration

6 Conclusion

This document presented some common & best practice recommendations and guidelines for verification and test of RF systems based on Infineon WLC and TPMS products.
Infineon application engineering team wishes you an exciting and in the first place successful design and verification work with our integrated circuits. In case you have any questions to this document please feel free to contact our Customer Support service.

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