CoolMOS™ C6
Mastering the Art of Slowness

Application Note

CoolMOS™ C6

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Revision History	
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1 Introduction

With the introduction of its fifth Superjunction generation CoolMOS™ C6 Infineon Technologies sets a new reference in the market for High voltage MOSFETs. We aimed at a combination of ultra-low $R_{DS(on)}$, high ruggedness and fast but well controlled switching speed. The application measurements show a very good light load efficiency in comparison to our own devices and competitor parts, a fault tolerant behavior in abnormal conditions such as turn-on on a conducting body diode and a well controlled switching characteristic especially in peak current conditions such as load steps, start-up and AC cycle drop out etc. Table 1 shows the device characteristics in comparison to previously launched CoolMOS™ generations. The first family CoolMOS™ S5 established the new Superjunction principle in the market and was the first High voltage MOSFET to break the limit line of silicon. This means it achieved an area-specific on-resistance which has been unreachable for conventional high voltage MOSFETs. The second family CoolMOS™ C3 is today the best selling Superjunction MOSFET worldwide and helped to create the brand of "CoolMOS". Its combination of low $R_{DS(on)}$, fast but well controlled switching speed, high ruggedness and user friendly behavior especially in abnormal operation conditions led to a very wide field of applications where this device is used today and a big market success overall.

The following families CoolMOS™ CFD and CoolMOS™ CP addressed specific markets and their needs; the CFD comes with a fast body diode for very high ruggedness in hard commutation and a very low reverse recovery charge for applications such as HID lamps, resonant SMPS topologies and applications with increased reverse requirements such as the Photovoltaic market. CoolMOS™ CP is our high performance series [5], which sets the benchmark in switching speed and efficiency. The device marks the border of silicon performance in the Superjunction arena; the realization of the potential of the device requires special care in layout and routing. For the use of CoolMOS™ CP we refer to the specific Application Note, which can be found on our Homepage.

	Market entry	Voltage class [V]	Special characteristic	V_{gs},th [V]	G_{fs} [S]	Internal R_g [Ohm]
CoolMOS™ S5	1998	600	Low $R_{DS(on)}$, Switching speed close to standard MOSFETs	4.5	Low	High
CoolMOS™ C2	2000	600	Fast switching speed	4.5	Low	Low
CoolMOS™ C3	2001	500/600/ 650/800	Fast switching speed, symmetrical rise/fall time at V_{gs}=10V	3	High	Low
CoolMOS™ CFD	2004	600	Fast body diode, Q_{rr} 1/10th of C3 series	4	High	Low
CoolMOS™ CP	2005	500/600	Ultra-low $R_{DS(on)}$, ultra-low Q_g, very fast switching speed	3	High	Low
CoolMOS™ C6	2009	600	Ultra-low $R_{DS(on)}$, low Q_g, fast and well controlled switching	3	High	High

Table 1: CoolMOS™ series at a glance.

The target of CoolMOSTM C6 was to create a general use part, similar to CoolMOSTM C3 series. So what can be improved in the C3 series? First of all the availability of better best-in-class parts such as 380mΩ in DPAK, 99mΩ in the TO-220 and 45mΩ in the TO-247 as already established with our high performance series CP. Second the energy stored in the output capacitance, as this parameter is decisive for the efficiency in high line or light load conditions. The third target was the ruggedness in failure cases such as hard commutation of the conducting body diode (for this application range our competitors as well as we came forward with special versions such as CFD, which is based on heavy life time-killing of the mobile carriers inside the MOSFET).

And last but not least we wanted to reduce the cost associated with the production of a given $R_{DS(on)}$. All these benefits should however come with the fast but well controlled switching behavior, which makes CoolMOS™ C3 very easy to design-in and which makes C3 the most popular Superjunction device today in the market. CoolMOS™ C6 is providing all of the above mentioned benefits as well as fast and well controlled switching behavior.

2 The Superjunction Principle

All CoolMOS™ series are based on the Superjunction (SJ) principle, which is a revolutionary technology for high voltage power MOSFETs [1, 2]. Infineon Technologies has been the first company worldwide to commercialize this idea into the market [4]. Where conventional power MOSFETs just command on one degree of freedom to master both on-state resistance and blocking voltage, the Superjunction principle allows to degree of freedoms for this task. Therefore conventional MOSFETs are stuck with the limit line of silicon, a barrier which marks the optimum doping profile for a given voltage class. This limit line has been theoretically derived by Chen and Hu in the late 80ies [3]. No commercial product has an on-state resistance better than the limit line of silicon.

In contrast to that the Superjunction principle allows to reduce the on-state resistance of a high voltage MOSFET virtually to Zero, limited only by technology efforts and manufacturing

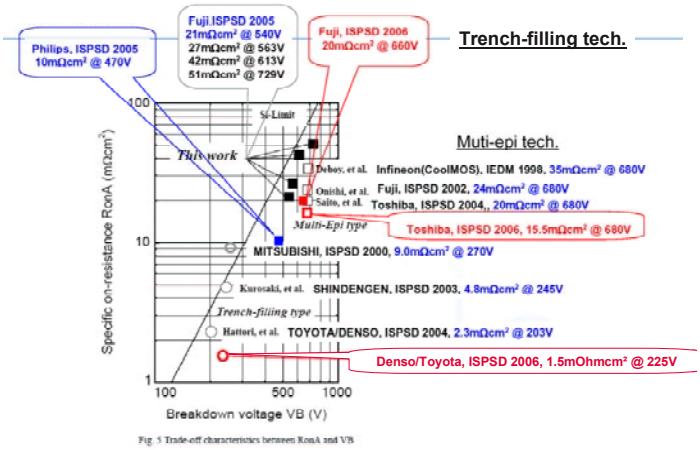

Fig. 1: The race for the lowest area specific $R_{DS(on)}$.

capabilities. Fig. 1 shows the race for the lowest specific on-state resistance, commercial state-of-the-art is 24mΩ *mm² reached in 2005 with CoolMOS™ CP. The basic idea is simple: instead of having the electrons flowing through a relatively high resistive (high voltage blocking) n--area, we allow them to flow in a very rich doped n-area, which gives naturally a very low on-state resistance. The crucial point for the SJ technology is to make the device block its full voltage, which requires a careful balancing of the additional n-charge by adjacently positioned deep p-columns, which go all the way straight through the device close to the back side n+ contact. This is where manufacturing capability comes in, as the charges within the device needs to be compensated precisely under the constraints of a mass market production line. Fig. 2 shows cross sections of a conventional MOSFET (left) and a CoolMOSTM (right) in comparison. For the interested reader we refer to the literature [3..10].

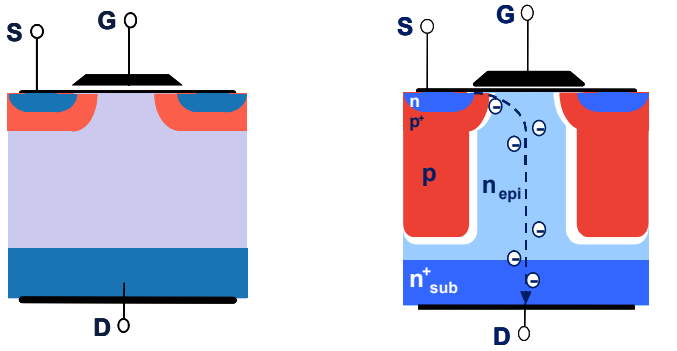

Fig. 2: Schematic cross-section of a standard power MOSFET versus a Superjunction MOSFET.

The SJ principle gives us the opportunity to create best-in-class types, which have not been possible before such as a 100 mΩ/600V part in a TO-220 package. Furthermore it allows making parts with very low capacitances for a given $R_{DS(on)}$ as the silicon chip is much smaller than for a conventional power MOSFET. Both input and high voltage level of the output capacitance scale directly with the chip size, whereas reverse capacitance and to some extent the low voltage level of the output capacitance is technology dependent. Characteristic of all Superjunction devices is a strong non-linearity of the output capacitance with high values at low voltage and low values at high voltage. This behavior can be easily understood if you take into account that the output capacitance is proportional to the area of the blocking pn-junction and inverse proportional to the width of the space charge layer (or the voltage sustaining area). At low voltage the p-columns are not depleted and form a very big surface, furthermore the width of the space charge layer is very narrow (the white area in Fig. 2, left). At high voltage however the p-columns are fully depleted and the space charge layer has reached its full extension of roughly 45µm for a 600V device. Important is that the non-linearity of the output capacitance allows a quasi zero-voltage-switching (ZVS) turn-off of the device, lowering turn-off losses. Superjunction devices are by nature fast in switching. Very small capacitances together with a low gate charge make rise and fall times of a few nanoseconds a reality. The further we go in exploitation of the SJ principle, the faster the devices will get, if we do not take counter actions. In the C6 family we have taken these counter actions, the application note is therefore entitled "**Mastering the Art of Slowness**".

3 Technology Comparison of CoolMOS™ C6 vs. CP and C3

CoolMOS™ C6 is a well balanced modern Superjunction high-voltage MOSFET with the following characteristics:

- Best-in-class types down to 41mΩ in TO-247 and 99mΩ in TO-220 respectively
- Fast but well controlled switching speed
- Very low energy stored in output capacitance
- High ruggedness in hard commutation of the body diode
- Low gate current requirements

… which gives the application benefits …

- Compact and very efficient designs
- Fast and easy design-in, less care for peak current conditions such as during start-up, load jump, AC cycle drop out etc
- Very good light load efficiency in hard turn on applications
- No need for more expensive fast body diode types, less care for abnormal conditions during start-up etc
- No need for high current sinking gate drivers, better system cost and more choice

Table 2 shows a comparison of key characteristics as published in the datasheet.

Specification	Symbol	IPW60R190C6	SPW20N60C3	IPW60R199CP
On-state resistance, maximum rating, 25 °C	$R_{DS(on)}$	190 mΩ	190 mΩ	199 mΩ
Drain current rating	I_D	20 A	20 A	16 A
Pulse current rating	$I_{D,\ pulse}$	59 A	62 A	51 A
Typical Gate - Drain charge	Q_{gd}	32 nC	33 nC	11nC
Total Gate charge	Q_g	63 nC	87 nC	32 nC
Energy stored in output capacitance @400V	E_{OSS}	5 µJ	10 µJ	7.5 µJ
Thermal resistance, junction-case	$R_{thJC,max}$	0.83 K/W	0.6 K/W	0.9 K/W
Body diode, reverse recovery charge	Q_{rr}	7 µC	11 µC	5.5 µC
Body diode, di/dt	dI_F/dt	500 A/µs	400 A/µs	200 A/µs
Body diode, dv/dt	dv/dt	15 V/ns	15 V/ns	15 V/ns

Table 2: Key feature comparison of CoolMOS™ C6 versus C3 and CP series.

The target for CoolMOS™ C6 is to provide fast but controlled switching and a good compatibility with layouts, where source inductances have not been brought to the absolute minimum. The basic idea is to provide a high voltage MOSFET, which is significantly fast at normal operation conditions and very limited overshoot in di/dt or dv/dt at high peak current conditions.

3.1 Switching Characteristics

Fig. 3 and 4 show a technology comparison C6 versus C3 and CP for di/dt and dv/dt both during turn on and turn off at currents of 5A and 16A respectively. For all devices the R_g was chosen at 3.3Ω, the junction temperature is 125°C. C3 and C6 have an on-state resistance of 190mΩ, CP of 199mΩ.

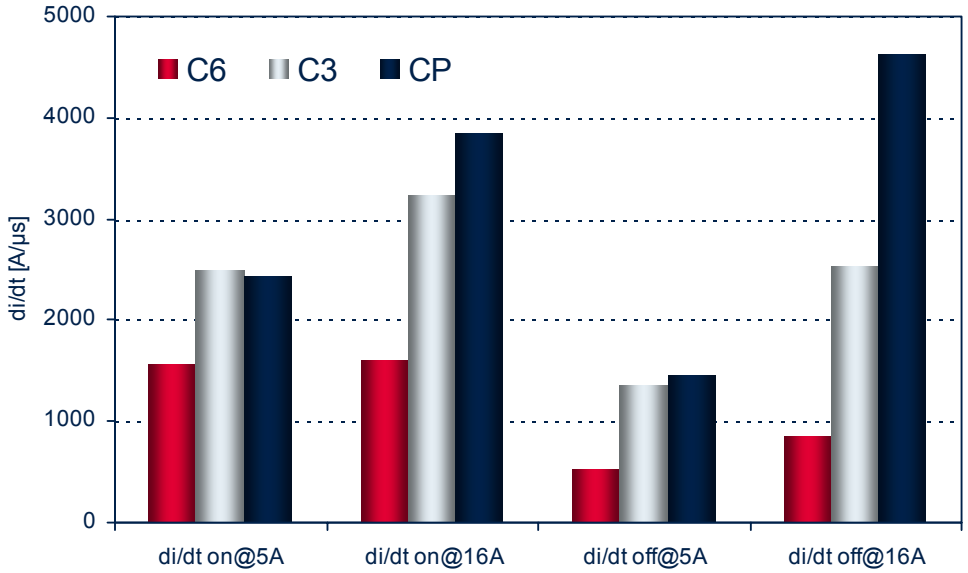

Figure 3: Comparison of switching characteristic, di/dt at turn on and turn off for 5A and 16A respectively, 190 / 199 mΩ types, R_g 3.3Ω, Tj 125°C.

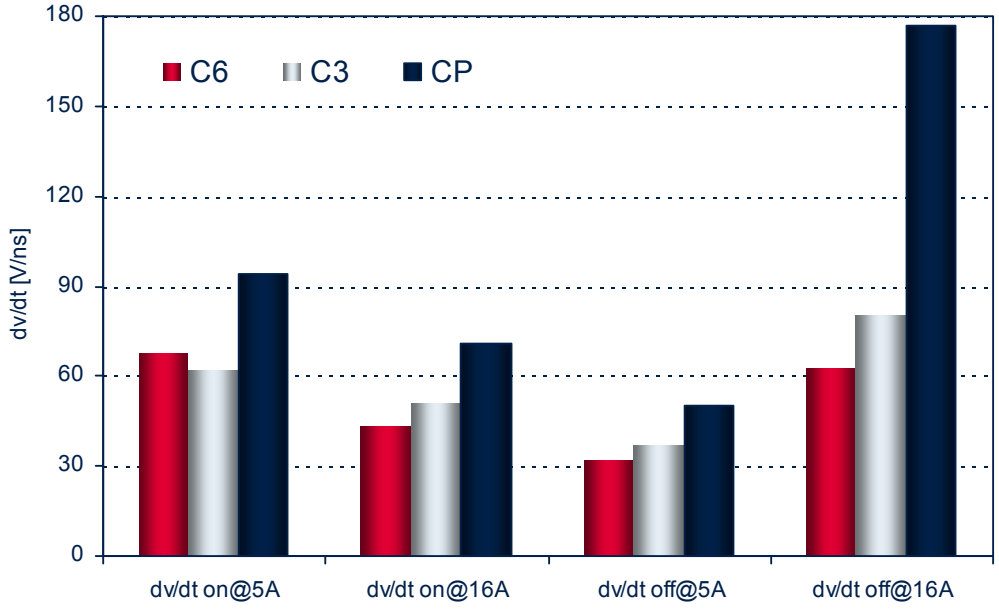

Figure 4: Comparison of switching characteristic, dv/dt at turn on and turn off for 5A and 16A respectively, 190 / 199 mΩ types, R_g 3.3Ω, Tj 125°C.

As can be clearly seen from Fig. 3 CoolMOS™ C6 shows relatively low values of di/dt both during turn on and during turn off. There is no increase in di/dt during turn on and only a small increase in di/dt during turn off when the current changes from 5A to 16A. This gives the designer safety in peak current conditions such as AC cycle drop out, start up or load jumps as the di/dt basically stays in the range of normal operation conditions. Therefore the likelihood of unwanted oscillations or dangerous gate spikes is significantly suppressed. For those who might consider 500A/µs a low di/dt value at turn off, please remember that a source inductance of only 10 nH only will already yield a voltage drop of 5V, which will bring the MOSFET already for short time into the Miller plateau via inductively induced turn on. As both the TO-220 and TO-247 package have parasitic source inductances of 5 nH already there is little room for layout routing to stay below 10 nH. In other words with conventional packages such as TO-220 or TO-247 there is little to no benefit from higher switching speeds than 800 to 1000A/µs. The self limitation of di/dt to these values being implemented in CoolMOS™ C6 does therefore not hurt efficiency wise but brings safety in peak current conditions and helps with the use of the part in non-ideal layout environments.

We get a similar picture from dv/dt both at turn on and turn off. The device shows reasonably fast turn on and turn off transients in the range of 50…60V/ns to ensure low turn on and turn off losses. The values are close to what CoolMOS™ C3 would yield under identical conditions, thus facilitating the change of designs from C3 into C6 to participate in the best-in-class offerings, improved E_{oss} and gate charge characteristics and last but not least attractive price structure of the more modern CoolMOS™ class. Furthermore CoolMOS™ C6 does not show extremely high dv/dt values at turn off under peak current conditions, as untamed Superjunction devices naturally tend to do due to ever decreasing output capacitance. The device supports therefore the aforementioned “Ease of use” with significantly suppressed tendency to unwanted ringing and gate spikes.

3.2 Device Capacitances

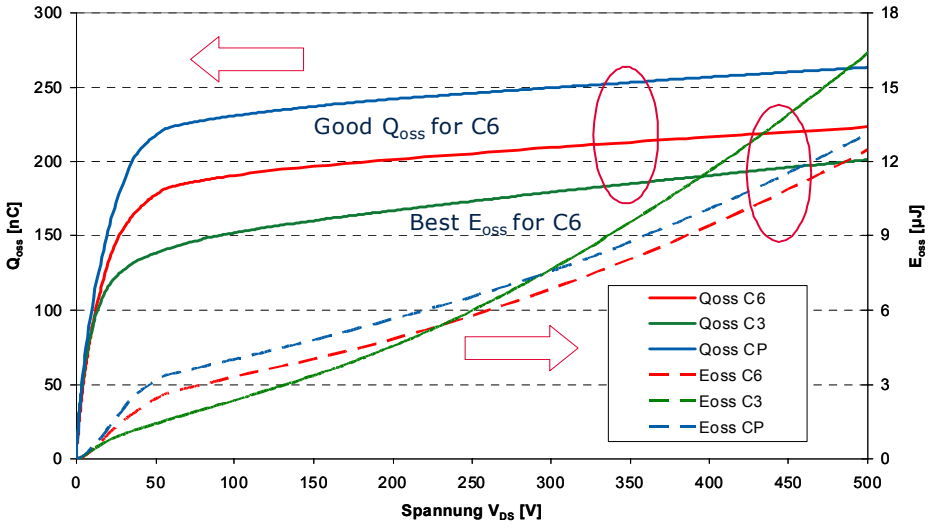

Figure 5: Comparison of the energy stored in the output capacitance E_{oss} and the capacitive displacement charge Q_{oss} for CoolMOS C6 versus C3 and CP.

Fig. 5 shows a comparison of the energy stored in the output capacitance E_{oss} and the capacitive displacement charge Q_{oss} as a function of the voltage the device is charged up to. As can be seen clearly from the graph the new CoolMOS™ generation C6 shows the best E_{oss} values at 400V, which helps to lower the capacitive losses in applications with hard turn on such as continues current mode PFC applications. As the capacitive losses are load independent these loss contribution typically shows off during light load conditions, when both conduction and Joule switching losses get lower due to their square or linear relationship with load current respectively. At 200V the E_{oss} curve of C6 intersects with C3 yieding similar capacitive losses at this operation point, which is e.g. important for Two Transistor Forward (TTF) and Interleaved TTF topologies.

The capacitive displacement charge Q_{oss} shows values in-between our previous families CoolMOS™ C3 and CP. The Q_{oss} charge is a measure for the time it takes to charge up the device from 0V to the voltage shown on the X-axis. This time is important for the dead time considerations in resonant switching applications such as the LLC converter.

3.3 Commutation Ruggedness

A further point of interest in resonant switching applications is the topology's inherent possibility of turning on into the conducting body diode of the same leg. This condition may appear in LLC converters during start up or load jumps and is also not unknown in phase shift ZVS applications. As shown in Table 2 the CoolMOS™ C6 technology comes with a lower Q_{rr} than C3 and higher di_F/dt max ratings than both CoolMOS™ C3 and CP. Care was taken from device design point-of-view to smooth the discontinuation of the reverse recovery current after the reverse recovery peak. Furthermore the hard commutation benefits considerably from the relatively low di/dt values CoolMOS™ C6 shows during turn on. The turn on speed can be brought down further to 500A/µs by using a turn on gate resistance of 33Ω. Therefore the di_F/dt can be easily adjusted by increasing the turn on gate resistor. The limitation of dv/dt across the diode under hard commutation is a more difficult task. As shown in the hard commutation measurements of Figs. 6 and 7 (at dif/dt slightly above the max rating of the datasheet) a violation of dv/dt max ratings is more likely at low forward current. In this case there is a higher tendency of a sharp discontinuation of the reverse recovery current. Please see Fig. 7 for the high dirr/dt after the reverse recovery peak. To soften the reverse recovery phase after the reverse recovery peak more charge is needed. CoolMOS™ C6 achieves this by allowing a soft capacitively coupled turn on of the MOS channel. The resulting sharp current discontinuation is therefore largely reduced.

In terms of reverse recovery charge and reverse recovery time our fast body diode series CoolMOS™ CFD is still the best option for applications requiring a fast body diode. For cases which are in need to survive hard commutation of the body diode only occasionally without periodic use the inherent high commutation ruggedness of CoolMOS™ C6 is however an asset. We therefore clearly recommend CoolMOS™ C6 for resonant applications such as LLC and phase shift ZVS.

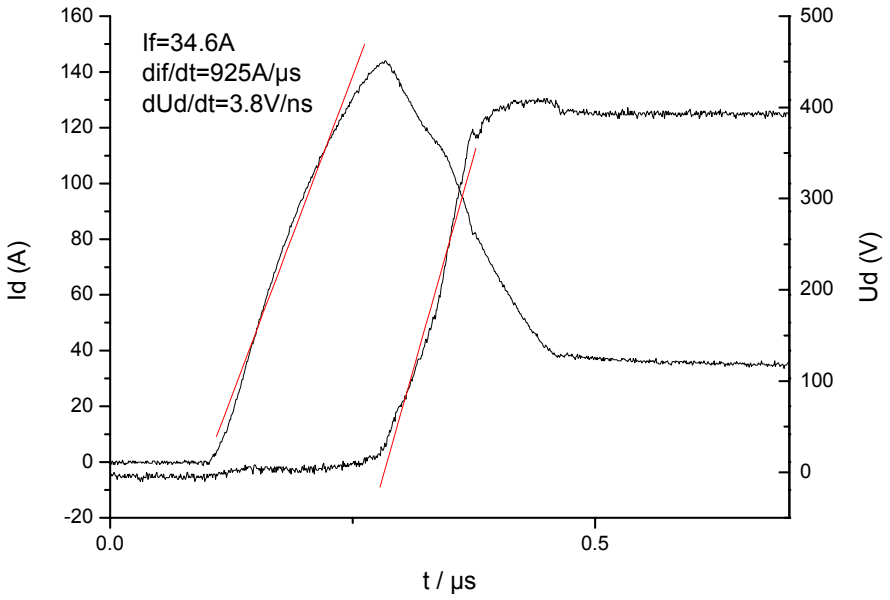

Fig. 6: Hard commutation of body diode CoolMOS™ C6 at a forward current of 37A.

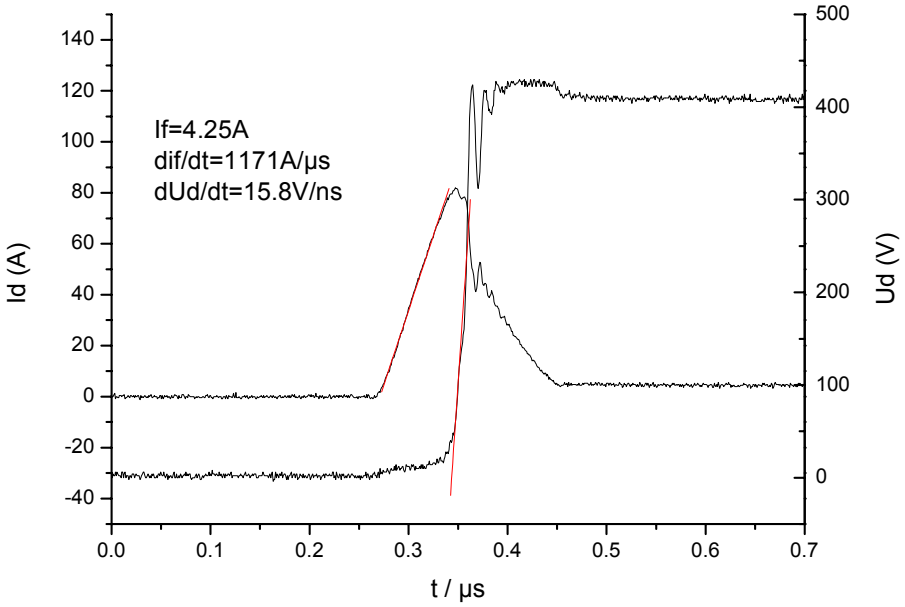

Fig. 7: Hard commutation of body diode CoolMOS™ C6 at a forward current of 4A .

3.4. Gate Charge and Integrated Gate Resistor

CoolMOS™ C6 comes with an integrated gate resistor in order to achieve self-limiting di/dt and dv/dt characteristics as discussed in the Chapter Switching characteristics. This integrated R_g allows fast turn on and turn off at normal operating current conditions but limits the di/dt and dv/dt in case of peak current conditions. The values of integrated R_g scales inversely with the gate charge respectively device capacitances. The following values have been chosen:

Type	Internal Rg [Ω]
IPx60R950C6	16.0
IPx60R600C6	17.5
IPx60R380C6	17.0
IPx60R190C6	8.5
IPx60R125C6	3.7
IPx60R099C6	1.6
IPW60R070C6	0.85

Table 3: Internal gate resistor for CoolMOS™ C6 series

Due to low gate charge plus integrated gate resistors the gate current is relatively low; hence the use of low cost gate drivers is therefore possible. In case of e.g. 190mΩ part the 8.5Ω integrated R_g limits the gate current to less than 2A even when switching with 0Ω from 0 to 15V. During the Miller phase the gate current will typically be even less than 1A. In combination with a relatively low total gate charge the losses dissipated in the driver are considerably lower as well.

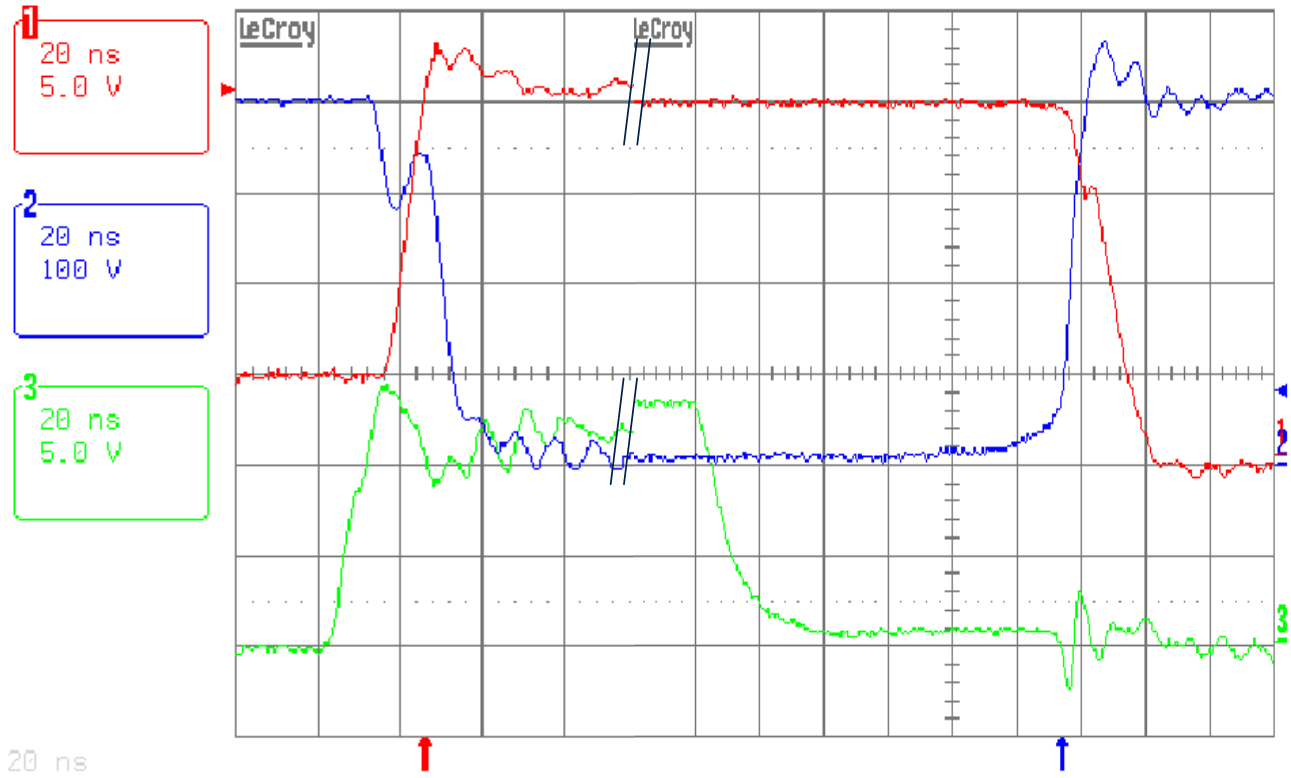

Fig. 8: Turn on and turn off waveforms of CoolMOS™ C6 IPP60R190C6 at 16A with an external R_g of 1.8Ω.

As shown in Fig. 8 the combination of low gate charge and internal gate resistor leads to smooth noiseless waveforms at peak current conditions even with extremely low external gate resistors of e.g. 1.8Ω. Please note that due to the ohmic voltage divider being present between the external and the internal gate resistor the gate voltage measured across the external R_g does not show the value of gate voltage being applied to the physical gate structure. During turn on you'll see the output of your driver, during turn off the gate voltage basically goes to Zero without visible Miller pateau.

We encourage to use very small external gate resistors to achieve optimum efficiency across a wide range of load conditions. Fig. 9 shows an efficiency comparison between CoolMOS™ C6 versus C3 and CP series. Using 0.6Ω external gate resistor with C6 (which corresponds to 9.1Ω R_g total) we reach the same efficiency level than with C3 at 4Ω or CP at 7Ω R_g (corresponding to 4.5Ω total or 9Ω total R_g for C3 and CP devices respectively). As shown in the inset CoolMOS™ C6 and CP show at light load conditions the highest efficiency, a benefit which is based on their lower energy stored in the output capacitance E_{oss}.

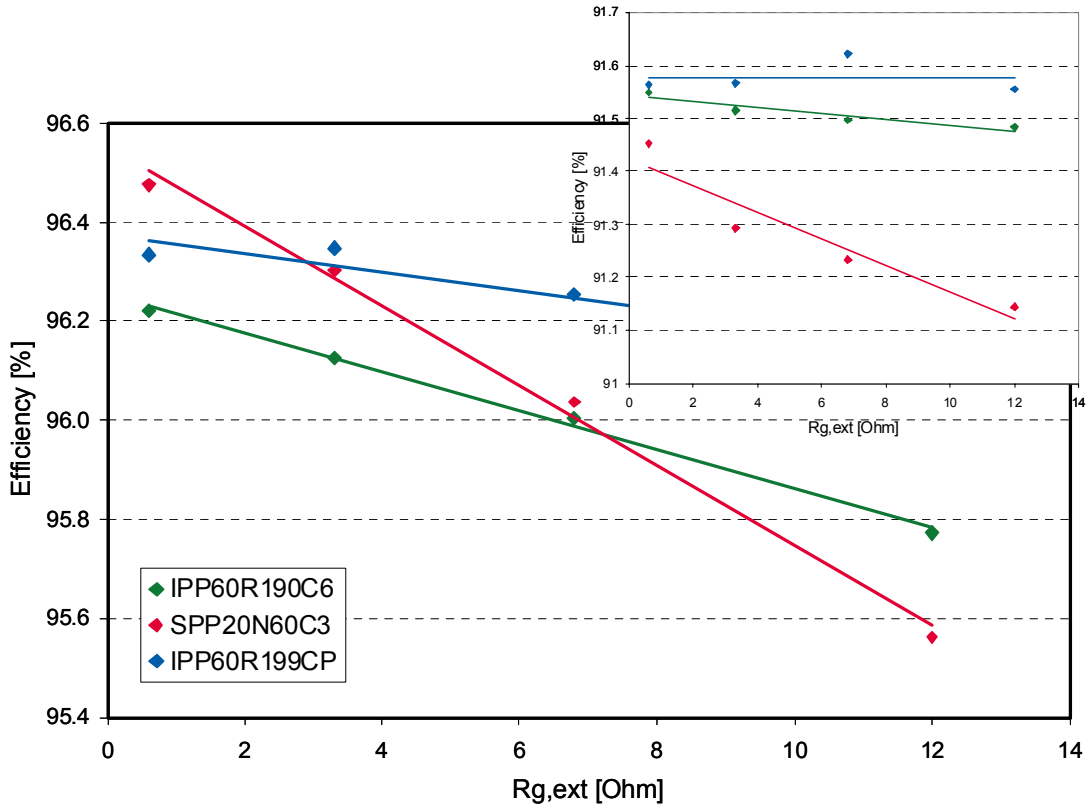

Fig. 9: Efficiency comparison of CoolMOS™ C6 versus CP and C3 series in a continues-current mode PFC stage at low-line full-load (main graph) and 20% load (inset top right) conditions.

3.5 Paralleling

Due to integration of gate resistors and matching gate charge characteristics CoolMOS™ C6 shows a significantly suppressed tendency to gate spikes and ringing even under peak current conditions. Fig. 10 shows the current ramp up in a continues current mode boost stage after AC cycle drop out. As clearly visible there is no gate spike up to a current level of 60A, which corresponds to three times rated nominal current.

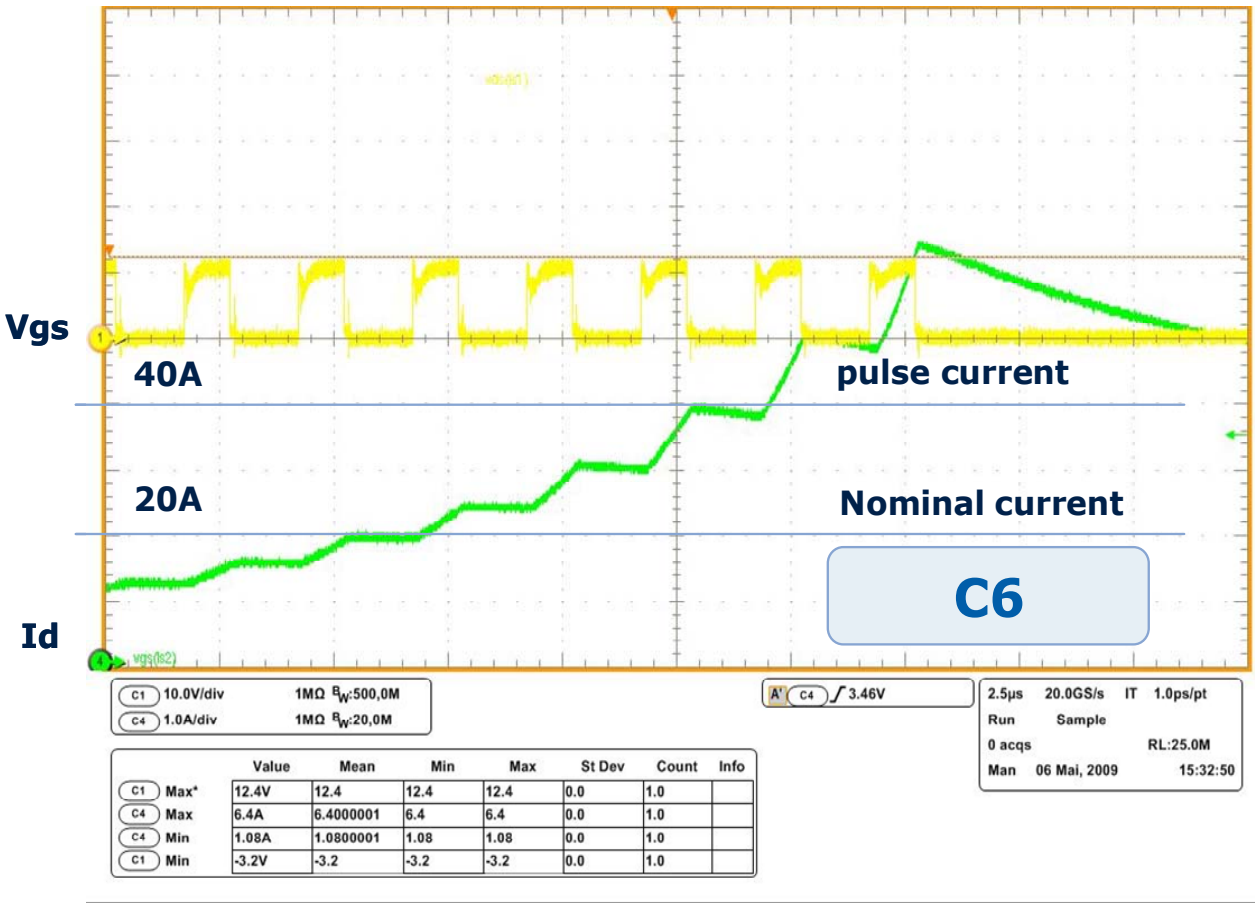

Fig. 10: Gate and current signals after an AC cycle drop out, 190 Ω C6.

Due to all measures taken from a device design point of view to suppress gate spikes Infineon Technologies recommends the layout suggestions and gate driver setup as e.g. described in the application note CoolMOS™ CP. The use of ferrite beads on the gate is recommended for paralleled devices.

4 Application Results and EMI Considerations

Driven by initiatives such as 80+ and the ubiquitous energy efficiency demands power supplies need to deliver a very high efficiency over a broad load and input voltage range. These requests translate into more demanding semiconductor requirements as well as more strict discipline in avoiding parasitic inductances and capacitances in the layout.

4.1 *Example 1: 400W Silverbox CCM PFC Stage, 67 KHz*

As shown in Fig. 11, different 190mΩ MOSFETs in a TO-220 FullPAK package are measured in a 400W silverbox at 115 V_{ac} and 230V_{ac} respectively. CoolMOS™ C6 shows higher system efficiency than a competitor SJ MOSFET across the entire load range.

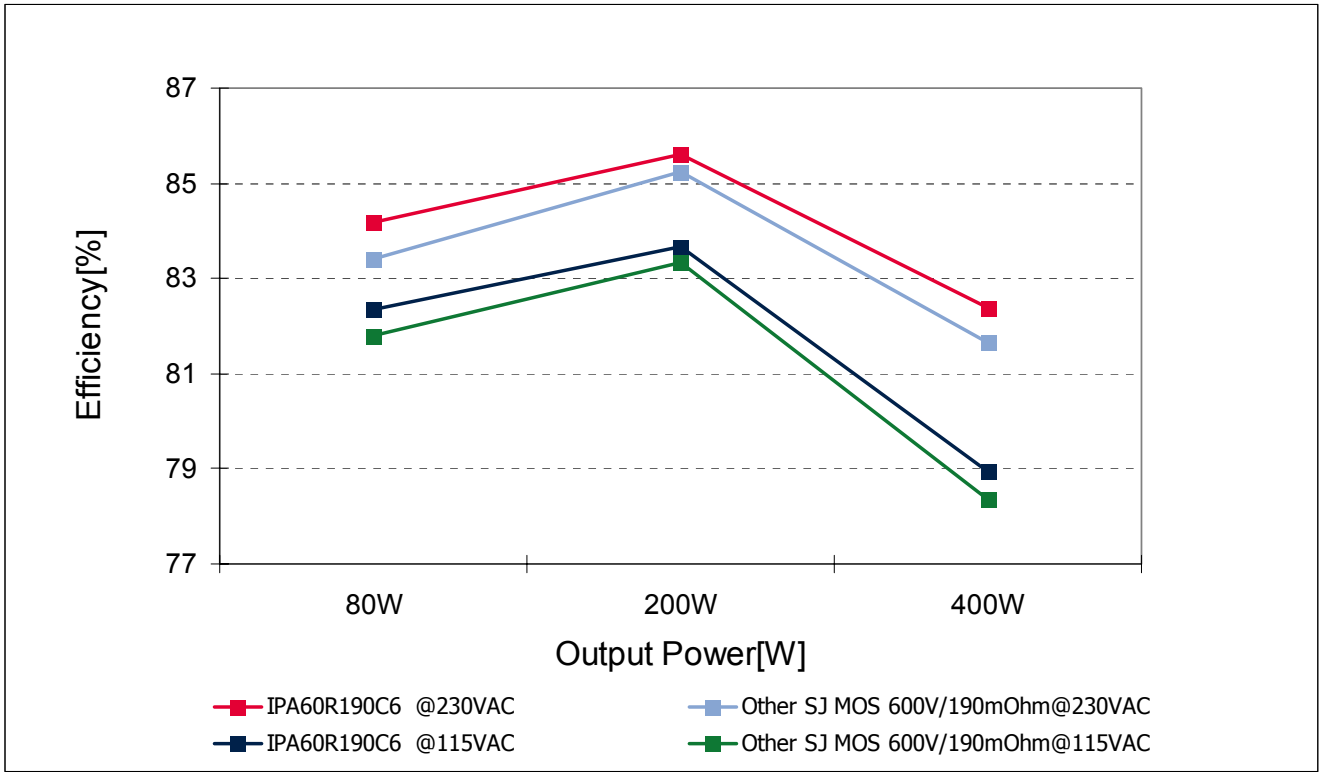

Fig. 11: System efficiency versus load for different input voltages of a 400W silverbox.

4.2 *Example 2: 135W Adapter using QR Flyback Topology*

As shown in Fig. 12 and 13, the Quasiresonant (QR) PWM stage of a 135W adapter uses CoolMOS™ to have a better efficiency and a satisfying EMI performance. The C_{ds} oscillates with the transformers main inductance to reach a low voltage switching loss and good EMI result. For QR PWM with C6 we only changed C_{ds} from original 100pF to 220pF. With this small change we obtain 4~5 db EMI improvement that versus CoolMOS™ C3 with 100pf C_{ds}. The efficiency at 100% load and high line 230V_{ac} is 0.35% worse, however C6 has 0.35% better efficiency than C3 at 20% load. Over all C6 has better efficiency at 115Vac input which normally is the worst case in adapter application. A 10 Ohm external R_g is used for both C6 and C3. The efficiency of the figure below is the system efficiency including DCM PFC and QR Flyback PWM stage.

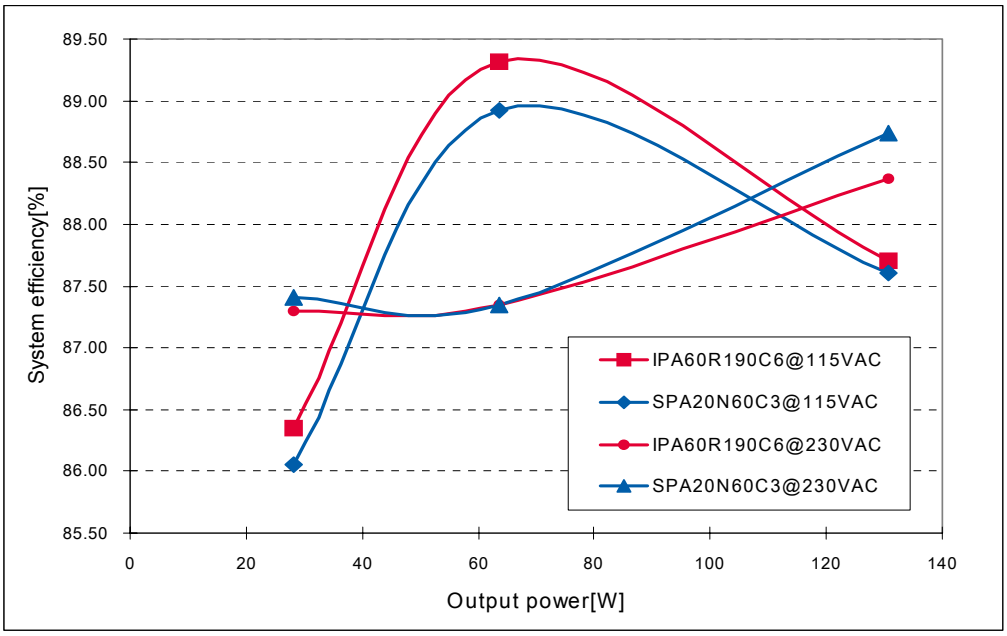

Fig. 12: System efficiency versus load for different input voltages of a 135W adapter

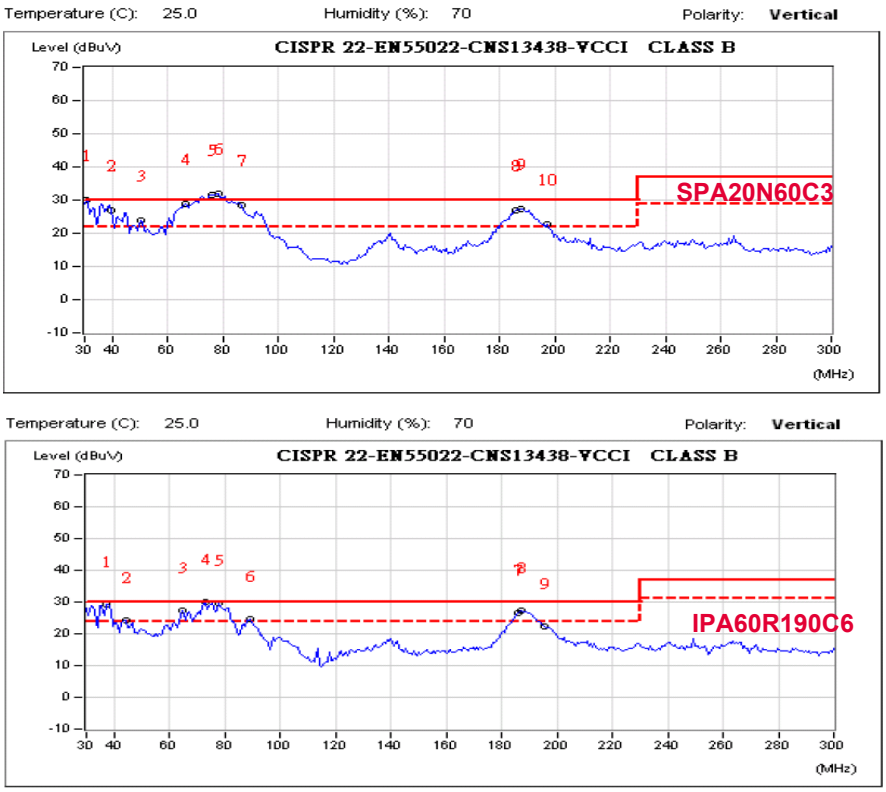

Fig. 13: QR PWM RFI performance of a 135W adapter at 230V_{ac}

CoolMOS™ C6 shows similar RFI performance with 220pf C_{ds} compared to CoolMOS™ C3 with 100pf C_{ds} in QR PWM topology. From the additional C_{ds} capacitance there is a slight increase in turn on losses but reduced dv/dt during turn off. This EMI test was set up with a dummy load without notebook connected.

v

4.3 Example 3: 300W Silverbox using TTF Topology

As seen in Fig. 14, 600V CoolMOS™ C6 gives the highest efficiency per $R_{DS(on)}$ class using the TTF stage of a commercially available 300W silverbox power supply. C6 is better than C3, CP and other competitors with 0.2 ~ 0.5% at 20% load due to its smaller output capacitance which leads to lower switching losses. Changing from less advanced SJ technologies or conventional MOSFETs to new CoolMOS™ series with identical $R_{DS(on)}$ enables a higher system frequency. This will result in smaller passive components and hence a reduction in form factor. The efficiency of below figure is system efficiency including CCM PFC stage and the TTF PWM stage. Since the integrated R_g of IPA60R190C6 is bigger, the external R_g can be adjusted to a lower value to gain a better efficiency.

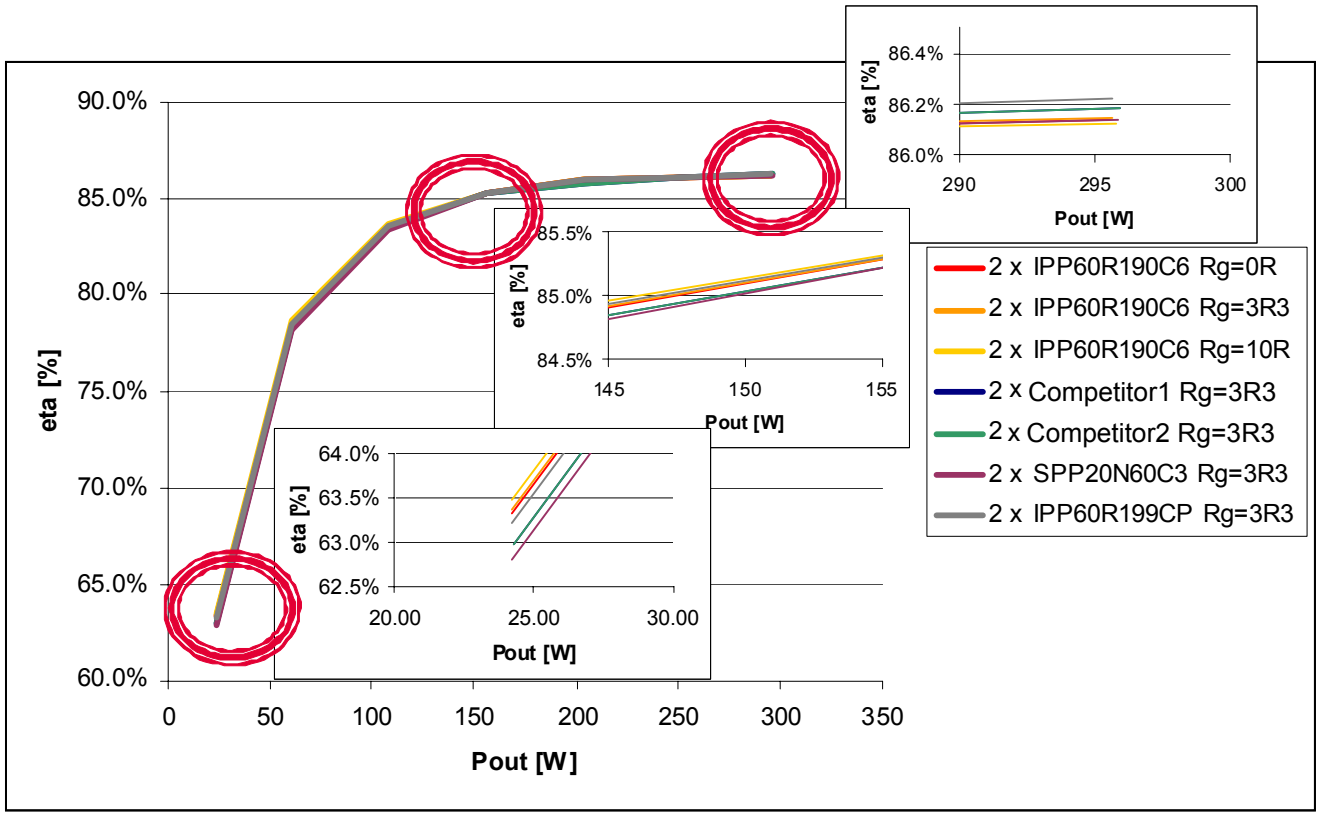

Fig. 14: System efficiency versus load of a 300W silverbox, comparing 600V CoolMOS™ C6 with C3 and other 600V MOSFETs

5 Product Portfolio and Naming System

CoolMOS™ C6 series follows the same naming guidelines as already established with the CP series e.g. IPB60R099C6, where I stands for Infineon Technologies, P for power MOSFETs, B for the package TO-263, 60 for the voltage class (divided by 10), R099 for the on-state resistance in Ohms and C6 for the name of the series. Fig. 15 shows the portfolio of CoolMOS™







	TO-220 FullPAK	D²PAK (TO-263)	DPAK (TO-252)	I²PAK (TO-262)	TO-220	TO-251 Short Leads	TO-247
3.000 Ω			IPD60R3K0C6				
2.000 Ω			IPD60R2K0C6				
1.400 Ω			IPD60R1K4C6		IPP60R1K4C6		
0.950 Ω	IPA60R950C6	IPB60R950C6	IPD60R950C6		IPP60R950C6		
0.750 Ω			IPD60R750C6		IPP60R750C6		
0.600 Ω	IPA60R600C6	IPB60R600C6	IPD60R600C6		IPP60R600C6		
0.520 Ω	IPA60R520C6		IPD60R520C6		IPP60R520C6		
0.450 Ω	IPA60R450C6		IPD60R450C6		IPP60R450C6		
0.380 Ω	IPA60R380C6	IPB60R380C6	IPD60R380C6	IPI60R380C6	IPP60R380C6	IPS60R380C6	
0.280 Ω	IPA60R280C6	IPB60R280C6		IPI60R280C6	IPP60R280C6		IPW60R280C6
0.190 Ω	IPA60R190C6	IPB60R190C6		IPI60R190C6	IPP60R190C6		IPW60R190C6
0.160 Ω	IPA60R160C6	IPB60R160C6			IPP60R160C6		IPW60R160C6
0.125 Ω	IPA60R125C6	IPB60R125C6			IPA60R125C6		IPA60R125C6
0.099 Ω	IPA60R099C6	IPB60R099C6			IPP60R099C6		IPW60R099C6
0.070 Ω							IPW60R070C6
0.041 Ω							IPW60R041C6

Fig. 15: Portfolio of CoolMOS™ C6.

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