TLE9260...63(-3)QX(V33)
MR-SBC Family

Reference: Data Sheet

TLE9263-3QX-Data-Sheet-110-Infineon, Rev 1.1

Errata Sheet

Overview

This document lists the errata of the MR-SBC Family related to the Data Sheet, TLE9263-3QX-Data-Sheet-110-Infineon, Rev 1.1.

It is strongly recommended that the device behavior and proposed workarounds are considered for the application.

Affected products

- TLE9260QX,
- TLE9260-3QX,
- TLE9260QXV33,
- TLE9260-3QXV33
- TLE9261QX,
- TLE9261-3QX,
- TLE9261QXV33,
- TLE9261-3QXV33
- TLE9262QX,
- TLE9262-3QX,
- TLE9262QXV33,
- TLE9262-3QXV33
- TLE9263QX,
- TLE9263-3QX,
- TLE9263QXV33,
- TLE9263-3QXV33

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1 Transceiver Enabling Times Can be Longer than Specified

Note: This behavior was already communicated via the EPN "TLE9260_63QX-EPN-100-Infineon" in July 2015

Description

The transceiver enabling times for the High-Speed CAN transceiver (P_10.3.27) and LIN transceiver (P_11.3.27) can be longer than specified.

If a CAN or LIN frame is transmitted or received before the transceiver is enabled, then the first frame could be lost.

Parameters specified in datasheet Rev 1.1:

CAN Transceiver Enabling Time	$t_{CAN,EN}$	–	10	–	µs	4) CSN = HIGH to first valid transmitted TXD dominant	P_10.3.27

4) Not subject to production test, tolerance defined by internal oscillator tolerance;

LIN Transceiver Enabling Time	$t_{LIN,EN}$	–	10	–	µs	2) CSN = HIGH to first valid transmitted TXD dominant	P_11.3.27

2) Not subject to production test, tolerance defined by internal oscillator tolerance

Figure 1 Transceiver Enabling Times as Specified in the Datasheet Rev 1.1

Actual transceiver enabling times:

CAN Transceiver Enabling Time	$t_{CAN,EN}$	8	13	18	µs	4)CSN = HIGH to first valid transmitted TXD dominant	P_10.3.27

4) Not subject to production test, tolerance defined by internal oscillator tolerance;

LIN Transceiver Enabling Time	$t_{LIN,EN}$	8	13	18	µs	2)CSN = HIGH to first valid transmitted TXD dominant	P_11.3.27

2) Not subject to production test, tolerance defined by internal oscillator tolerance

Figure 2 New Specified Transceiver Enabling Times

Workaround

In the rare case that a CAN or LIN frame needs to be sent shortly after the CAN or LIN transceiver is enabled, the above described enabling time shall be considered in the software.

Planned Fixes

New specified times will be updated in next revision of the Data Sheet.

2 Configuration Select Filter Time Can be Longer than Specified

Note: This behavior was already communicated via the EPN "TLE9260_63QX-EPN-100-Infineon" in July 2015

Description

The configuration select filter time (P_13.2.6) to determine the watchdog failure behavior and the VCC1 over-voltage detection behavior can be longer than specified.

Parameters specified in datasheet Rev 1.1:

Config Select Filter Time	t_{CFG_F}	–	7	–	µs	2)	P_13.2.6

2) Not subject to production test, tolerance defined by internal oscillator tolerance

Figure 3 Configuration Select Filter Time as Specified in the Datasheet Rev 1.1

New specified transceiver enabling time:

Config Select Filter Time	t_{CFG_F}	5	10	14	µs	2)	P_13.2.6

2) Not subject to production test, tolerance defined by internal oscillator tolerance

Figure 4 New Specified Configuration Select Filter Time

Impact

There is no impact on the application, i.e. no workaround is required. The actual filter time is ensuring a proper filtering of the signal at pin INT during SBC Init Mode.

Planned Fixes

New specified times will be updated in next revision of the Data Sheet.

3 Min. Dominant Time for CAN Bus Wake-Up Can be Longer than Specified

Description

The minimum dominant time for a CAN Bus wake-up (P_10.3.28) can be longer than specified.

Parameters specified in datasheet Rev 1.1:

Min. Dominant Time for Bus Wake-up	t_{Wake1}	0.50	–	3	µs	-12V ≤ V_{CM}(CAN) ≤ +12 V; CAN Wake capable Mode	P_10.3.28

Figure 5 Min. Dominant Time for CAN Bus wake-up as Specified in the Datasheet Rev 1.1

New specified transceiver enabling timing:

Min. Dominant Time for Bus Wake-up	t_{Wake1}	0.50	–	5	µs	-12V ≤ V_{CM}(CAN) ≤ +12 V; CAN Wake capable Mode	P_10.3.28

Figure 6 New Specified Min. Dominant Time for CAN Bus wake-up

Impact

The device might not wake up for min. dominant time <5us, i.e. to ensure a proper wake-up the min. dominant times must be >5us.

Note: The CAN specification in the ISO 11898-5 (1st Ed. 2007) requires a max. value of 5µs. Hence the CAN conformance of this parameter is still ensured.

Planned Fixes

New timings will be updated in next revision of the Data Sheet.

4 Possible POR Trigger during SBC Sleep Mode Entry

4.1 Description of Behavior

Occurrence:

While trying to enter SBC Sleep Mode an unexpected POR (power on reset of the device) could be triggered under following conditions:

- Only the WKx pins and/or LIN are activated as wake-up sources and
- VCC1 is slowly discharged (a typical discharge slew rate of ~0.2V/ms or slower) and VCC1 is crossing the range between 0.7V...0.5V

The behavior will not occur if any of the following conditions is fulfilled:

- if other additional wake-up sources are activated, e.g. CAN in SBC Sleep Mode
- if other peripherals, e.g. VCC2 or cyclic sense are enabled during SBC Sleep Mode
- if VCC1 is discharged faster (factor >10, i.e. >2V/ms)
- if SBC Sleep Mode is not used in the application

Impact:

SBC Sleep Mode will not be entered. Instead the device will start up in SBC Init Mode and the SBC has to be initialized again to its previous configuration.

Root Cause Description:

If the VCC1 voltage crosses the range between 0.7V...0.5V then a cross-current can be generated in the digital I/O pad structures of the device.
The generated cross-current is causing a load jump on the internal 1.5V voltage supply.
This load jump is inducing a disturbance on the internal supply, which can cause an unintended trigger of the POR, forcing the device to SBC Init Mode.

Note: This can only occur if the internal 1.5V voltage supply is in a low-load condition in SBC Sleep Mode where it is more sensitive to external disturbances

As mentioned above, a POR trigger can be avoided by means of:

- adding an additional load on the internal 1.5V supply (the low-load condition is prevented) or
- crossing the VCC1 voltage between 0.7V...0.5V faster, i.e. a faster discharge of VCC1 is achieved

Possible workarounds are described in **Chapter 4.2**.

4.2 Possible Workarounds

Possible workarounds to avoid an unexpected POR trigger when entering SBC Sleep Mode are listed below. Depending on the boundary conditions of the application and partitioning, a suitable workaround can be selected.

Workaround 1: Activation of CAN wake capability configuration

Set the CAN to wake capable before entering SBC Sleep Mode. It is recommended to enter SBC Sleep Mode within $t_{Silence}$ (typ. 1s) because the additional load on the internal 1.5V supply is typ. ~15uA during this time making the internal supply very stable.

Impact: Average current consumption adder during SBC Sleep Mode is typ. 4.5uA @25°C. In case of traffic on the CAN bus, the device and thus the application would be woken due to the CAN wake capability.

Workaround 2: Activation of Cyclic Sense of unused HS switch

Activate the cyclic sense feature by assigning an unused HS switch. The cyclic sense function will operate even without assigning a WK input and even leaving the respective HS switch unconnected.

It is recommended to choose the longest on-time (i.e. 20ms) to have the max. load (~80uA) on the internal supply when entering SBC Sleep Mode (Note: the SBC Sleep Mode command should be sent right after the cyclic sense is activated). To reduce the average current consumption, the longest period should be configured.

Impact: Average current consumption adder during SBC Sleep Mode is typ. 20uA @25°C.

Note: The HS needn't to be connected to WKx or other circuitries for this workaround. Care should be taken in the software to properly handle open load detection and to avoid supply under- or overvoltage shutdown.

Workaround 3: Activation of VCC2 in SBC Sleep Mode & activation of automatic pull-up/down of WK1…3

VCC2 and the pull-up / down source of WK1...3 are active during SBC Sleep Mode making the internal 1.5V supply more stable.

Impact: Average current consumption adder during SBC Sleep Mode is typ. 25...30uA @25°C.

Workaround 4: Addition of a pull-down structure on VCC1

A pull-down structure is added on VCC1 with a value of <250Ω to ensure a fast discharge time during SBC Sleep Mode entry (Assumption: the capacitor value on VCC1 is in the range of 470nF...4.7uF).

Note: Also an active load could be added, which would only be active during SBC Sleep Mode entry. Alternatively, it could be also sufficient if the microcontroller (due to configured pull-down structures or similar circuitries) or other loads are discharging VCC1 sufficiently despite a VCC1 undervoltage reset.

Impact: >20mA additional current consumption when VCC1 is enabled. The SBC Sleep Mode current consumption stays unchanged.

Possible POR Trigger during SBC Sleep Mode Entry

Workaround 5: Activation of a HS switch or FOx output in SBC Sleep Mode

Activate an unused HS switch or FOx output for SBC Sleep Mode to add a load on the internal 1.5V supply voltage.

Impact: Current consumption adder during SBC Sleep Mode is typ. 525uA (one HS switch enabled) and typ. 300uA (one FO output enabled) respectively.

Other workarounds or combination of workarounds might also be possible and could be checked for the application.

5 Unexpected VCC1 Overvoltage Reset in SBC Stop Mode after a Double Load Jump when the SPI bit 'VCC1_OV_RST' is set

As stated in the datasheet, it is not recommended to set the SPI bit 'VCC1_OV_RST' in SBC Stop Mode to avoid unintentional SBC Restart- or Fail-Safe Mode entries due to external noise as the regulator is more sensitive to overvoltage in this low-load condition. In any case the software concept should include a robust handling of the VCC1 overvoltage detection.

However, if the bit 'VCC1_OV_RST' is set during SBC Stop Mode despite above mentioned arguments, then the below described behavior and hints could apply.

5.1 Description of Behavior

Occurrence:

- While the device is in SBC Stop Mode a sporadic VCC1 overvoltage reset could be observed erroneously although the VCC1 voltage does not cross the overvoltage threshold
- After the low-power mode is entered in SBC Stop Mode only the low-current mode (LCM) regulator is active. The reset could occur after a double load jump, e.g. a periodic wake-up event
- The device signals the erroneously detected VCC1 overvoltage condition via the SPI bit 'VCC1_OV'
- Necessary conditions:
  - the SPI bit 'VCC1_OV_RST' must be set and
  - the device must be in SBC Stop Mode and
  - a load step (external disturbance) must occur on VCC1 or VCC2 in a certain timing window after the low-current mode regulator has been activated, i.e. the load current has fallen below the threshold $I_{VCC,Ipeak,f}$ and
  - no HSx switch is turned on during this load step

Impact:

SBC Stop Mode will be left unintentionally. The device will enter SBC Normal Mode via SBC Restart Mode and the SBC has to be brought to SBC Stop Mode again.

Proposals to avoid this behavior are described in **Chapter 5.2**.

5.2 How to Avoid an Unintentional VCC1 Overvoltage Reset in SBC Stop Mode?

Proposals to avoid an unintended VCC1 overvoltage reset during SBC Stop Mode are listed below.

Other solutions might be also possible and could be checked for the application.

Clearing the SPI bit 'VCC1_OV_RST' before entering SBC Stop Mode

Clearing the SPI bit 'VCC1_OV_RST' before entering SBC Stop Mode will prevent an unintended VCC1 overvoltage reset. In this case only the SPI bit 'VCC1_OV' will be set in case of a VCC1 over-voltage detection. 'VCC1_OV_RST' can be set again when returning to SBC Normal Mode.

Impact: VCC1 overvoltage reset is not available during SBC Stop Mode

General hint regarding VCC1 overvoltage handling

A "robust" software strategy, e.g. filtering concept, is recommended in general on handling VCC1 overvoltage resets and the respective SPI bit 'VCC1_OV'. For example, depending on the loads a VCC1 overvoltage event could be also generated due to a temporary EMC conditions because the regulator is naturally more sensitive to external disturbances in a low-load condition.

6 Application Hints

6.1 Handling the FO3/TEST Pin during Software Debugging or End-of-Line Programming

Description:

For software debugging or end-of-line programming of the ECU it is possible to enter SBC Development Mode to stop the integrated watchdog and to prevent a reset due to watchdog trigger failure. SBC Development Mode is activated by pulling down the FO3/TEST pin during device power-up.
To avoid device damage it is mandatory to ensure the absolute maximum ratings of the FO3/TEST pin as shown in below figure

Fail Pins FO2, FO3/TEST	$V_{FO2\_3,\ max}$	-0.3	–	V_S + 0.3	V	–	P_4.1.23

Figure 7 Absolute Maximum Ratings for the FO3/TEST Pin

Failure in observing the maximum ratings could result in serious device damage, e.g. due to unprotected handling (ESD risks) or due to a long wire harness of the debugging or programming connector with capacitances in the debugger / programmer.

FO3/TEST Pin Application Hint:

In order to avoid device damage during debugging or programming of the ECU, it is recommended to handle the ECU in a “controlled” production environment to ensure the maximum ratings.
If this cannot be ensured, e.g. during software debugging in the development phase then a series resistor between FO3/TEST pin and the connector (see **Figure 8**) is recommended to limit the current into or out of the pin.

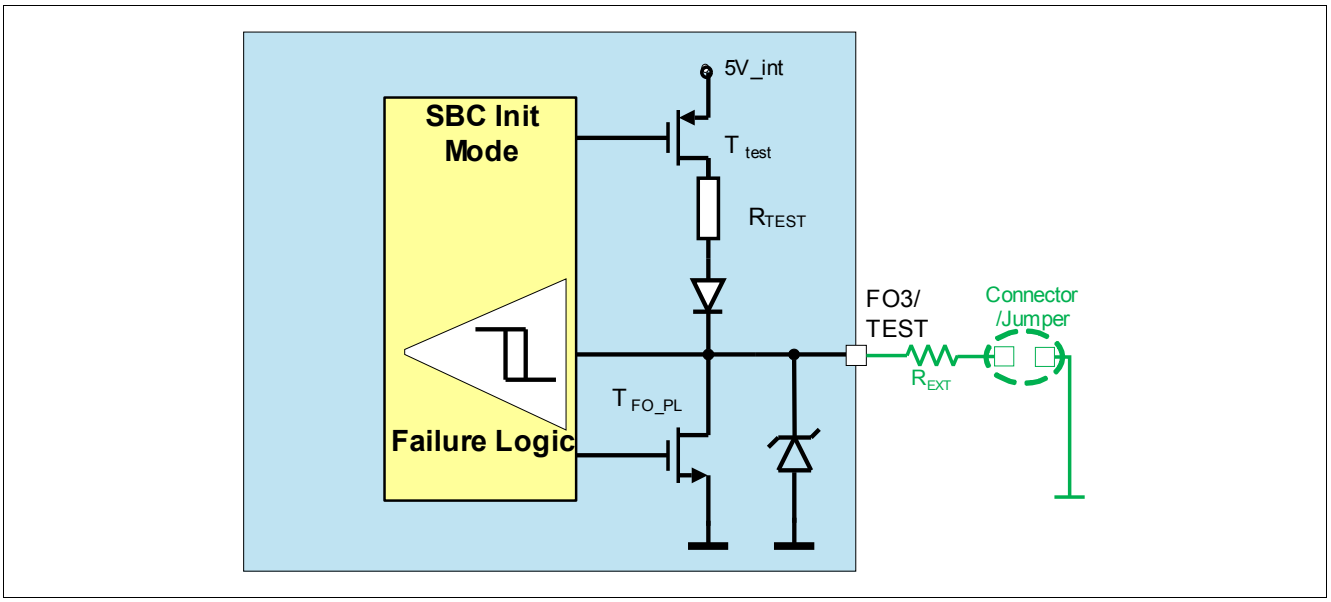

Figure 8 Absolute Maximum Ratings for the FO3/TEST Pin

Application Hints

A low level at the FO3/TEST pin must be ensured for a safe entry of the SBC Development Mode during the device power-up phase

GPIO input threshold voltage	$V_{GPIOI,th}$	1.5	2.5	3.5	V	[6] hysteresis included	P_14.2.11

Figure 9 Absolute Maximum Ratings for the FO3/TEST Pin

The value of the series resistor can be calculated by taking the minimum value of the internal pull-up resistor (P_14.2.5) and the minimum threshold value of FO3/TEST:

$$\frac{R_{EXT}}{2.5\ k\Omega\ + R_{EXT}} \cdot (5V - 0.7V) < 1.5V$$

Figure 10 Calculation of the external series resistor value to ensure a low-level on FO3/TEST

A low-level on FO3/TEST can be achieved for resistor values of $R_{EXT} < 1.3k\Omega$. To ensure a safety margin **resistor values of $100\Omega < R_{EXT} < 470\Omega$ are recommended**.

6.2 Possible Ripple on VCC1 After a Load Jump

Occurrence:

Under certain conditions (described below) a small ripple of ~30mV (peak-peak) can be observed on the VCC1 after a load jump in SBC Init-, Normal-, and Restart Mode (example shown in **Figure 11**).

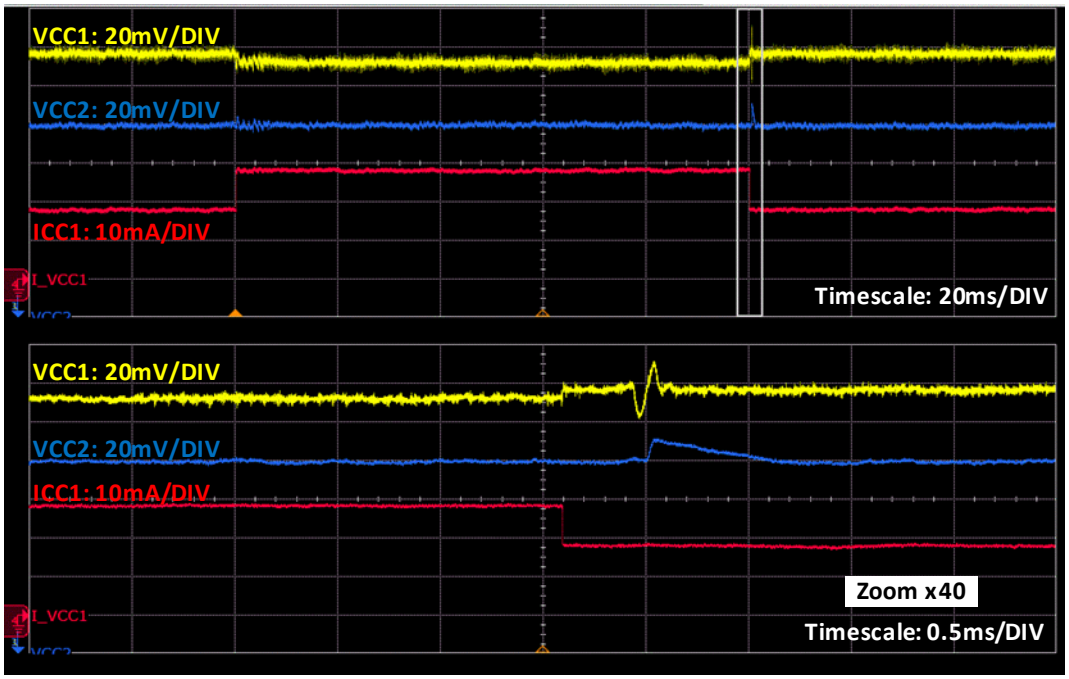

Figure 11 Example Oscilloscope Plot Showing the Ripple on the VCC1 Output after a load Jump

Impact:

The described ripple on VCC1 is not violating any electrical parameter, i.e. the output voltage is not exceeding the specified +/-2% tolerance. However, the unexpected behavior could disturb voltage measurements, e.g. when VCC1 is used as a ADC reference voltage or during end-of-line voltage calibration.

Root Cause Description:

- The ripple on VCC1 is caused by the switching of the active peak comparator in SBC Init-, Normal-, and Restart Mode. The comparator is used in SBC Stop Mode to switch the regulator from high-current mode (HCM) to low-current mode (LCM) and vice versa. However, the comparator is also enabled in SBC Init-, Normal-, and Restart Mode and will switch when crossing higher (~20mA) load currents (Note: the comparator switching has no functionality in these SBC modes).
- the ripple will only occur at the falling edge of the load jump, i.e. when the load current is falling below the ~20mA range,
- the switching of the active peak comparator applies a load jump on the internal 5V supply and thus a disturbance on it. The voltage regulator reference is derived from the internal 5V supply and therefore this disturbance from the internal 5V supply induces also ripple on the reference voltage which in return causes the ripple on VCC1.

Application Hints

Potential Workarounds:

Possible workarounds to avoid an unintended ripple on VCC1 are listed below. The solution is to load the internal 5V supply making it considerably less sensitive to disturbances (e.g. load jumps) and thus minimizing the ripple on VCC1.
Depending on the boundary conditions of the application and partitioning, a suitable workaround can be selected:

Workaround 1: Enabling the LIN will stabilize the internal 5V supply and reduce the ripple on the VCC1 output voltage to a minimum.

Note: This workaround is only available on the TLE9262(-3)QX(V33) or TLE9263(-3)QX(V33) variants.

Workaround 2: Enabling the low-side switch function (GPIO functionality) of FO2 or FO3 will also stabilize the internal 5V supply. Set the GPIOs to '110' in GPIO_CTRL.

Note: The pin must not be connected to any other circuitries for this workaround. No failure flag will be set.

Workaround 3: Depending on the load jump the ripple can be avoided when the higher active peak threshold $I_{VCC1,Ipeak2}$ is selected via SPI (I_PEAK_TH = 1). In this case the ripple will occur only at a load current of factor two (~40mA range). If required for quiescent current reasons, the lower active peak threshold should be selected when entering SBC Stop Mode.

Other workarounds or combination of workarounds might also be possible and could be checked for the application.

Edition 2016-06-24
Published by
Infineon Technologies AG
81726 Munich, Germany

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