5 V low dropout voltage regulator

Features

- Ultra low current consumption 20 µA
- Output voltage 5 V ±2%
- Output current up to 300 mA
- Very low dropout voltage
- Stable with ceramic output capacitor of 470 nF
- Output current limitation
- Overtemperature shutdown
- Wide temperature range from -40°C up to 150°C
- Green Product (RoHS-compliant)

RoHS

AEC Qualified

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications.

Product validation according to AEC-Q100.

Description

The OPTIREG™ linear TLE7274-2D is a monolithic integrated low dropout voltage regulator for load currents up to 300 mA. An input voltage up to 42 V is regulated to $V_{Q,nom}$ = 5.0 V with a precision of ±2%. The sophisticated design allows to achieve stable operation even with ceramic output capacitors down to 470 nF. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The OPTIREG™ linear TLE7274-2D can be also used in all other applications requiring a stabilized 5 V voltage. Due to its ultra low quiescent current of typically 20 µA the OPTIREG™ linear TLE7274-2D is dedicated for use in applications permanently connected to V_{BAT}. An integrated output sink current circuitry keeps the voltage at the output pin Q below 5.5 V even in case of occurring reverse currents. Thus connected devices are protected from overvoltage damage. For applications requiring extremely low noise levels the OPTIREG™ Infineon voltage regulator family TLE42XX and TLE44XX is more suited than the OPTIREG™ linear TLE7274-2D. A mV-range output noise on the TLE7274-2D caused by the charge pump operation is unavoidable due to the ultra low quiescent current concept.

Type	Package	Marking
TLE7274-2D	PG-TO252-3	7274-2D

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1 Block diagram

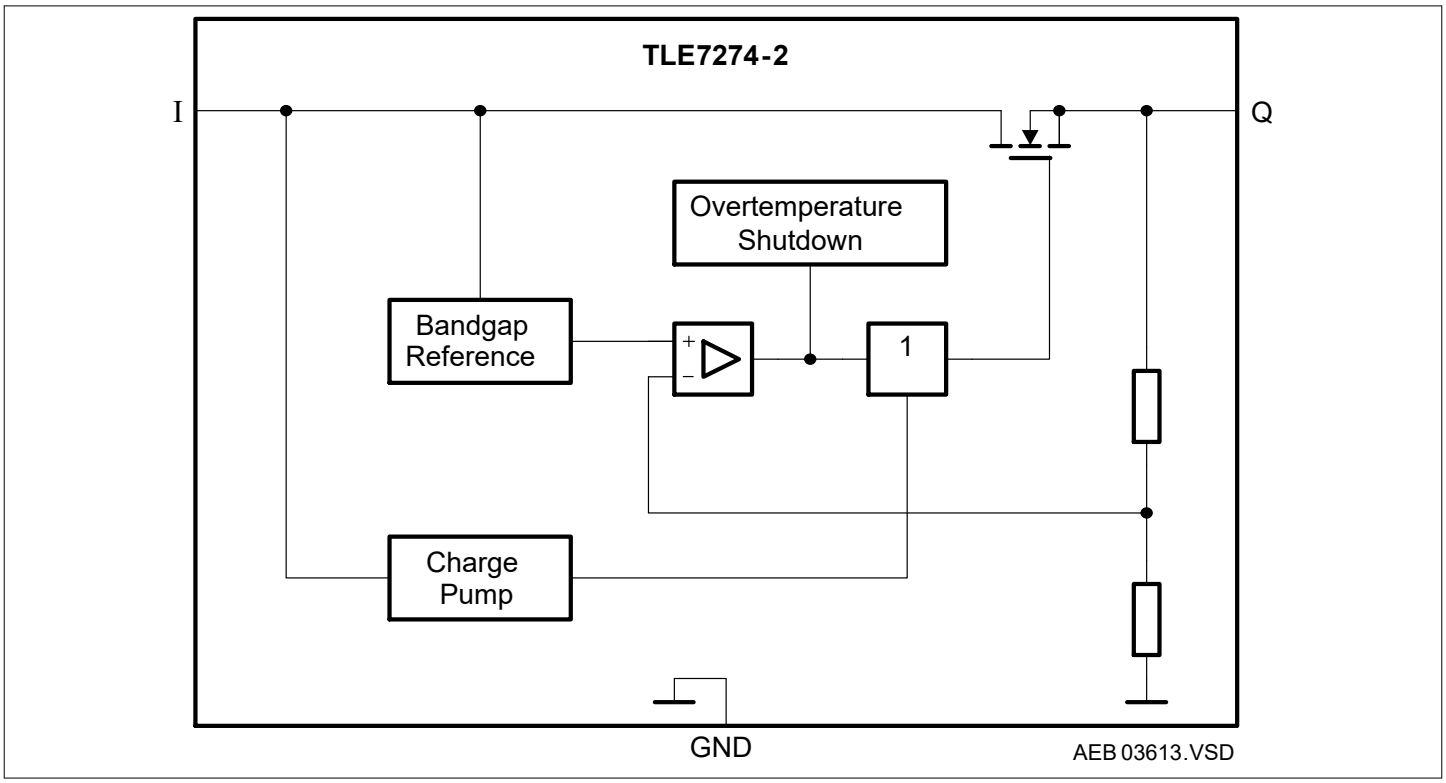


Figure 1 **Block diagram**

2 Pin configuration

2.1 Pin assignment PG-TO252-3

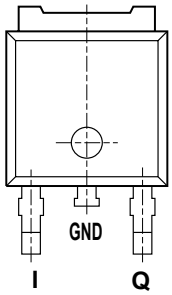


Figure 2 **Pin configuration (top view)**

2.2 Pin definitions and functions

Table 1 **Pin definitions and functions**

Pin no.	Symbol	Function
1	I	**Input** Block to ground directly at the IC with a ceramic capacitor
2	GND	**Ground** Internally connected to heat slug
3	Q	**Output** Block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in Functional range
Heat slug	–	**Heat slug** Internally connected to GND; connect to GND and heatsink area

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings [1)]

T_j = -40°C to 150°C; all voltages with respect to ground, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Voltage	V_I	-0.3	–	45	V	–	P_4.1.1
Output Q							
Voltage	V_Q	-0.3	–	6	V	–	P_4.1.2
Voltage	V_Q	-0.3	–	6.2	V	[2)] t < 10 s	P_4.1.3
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.4
Storage temperature	T_{stg}	-50	–	150	°C	–	P_4.1.5
ESD robustness							
ESD robustness all pins (HBM)	$V_{ESD,HBM}$	-3	–	3	kV	[3)]	P_4.1.6
ESD robustness all pins (CDM)	$V_{ESD,CDM}$	-1.5	–	1.5	kV	[4)]	P_4.1.7

1) Not subject to production test, specified by design.
2) Exposure to these absolute maximum ratings for extended periods (t > 10 s) may affect device reliability.
3) Human body model (HBM) robustness according to AEC-Q100-002 - JESD22-A114.
4) Charged device model (CDM) robustness according to ESDA STM5.3.1.

***Notes**:*

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	5.5	–	42	V	–	P_4.2.1
Output capacitor's requirements for stability	C_Q	470	–	–	nF	1)	P_4.2.2
Output capacitor's requirements for stability	ESR(C_Q)	–	–	10	Ω	2)	P_4.2.3
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
2) Relevant ESR value at f = 10 kHz.

***Note**: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*

3.3 Thermal resistance

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to* www.jedec.org.

Table 4 Thermal resistance 1)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	6	–	K/W	Measured to tab	P_4.3.1
Junction to ambient	R_{thJA}	–	32	–	K/W	2)	P_4.3.2
Junction to ambient	R_{thJA}	–	115	–	K/W	3) Footprint only	P_4.3.3
Junction to ambient	R_{thJA}	–	62	–	K/W	3) 300 mm² heatsink area	P_4.3.4
Junction to ambient	R_{thJA}	–	47	–	K/W	3) 600 mm² heatsink area	P_4.3.5

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip and package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70 µm Cu).

4 Electrical characteristics

4.1 Electrical characteristics voltage regulator

Table 5 Electrical characteristics voltage regulator

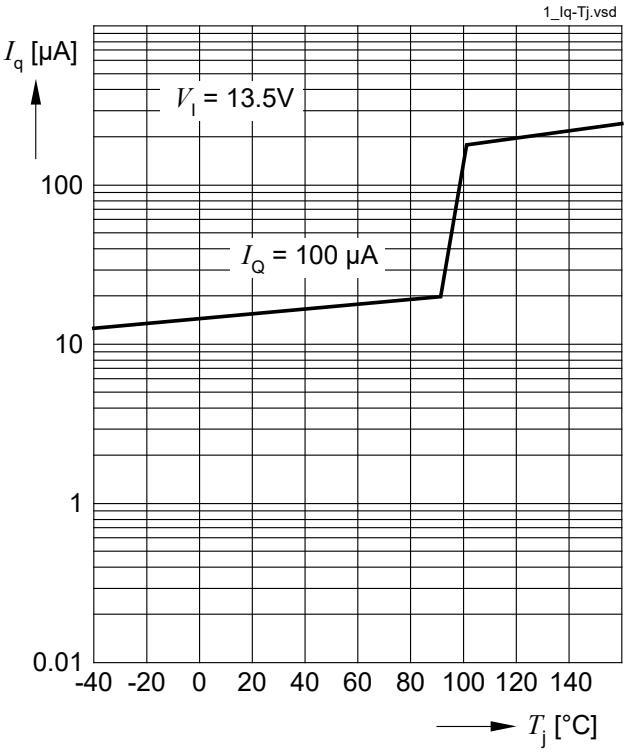
V_I = 13.5 V; -40°C < T_j < 150°C; all voltages with respect to ground, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Q							
Output voltage	V_Q	4.9	5.0	5.1	V	0.1 mA < I_Q< 300 mA; 6 V < V_I < 16 V	P_5.1.1
Output voltage	V_Q	4.9	5.0	5.1	V	0.1 mA < I_Q< 100 mA; 6 V < V_I < 40 V	P_5.1.2
Dropout voltage	V_{dr}	–	250	500	mV	I_Q = 200 mA; V_{dr} = V_I – V_Q	P_5.1.3
Load regulation	$\Delta V_{Q,lo}$	– 40	15	40	mV	I_Q = 5 mA to 250 mA	P_5.1.4
Line regulation	$\Delta V_{Q,li}$	– 20	5	20	mV	V_I = 10 V to 32 V; I_Q = 5 mA	P_5.1.5
Output current limitation	I_Q	301	–	–	mA	1)	P_5.1.6
Output current limitation	I_Q	–	–	800	mA	V_Q = 0 V	P_5.1.7
Power supply ripple rejection	*PSRR*	–	60	–	dB	2) f_r = 100 Hz; V_r = 0.5 V_{pp}	P_5.1.8
Temperature output voltage drift	$\Delta V_Q/\Delta T$	–	0.5	–	mV/K	–	P_5.1.9
Current consumption							
Quiescent current $I_q = I_I - I_Q$	I_q	–	20	30	µA	I_Q = 0.1 mA; T_j = 25°C	P_5.1.10
Quiescent current $I_q = I_I - I_Q$	I_q	–	–	40	µA	I_Q = 0.1 mA; T_j ≤ 80°C	P_5.1.11

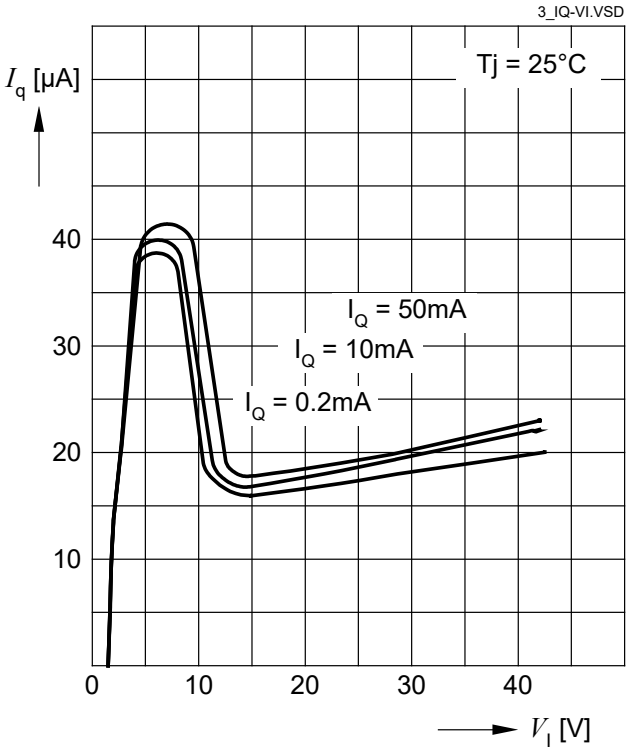
1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.
2) Not subject to production test, specified by design.

4.1.1 Typical performance characteristics

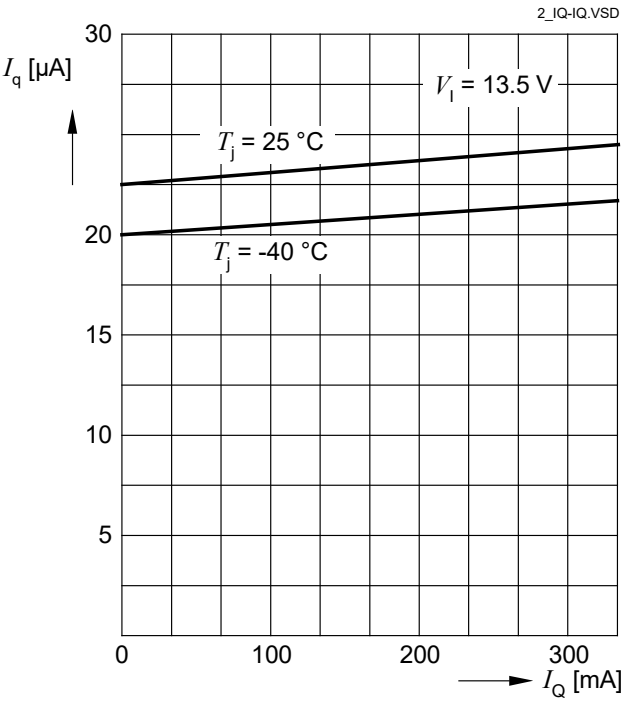
Current consumption I_q versus junction temperature T_j



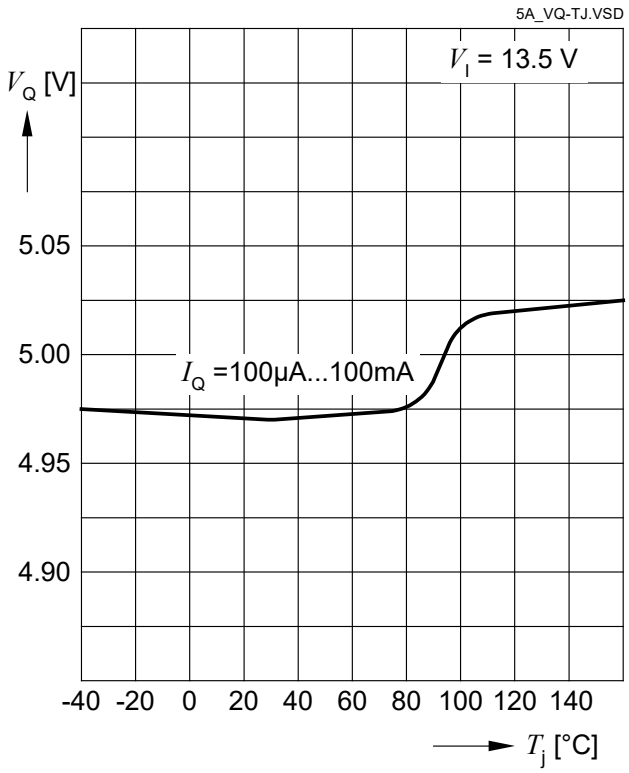
Current consumption I_q versus input voltage V_I



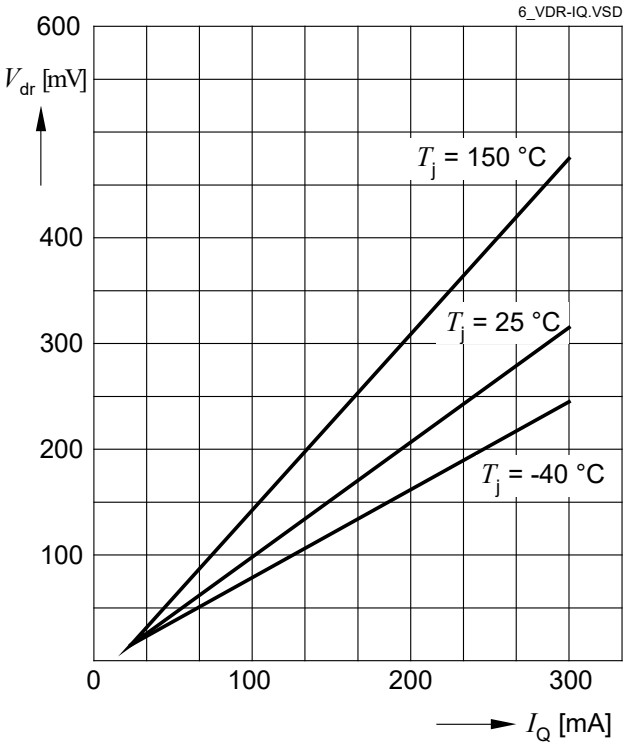
Current consumption I_q versus output current I_Q



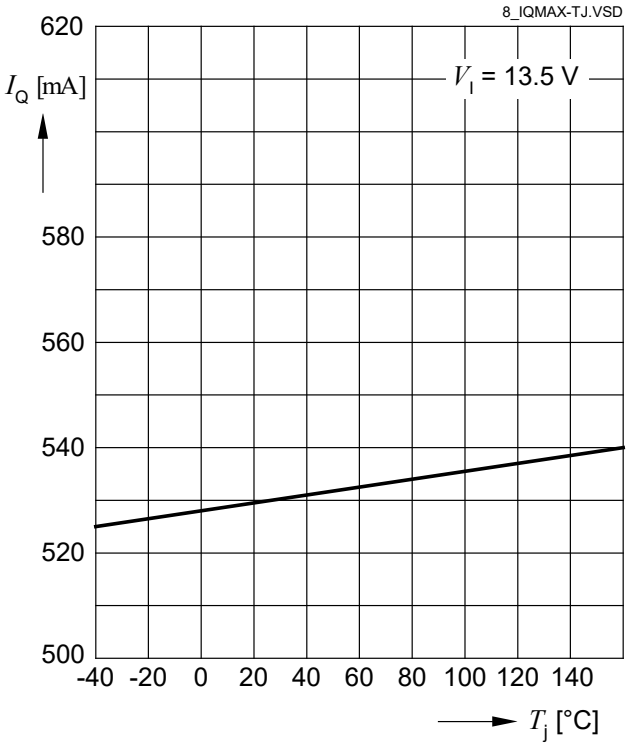
Output voltage V_Q versus junction temperature T_j



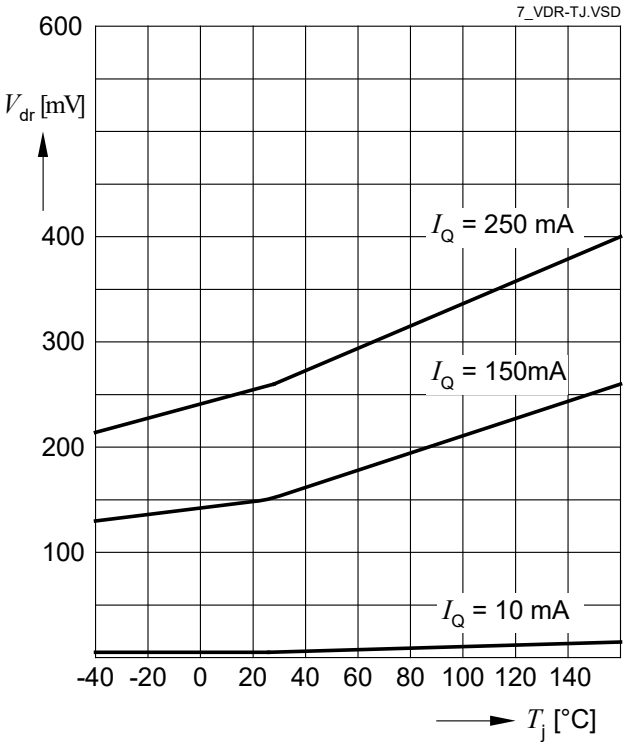
Dropout voltage V_{dr} versus output current I_Q



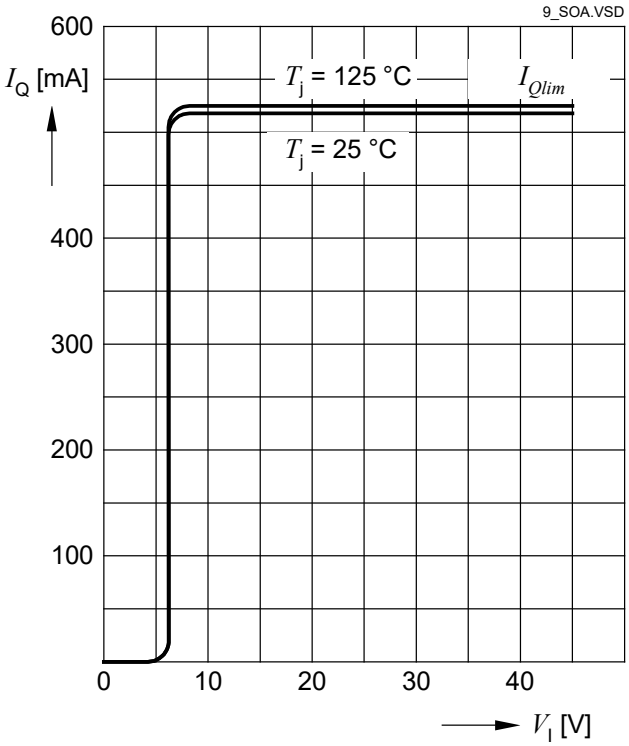
Maximum output current I_Q versus junction temperature T_j



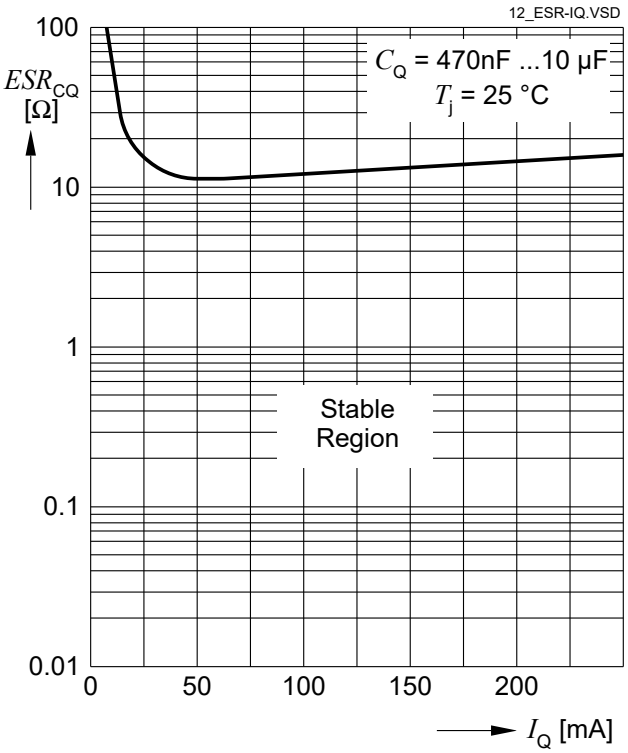
Dropout voltage V_{dr} versus junction temperature T_j



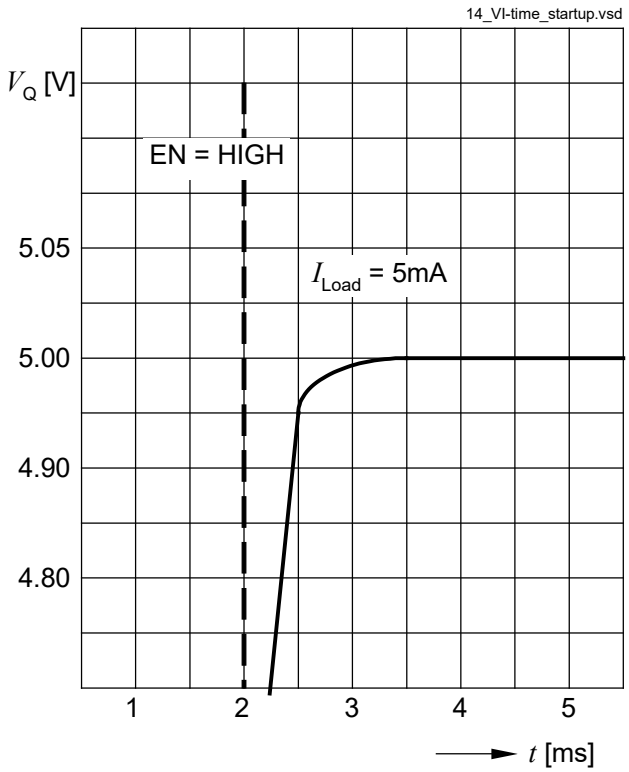
Maximum output current I_Q versus input voltage V_I



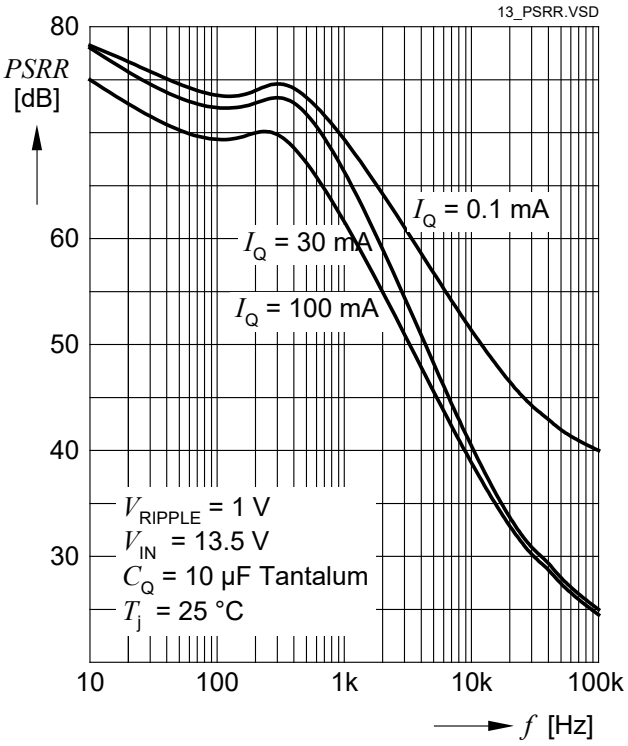
Region of stability



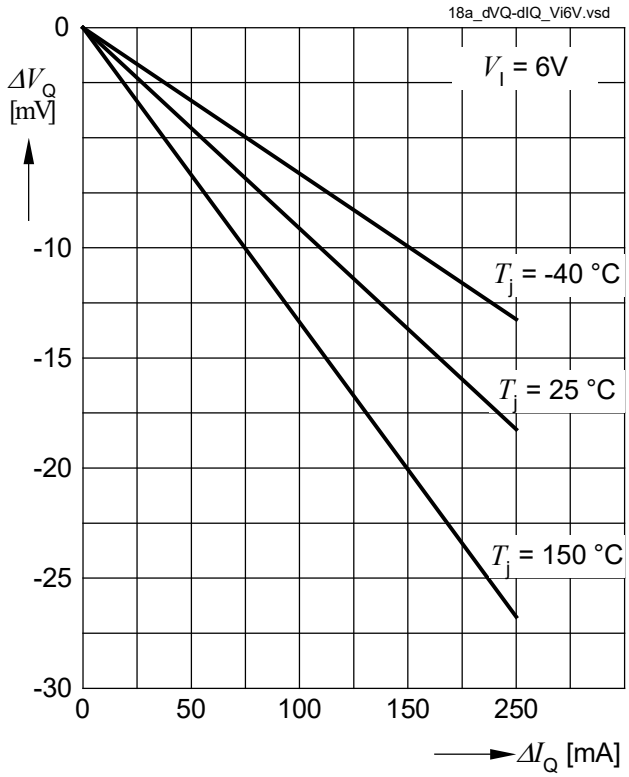
Output voltage V_Q start-up behavior



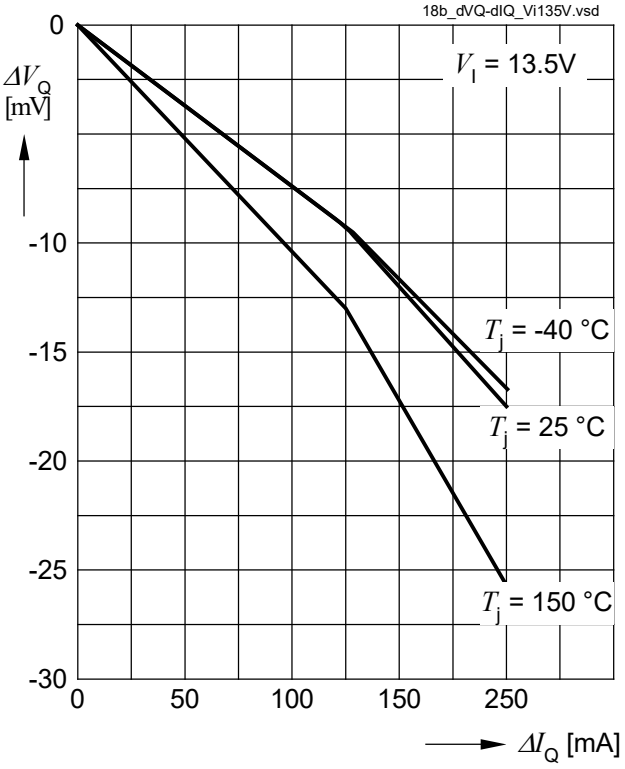
Power supply ripple rejection *PSRR* versus frequency *f*



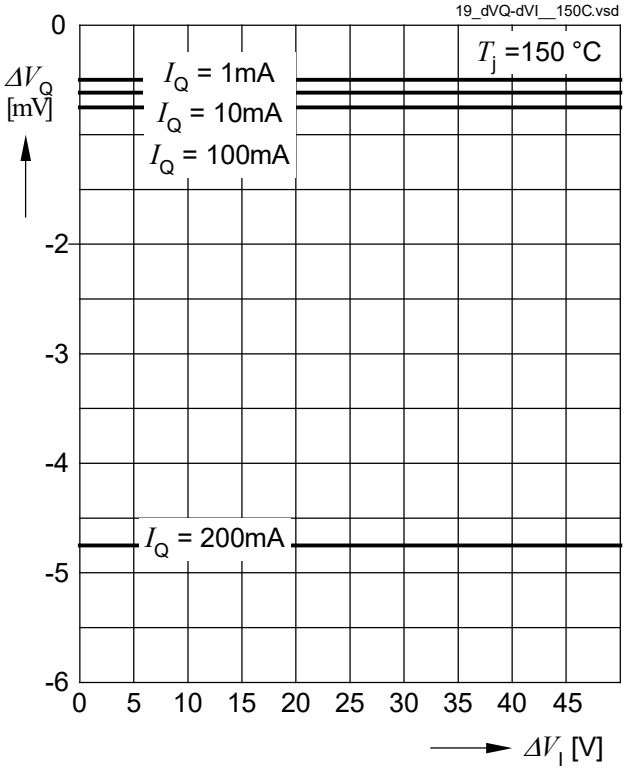
Load regulation ΔV_Q versus output current change ΔI_Q



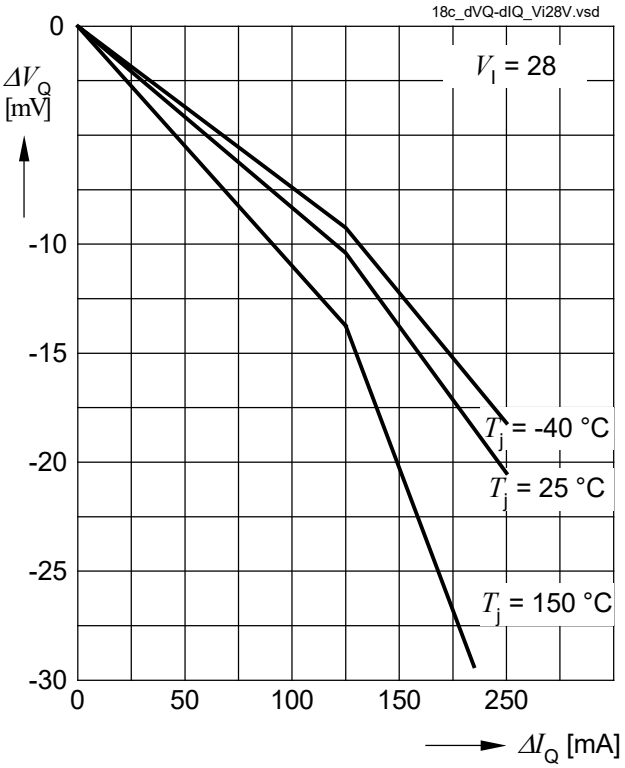
Load regulation ΔV_Q versus output current change ΔI_Q



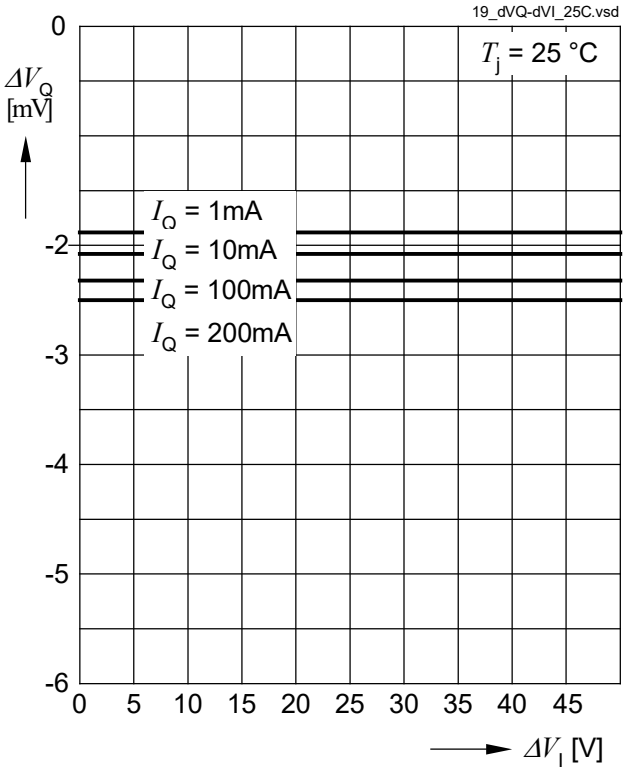
Line regulation ΔV_Q versus input voltage change ΔV_I



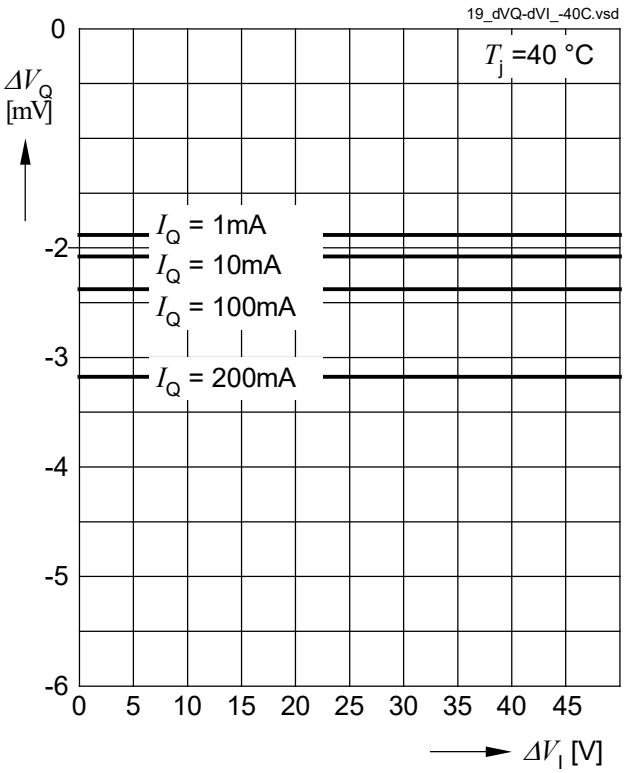
Load regulation ΔV_Q versus output current change ΔI_Q



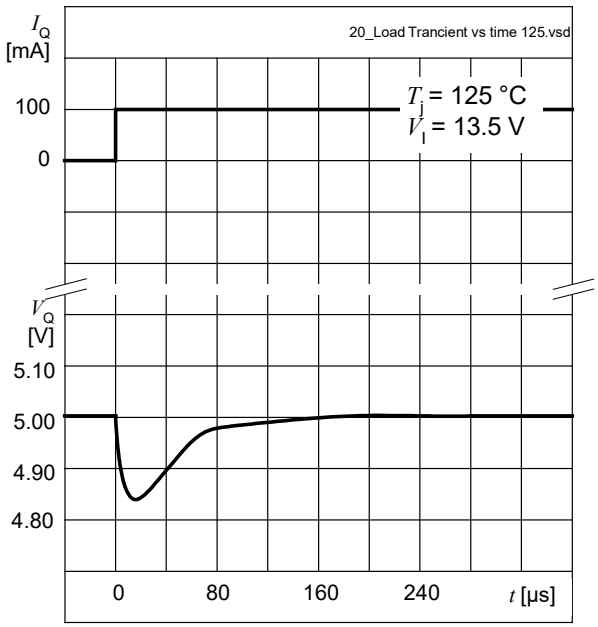
Line regulation ΔV_Q versus input voltage change ΔV_I



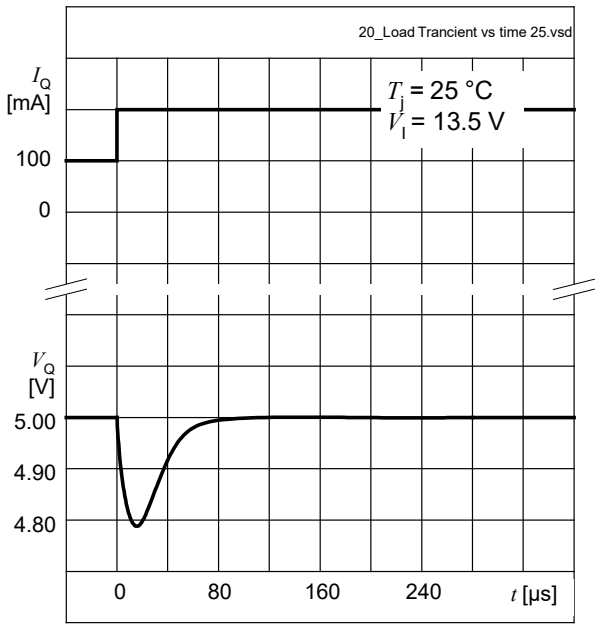
Line regulation ΔV_Q versus input voltage change ΔV_I



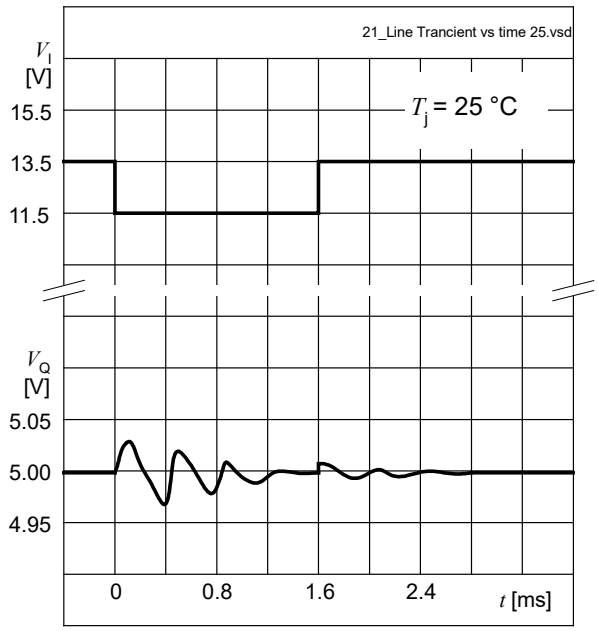
Load transient response peak voltage ΔV_Q



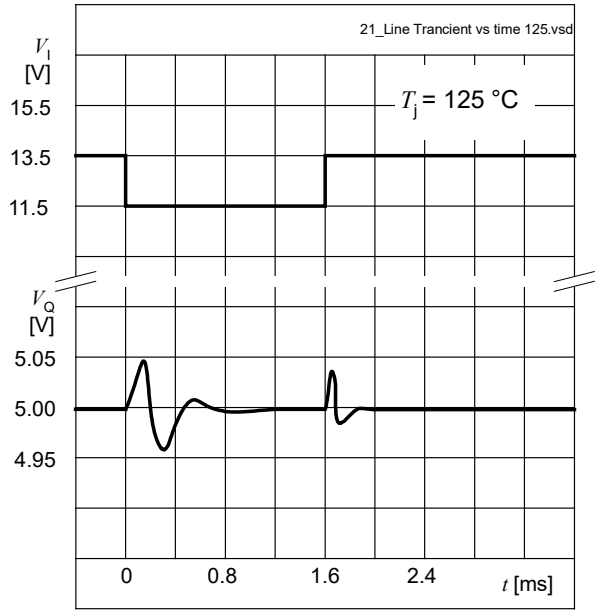
Load transient response peak voltage ΔV_Q



Line transient response peak voltage ΔV_Q



Line transient response peak voltage ΔV_Q



5 Package information

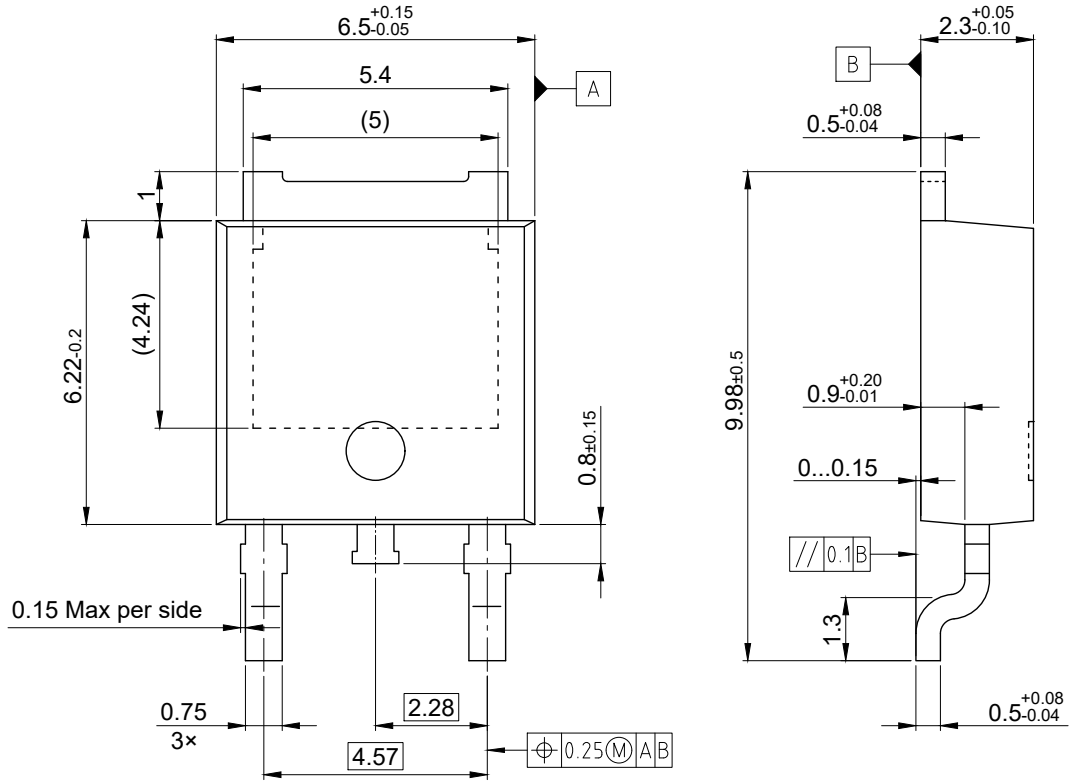


Figure 3 PG-TO252-3 package outline

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

6 Revision history

Version	Date	Changes
1.02	2024-11-14	Updated template, editorial changes Removed discontinued package options TLE7274-2G & TLE7274-2E
1.01	2011-11-30	Updated version data sheet: (no change in function or design of device) Package TO263-3 corrected to TO263-3-2. in “Overview” on Page 2 Package Drawing corrected. in “Pin Assignment PG-TO252-3, PG-TO263-3” on Page 11 Pin Assignment for TO263-3 corrected and Headlines added. in Figure 23 “PG-TO263-3” on Page 37 Package Outlines corrected In “Electrical Characteristics Voltage Regulator” on Page 19, former Item 5.1.12 “Current Consumption, Regulator Disabled” removed, in Condition of Item and Item “V_{EN} = 5 V” removed: Non relevant information as TLE7270-2 does not implement Enable Feature
1.00	2009-06-01	Initial version datasheet

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