Advanced Silicon Devices – Applications and Technology Trends

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Infineon

Content

- Silicon devices versus GaN devices: An unbiased view on key performance indicators
- Applications: Comparison of devices in hard-switching and resonant circuits
- Summary

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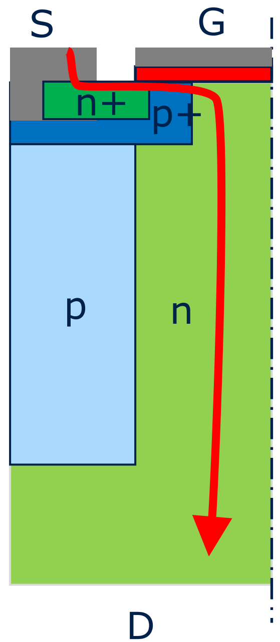
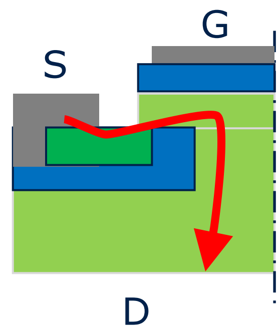
Comparing competing device concepts

Si
Superjunction



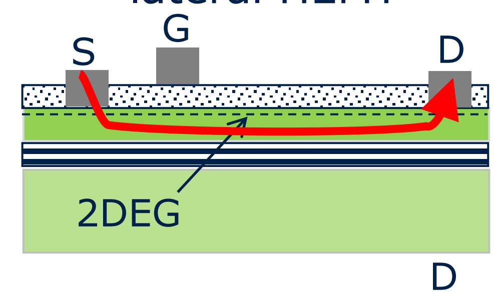
- $R_{ON}\times A$ scales with cell pitch
- Inherently fast switching
- dv/dt scales inversely with cell pitch
- Reverse recovery charge and snappyness of body diode as major drawbacks

SiC
vertical drift zone



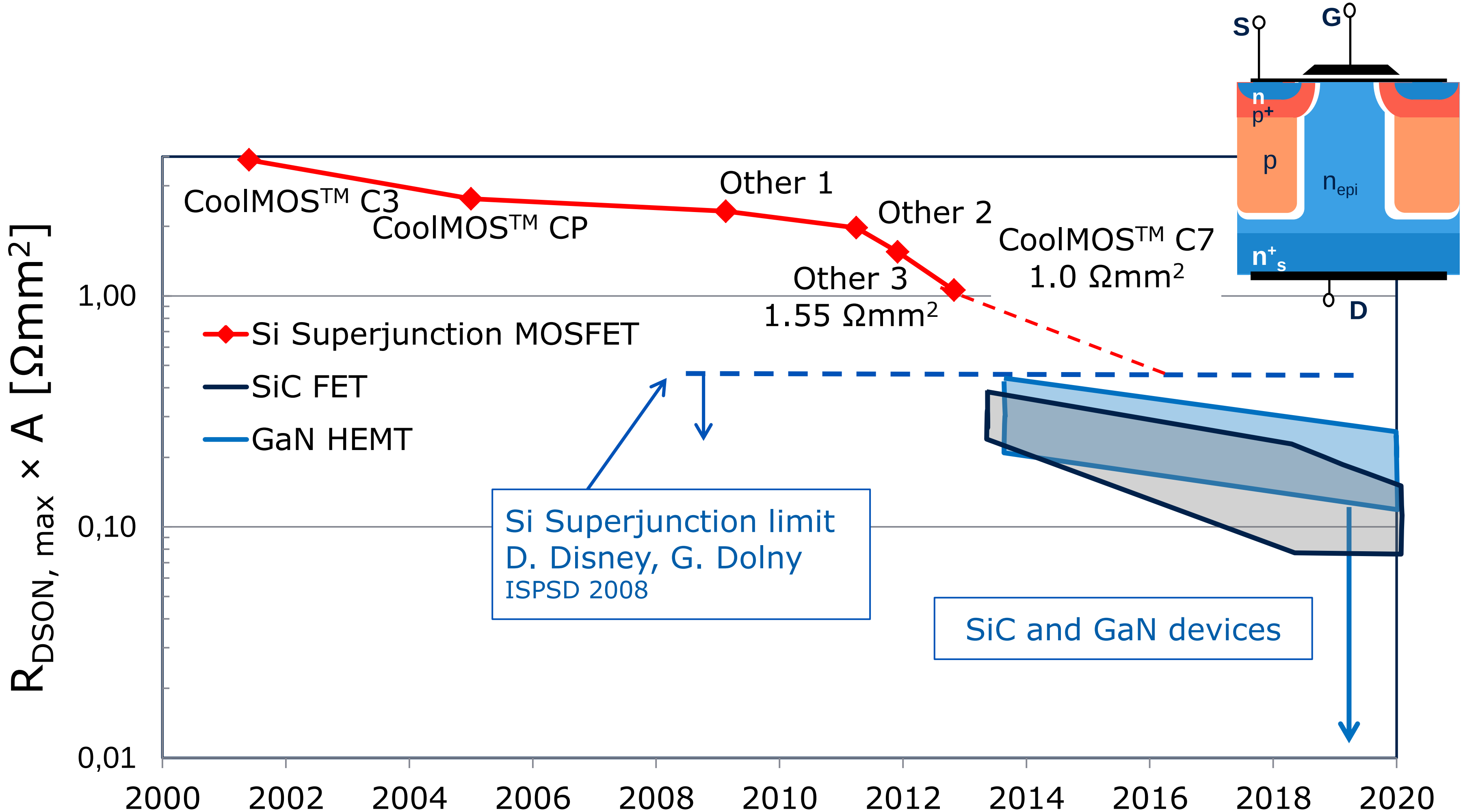
- Pitch influences $R_{ON}\times A$ by improved utillization of the semiconductor volume
- Normally-on; turns into normally-off by Cascode or direct-driven concept
- Good body diode; Q_{rr} close to SiC Schottky diodes

GaN
lateral HEMT



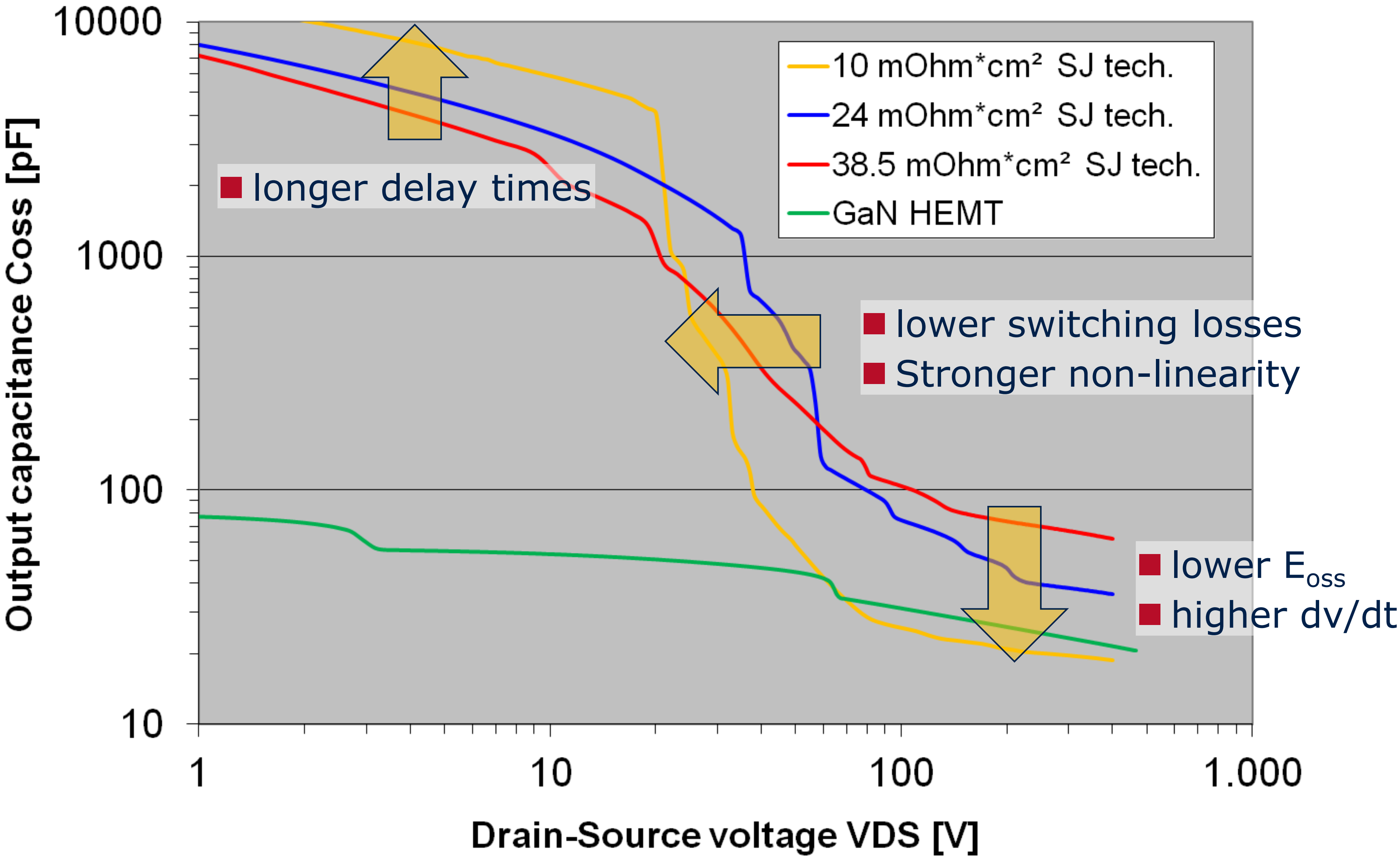
- Good starting point for low $R_{ON}\times A$ and Q_{OSS} due to high electron mobility
- Device capacitances are strongly influenced by the metal re-routing
- Excellent reverse behavior

How far can the Superjunction concept be exploited in terms of R_{DSon}*A?

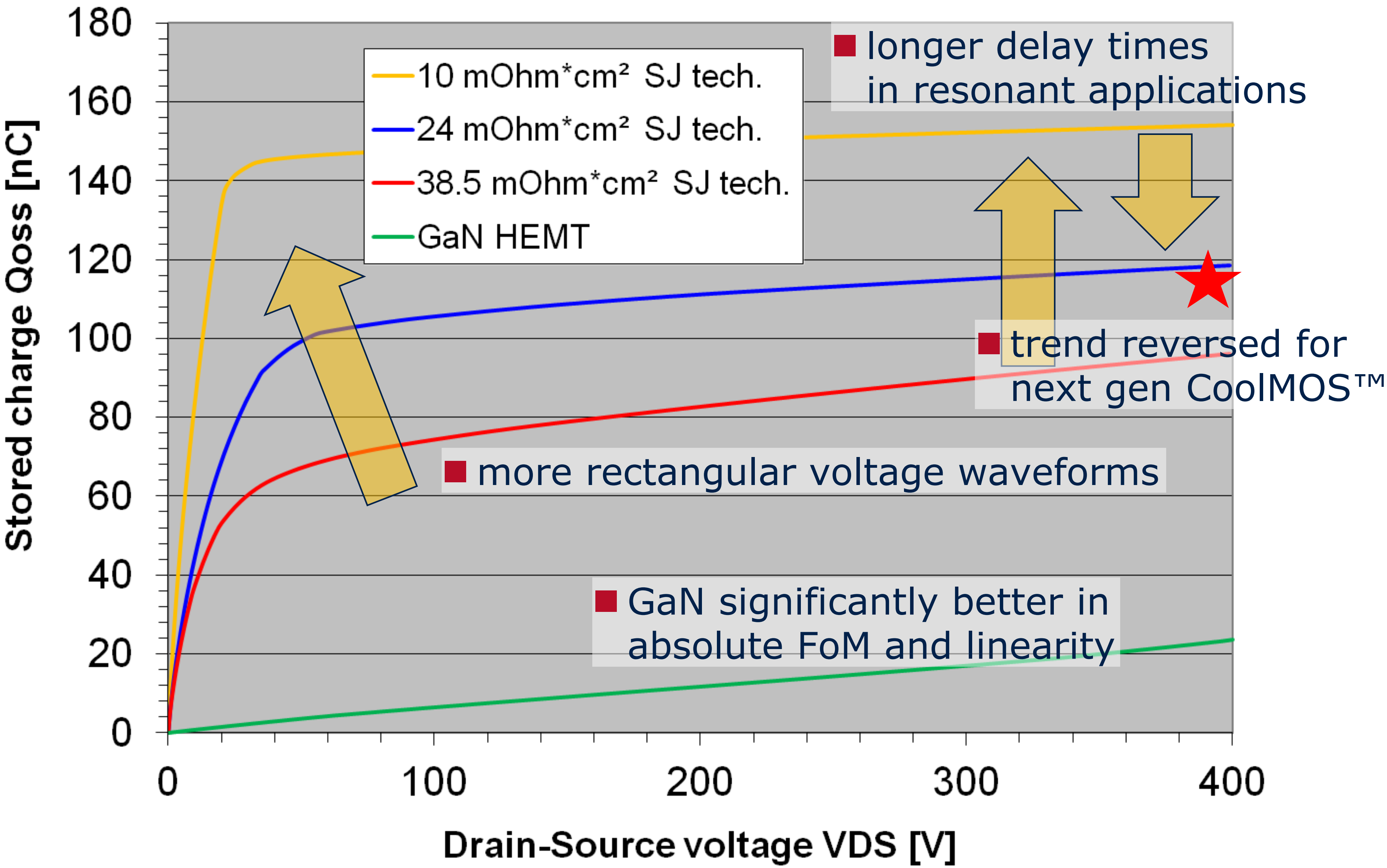


Still a long way until the limit is reached with Si Superjunction.
Si limit potentially lower than 0.5 Ωmm²

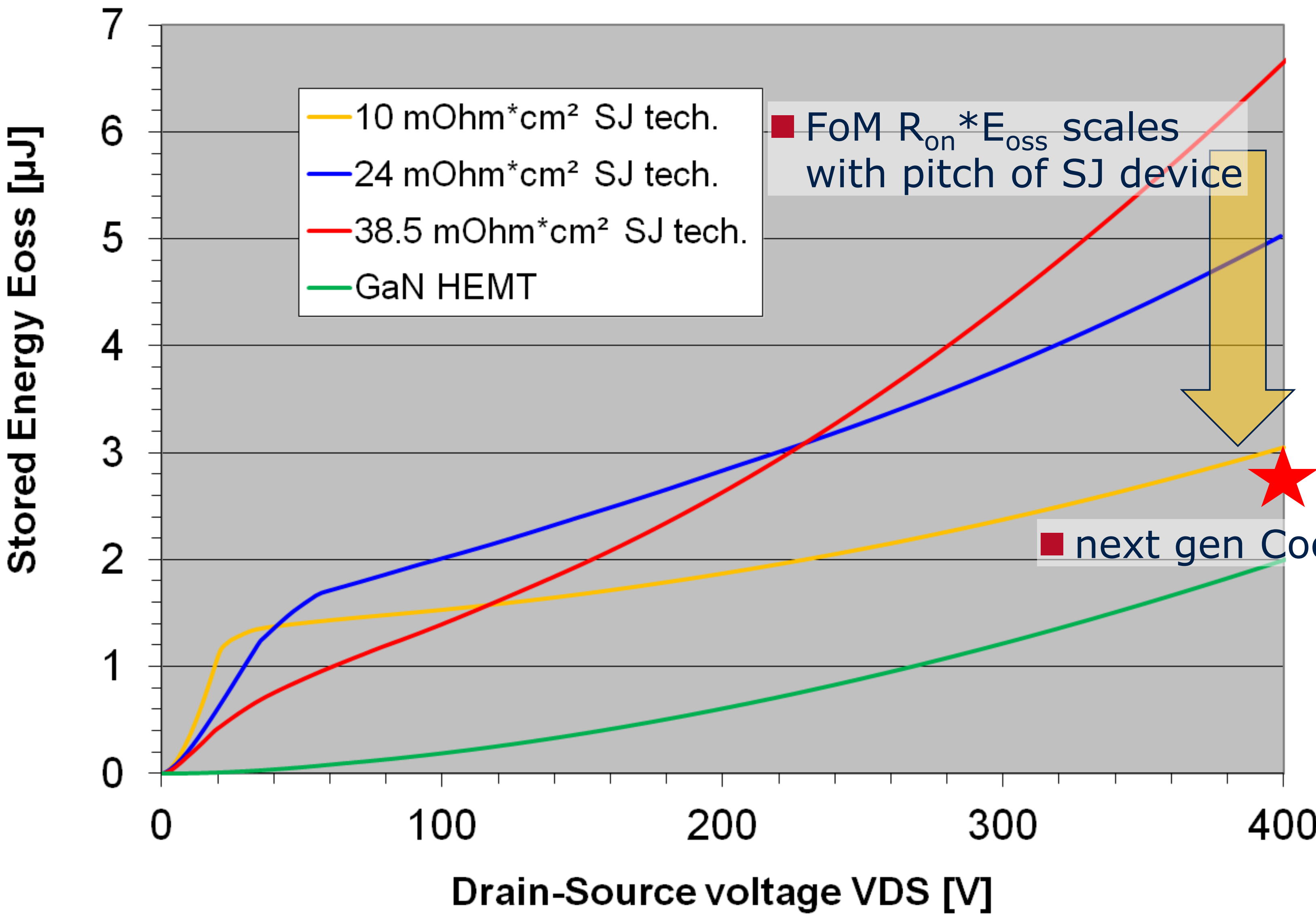
The output capacitance of SJ devices gets more non-linear with every generation! 190 mOhm, 600V / 650V devices



The Q_{oss} characteristic will become more and more flat! 190 mOhm, 600V / 650V devices

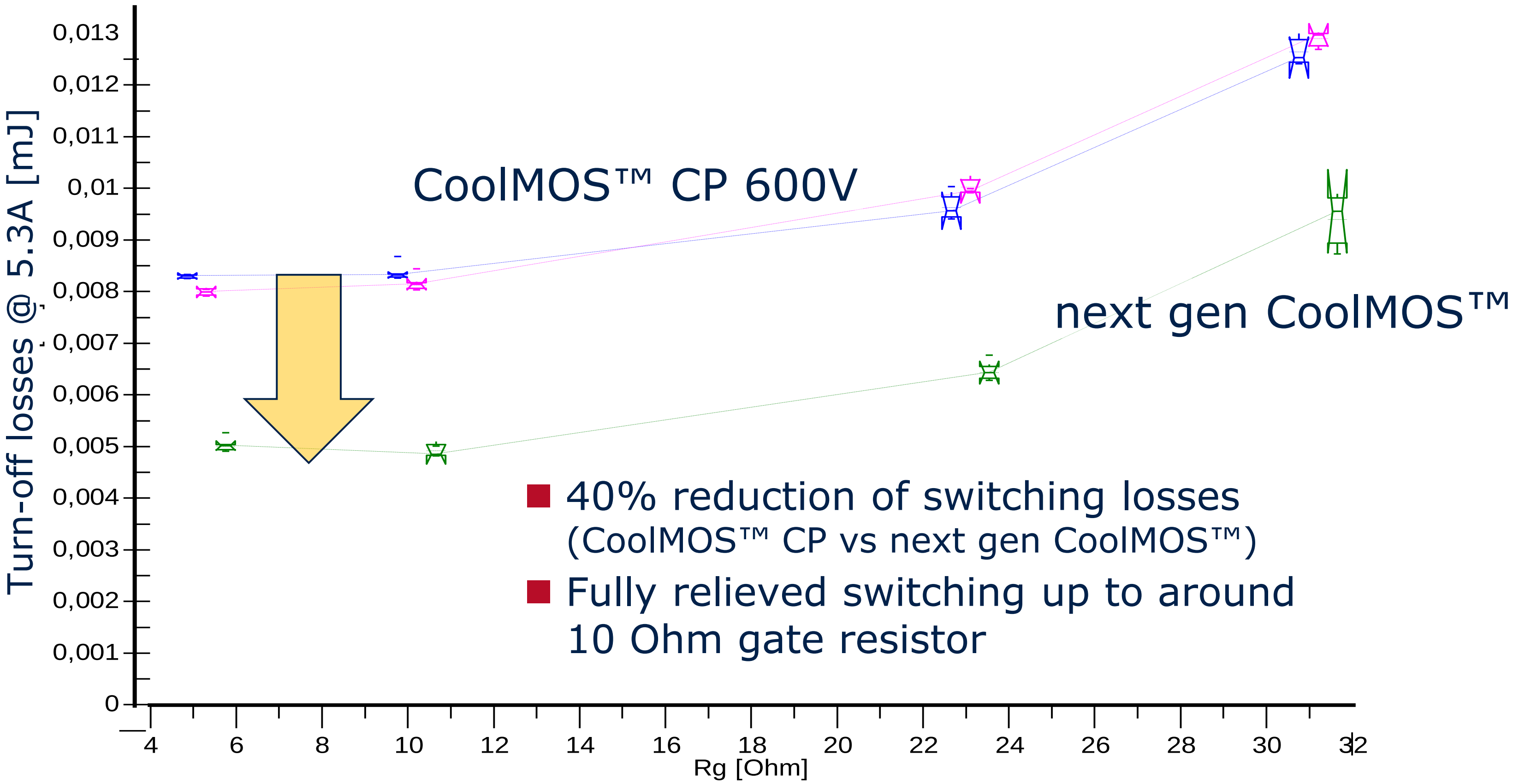


E_{oss} scales with cell pitch and can be brought below the level of 1st gen GaN devices 190 mOhm, 600V / 650V devices



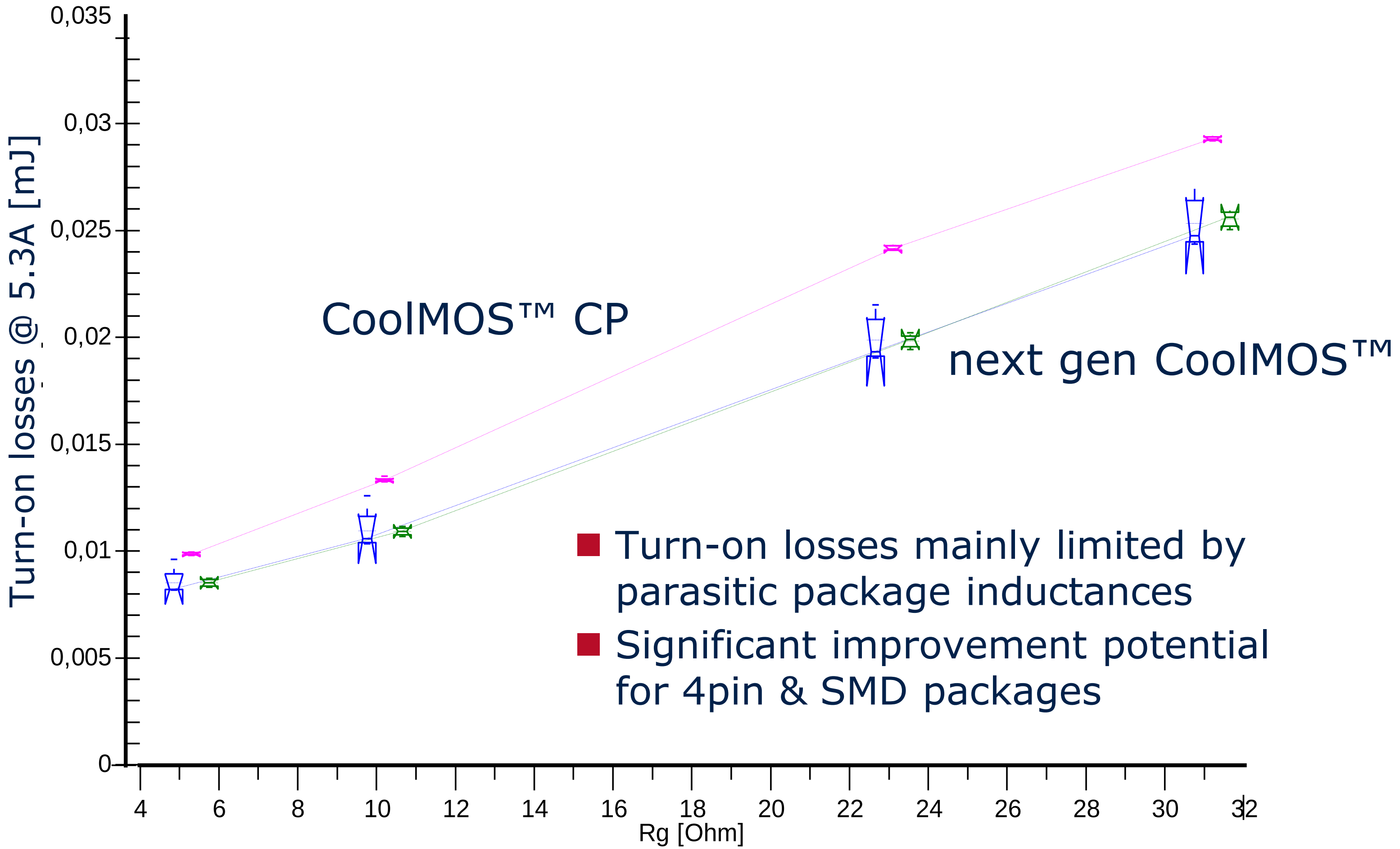
- FoM R_{on}*E_{oss} scales with pitch of SJ device
- next gen CoolMOS™

40% E_{oss} reduction versus earlier SJ generation fully translates into lower turn-off losses! 190 mOhm / 600V



- 40% reduction of switching losses (CoolMOS™ CP vs next gen CoolMOS™)
- Fully relieved switching up to around 10 Ohm gate resistor

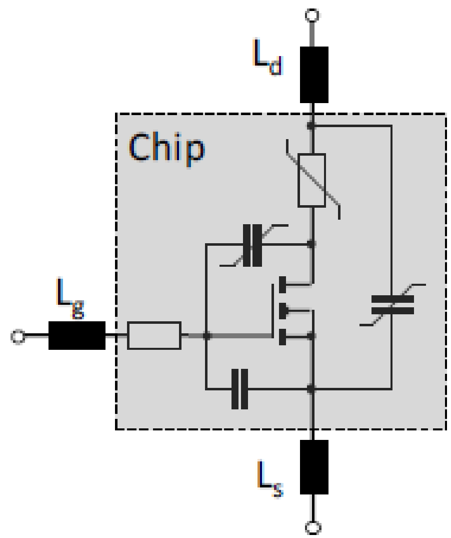
Turn-on losses are mainly determined by package and no longer benefit from silicon improvements! 190 mOhm / 600V



- Turn-on losses mainly limited by parasitic package inductances
- Significant improvement potential for 4pin & SMD packages

Package and switching cell optimization are mandatory to fully benefit from fast switching devices!

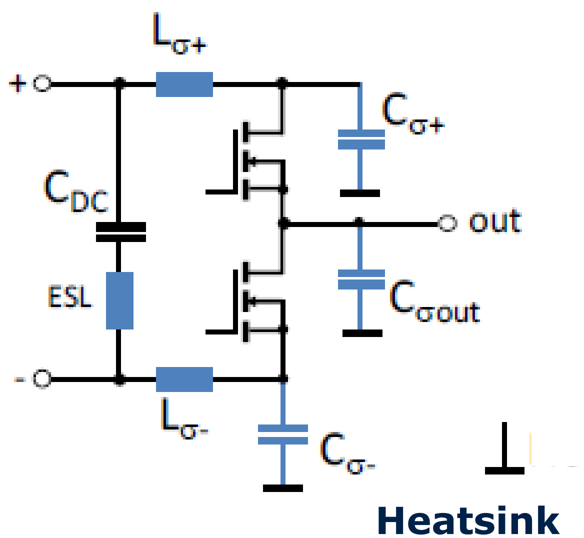
- **Package level**
  - Source inductance most critical
  - Solved by Kelvin contact
  - however inductance still in the commutation loop



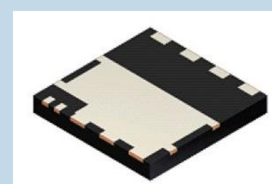
TO-247 4pin

Kelvin contact to source, decoupling of gate drive, E_{on} improvement

- **Switching cell level**
  - True SMD solution allows compact, low-inductive switching cell
  - Symmetric coupling capacitances to heatsink are important from EMI point of view
  - Top side cooling optional in DSO-20

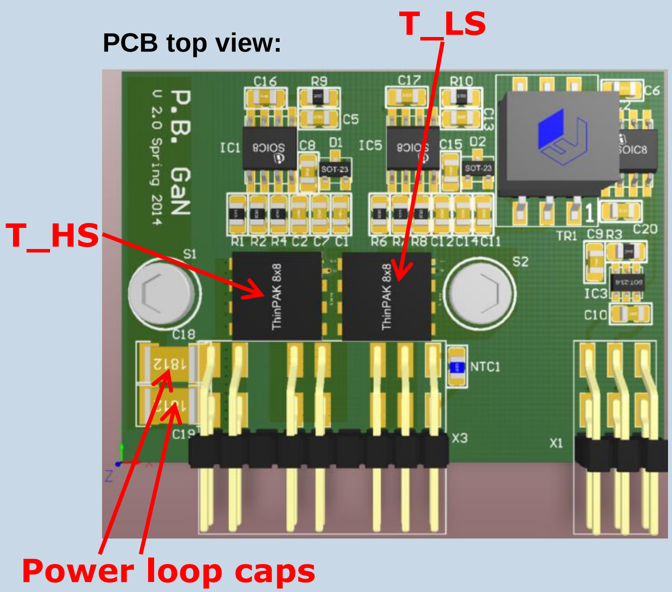


ThinPAK, TOLL, DSO-20

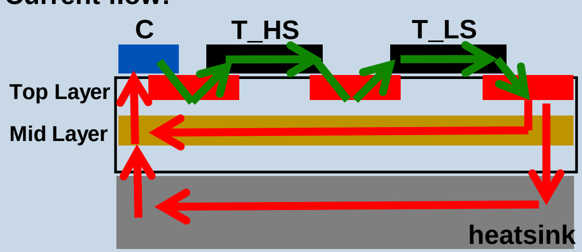


SMD packages will be important for SJ devices and mandatory for GaN!

PCB top view:

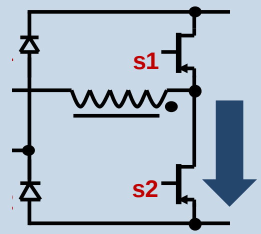


Current flow:



Commutation loop 3.2 nH

- Losses

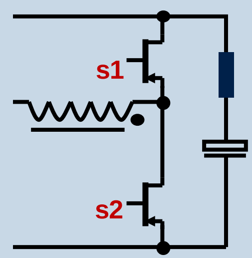


$C_{heatsink\ TO}$ = ~20 pF

E_{Cpar} = 1.6 µJ

E_{dev} = 3 µJ

- Voltage overshoot



$L_{par\ TO}$ = ~20 nH

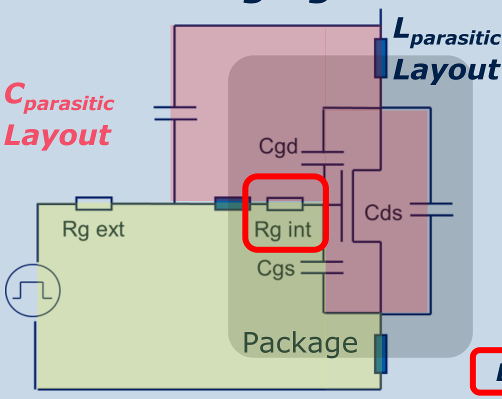
E_{lpar_10A} = 1 µJ

$V_{overshoot}$ = 100V @ 5kA/µs

L_{par} = 3- 6 nH

In case of layout constraints…

Possible Ringing Circuit

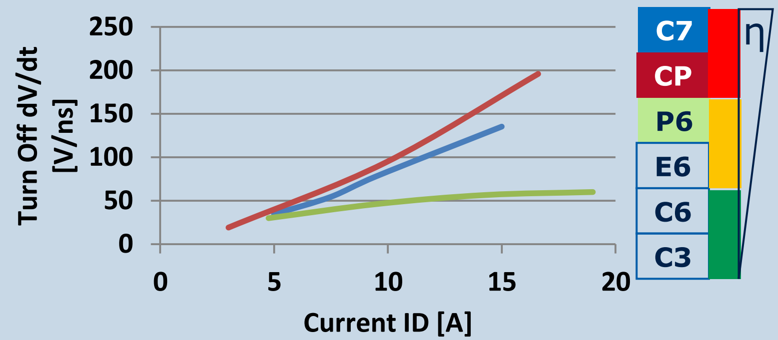


Damping Element

Oscillation circuit triggered by dV/ dt dI/ dt

dV/ dt

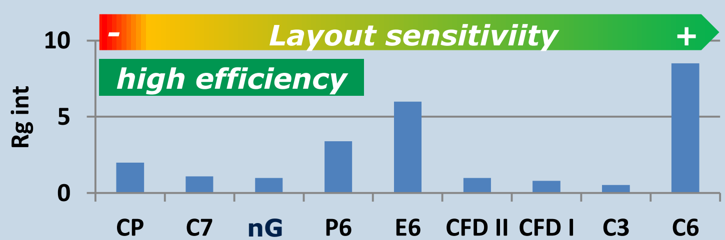
Example 190 mΩ



Low switching losses are inevitably coupled to high dv/dt and di/dt values both at turn-on and turn-off.

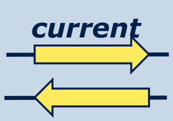
Layout Sensitivity

- **With C6 a integrated Gate Resistor was introduced to damp Oscillations**
- **Optimization tradeoff efficiency and Layout with each new technology**



How to use fast switching SJ devices

- **Avoid a coupling capacitance between G,D**
- **Place the gate resistor close to the gate**
- **Avoid Stray inductance in the Power Loop**
- **Use the mutual inductance effect (opposite current flow, forced current) in the power loop**



- **Add ferrite beads if necessary**

Best performance | Cost/performance segment | Ease of Use optimized

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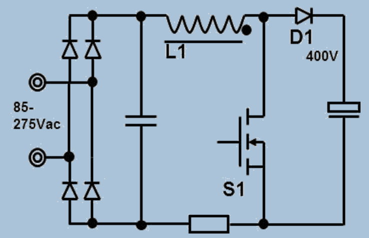
SJ devices will prevail in classic and dual boost GaN offers significant value in Totem Pole PFC

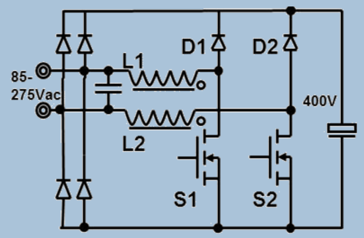
Classic PFC



- Less System Cost
- Less Efficiency
- High Power Density

- Superjunction (S1)
- SiC (D1)

Dual Boost PFC

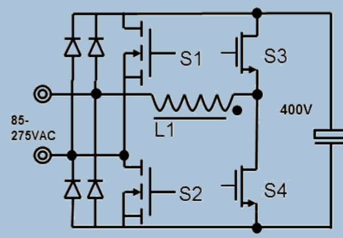


- High System Cost
- High Efficiency
- Less Power Density

- Superjunction (S1, S2)
- SiC (D1, D2)

GaN enables hard commutation on internal "diode"

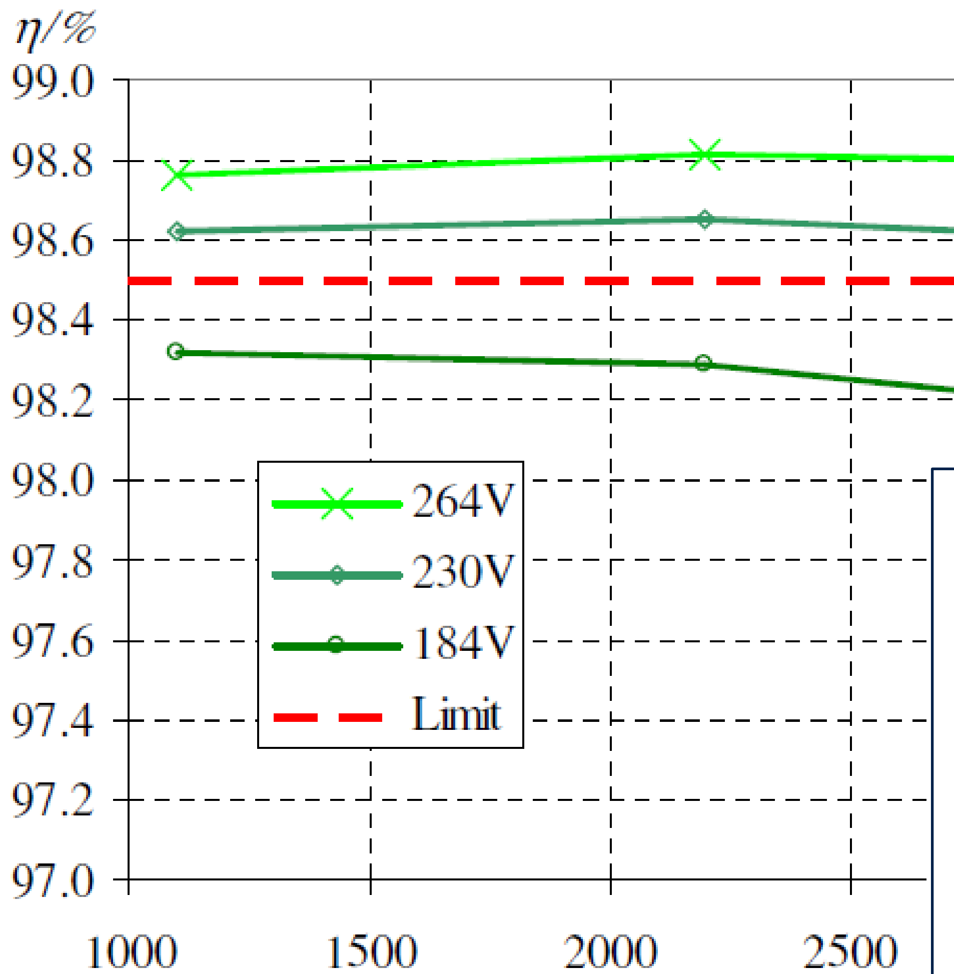
Totem Pole PFC

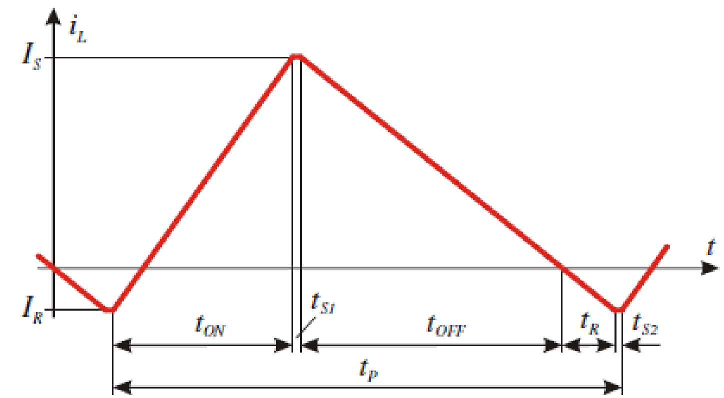


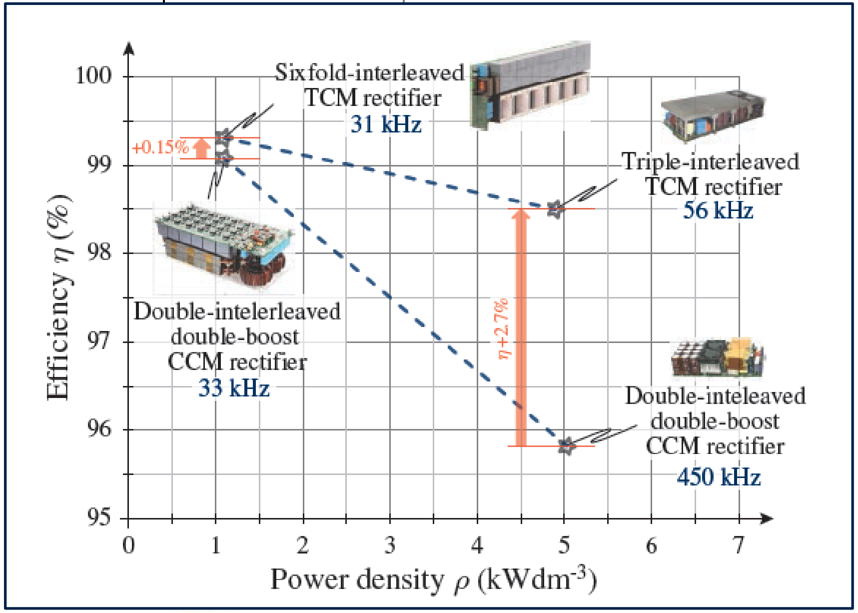
- Less System Cost
- High Efficiency
- High Power Density

- Superjunction (S1, S2)
- GaN, SJ, IGBT (S3, S4)

Best competing silicon alternative in terms of power density and efficiency: TCM PFC 3 kW, 4.5 kW/l (74W/in³)

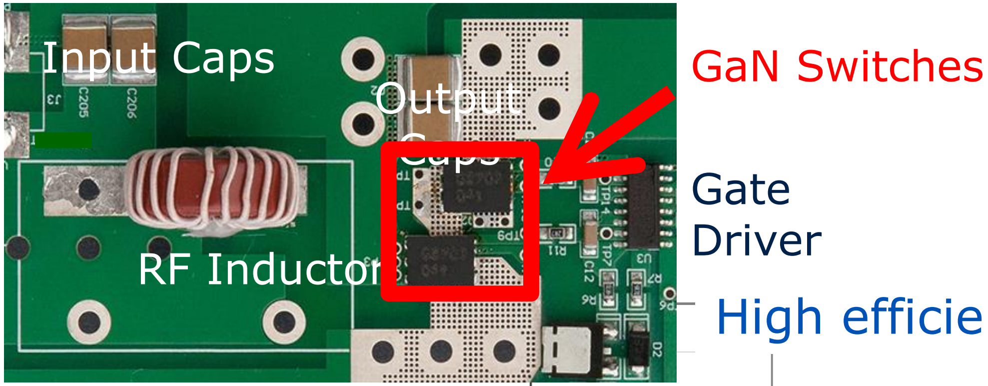




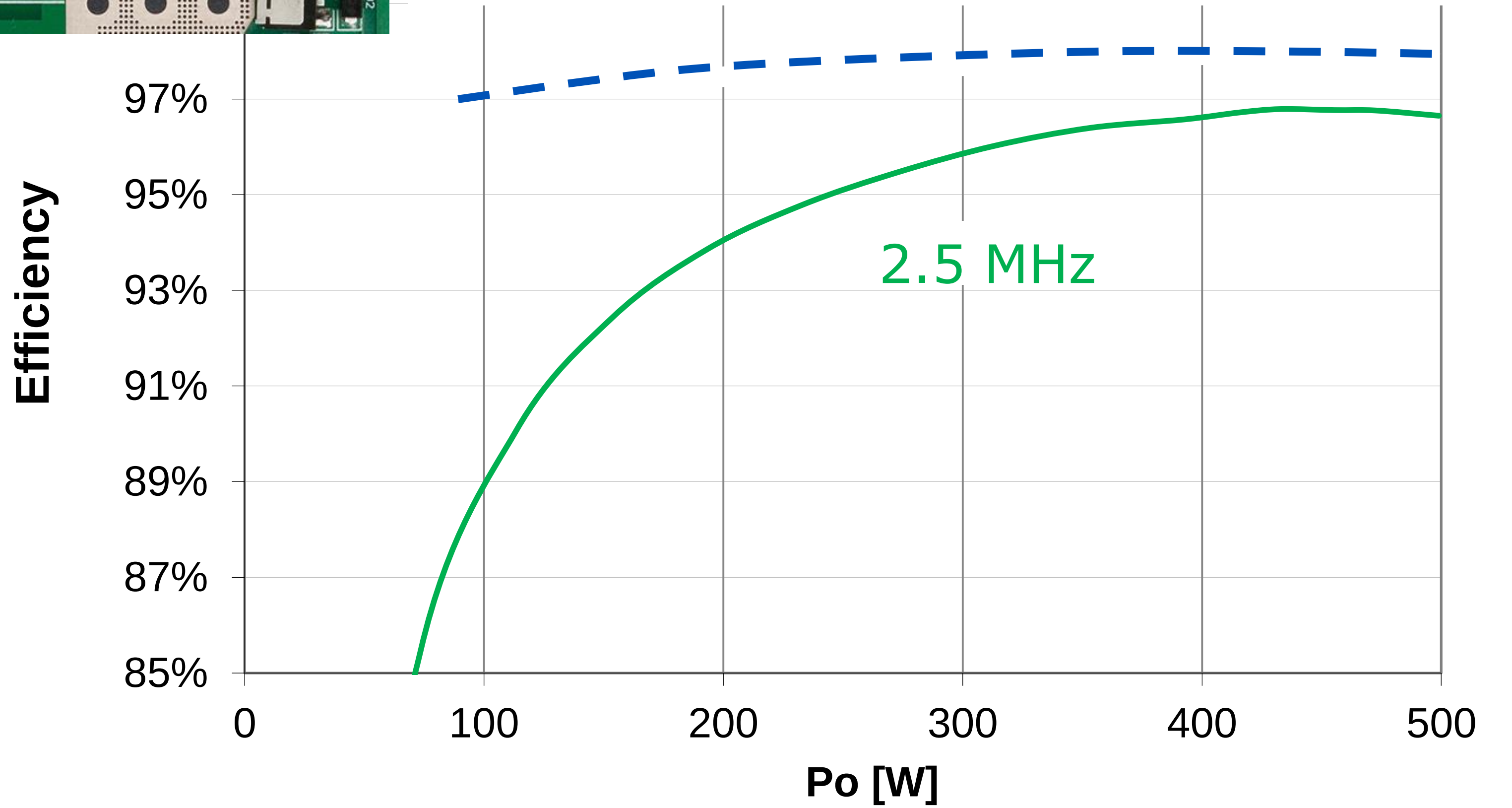


Source: U. Badstübner, J. Miniböck, J. Kolar, „ Experimental Verification of the Efficiency/Power-Density (η-ρ) Pareto Front of Single-Phase Double-Boost and TCM PFC Rectifier Systems", Proc. APEC 2013.

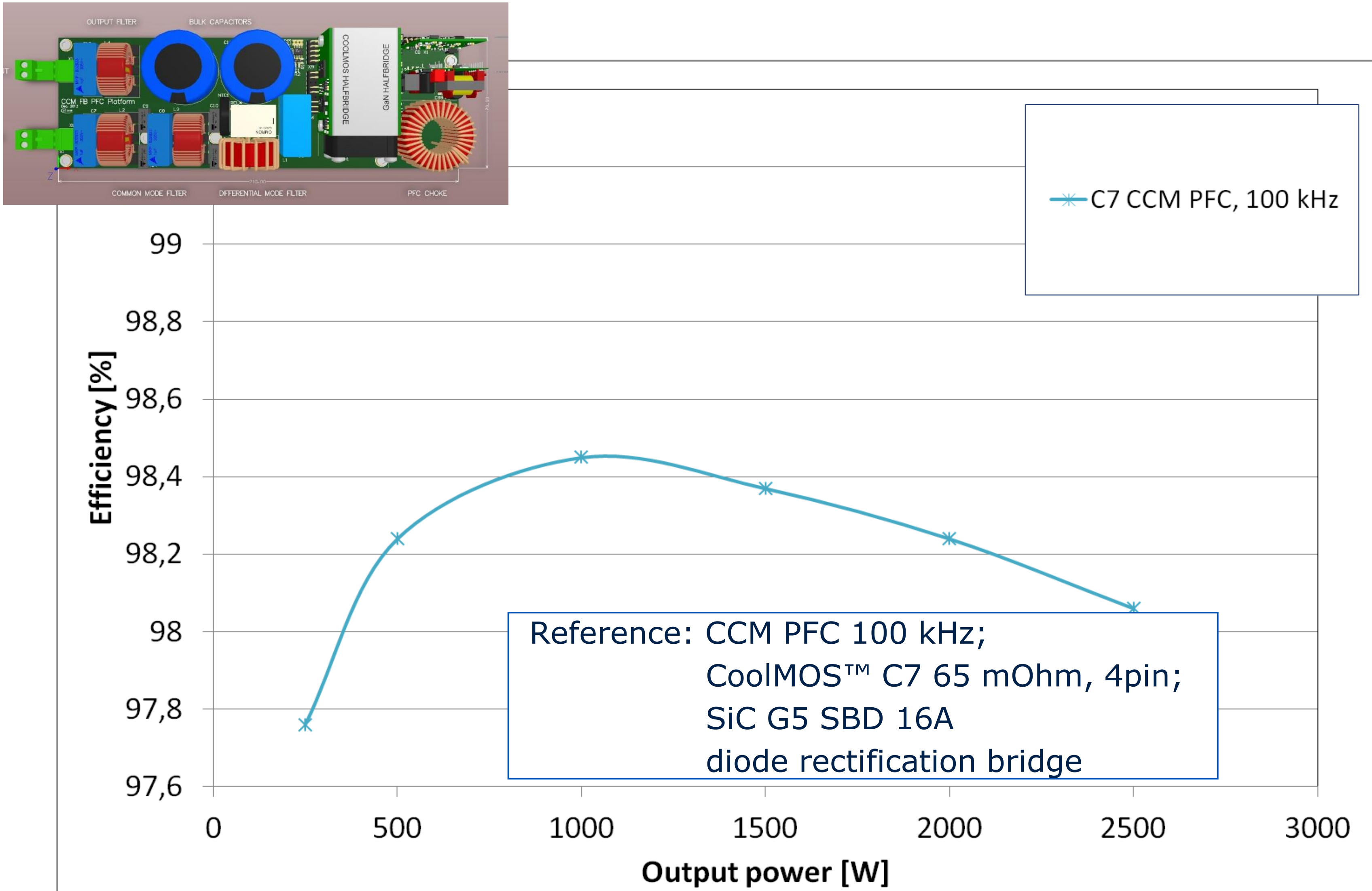
Advantage of GaN: very high frequency operation with $R_{on}*Q_{oss}$ and Q_g as key parameters



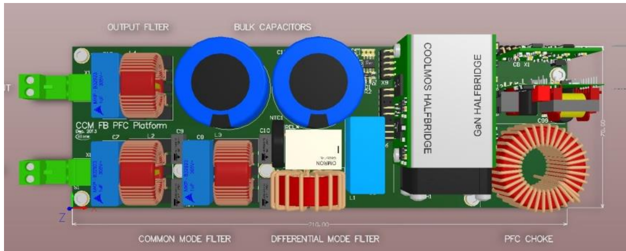
High efficiency possible by frequency control

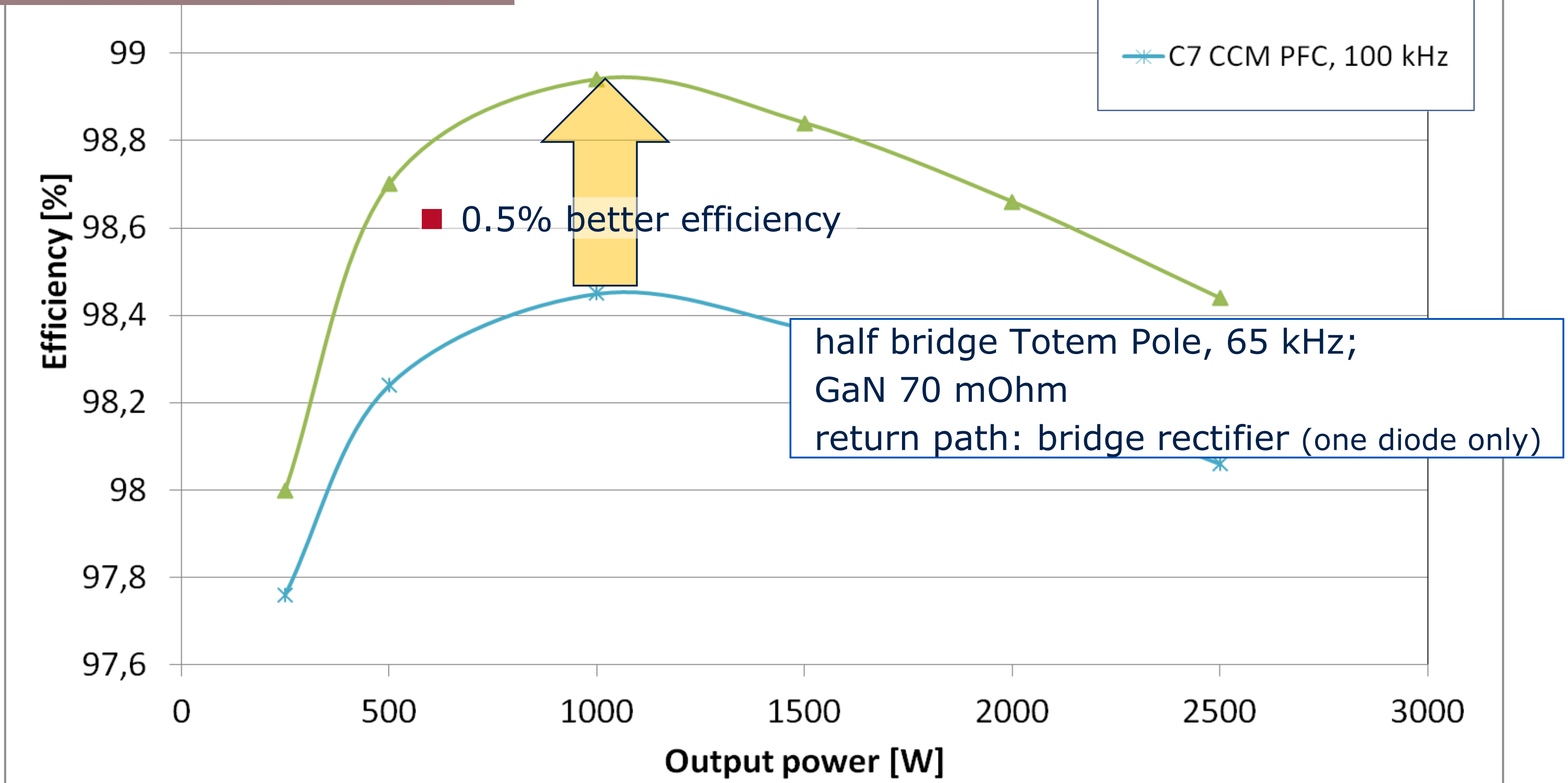


Comparison of hard-switching PFC stages: Reference: CoolMOS™ C7 / SiC G5



Advantage of GaN: CCM modulation in Totem Pole PFC, close to 99% efficiency with simple half bridge solution

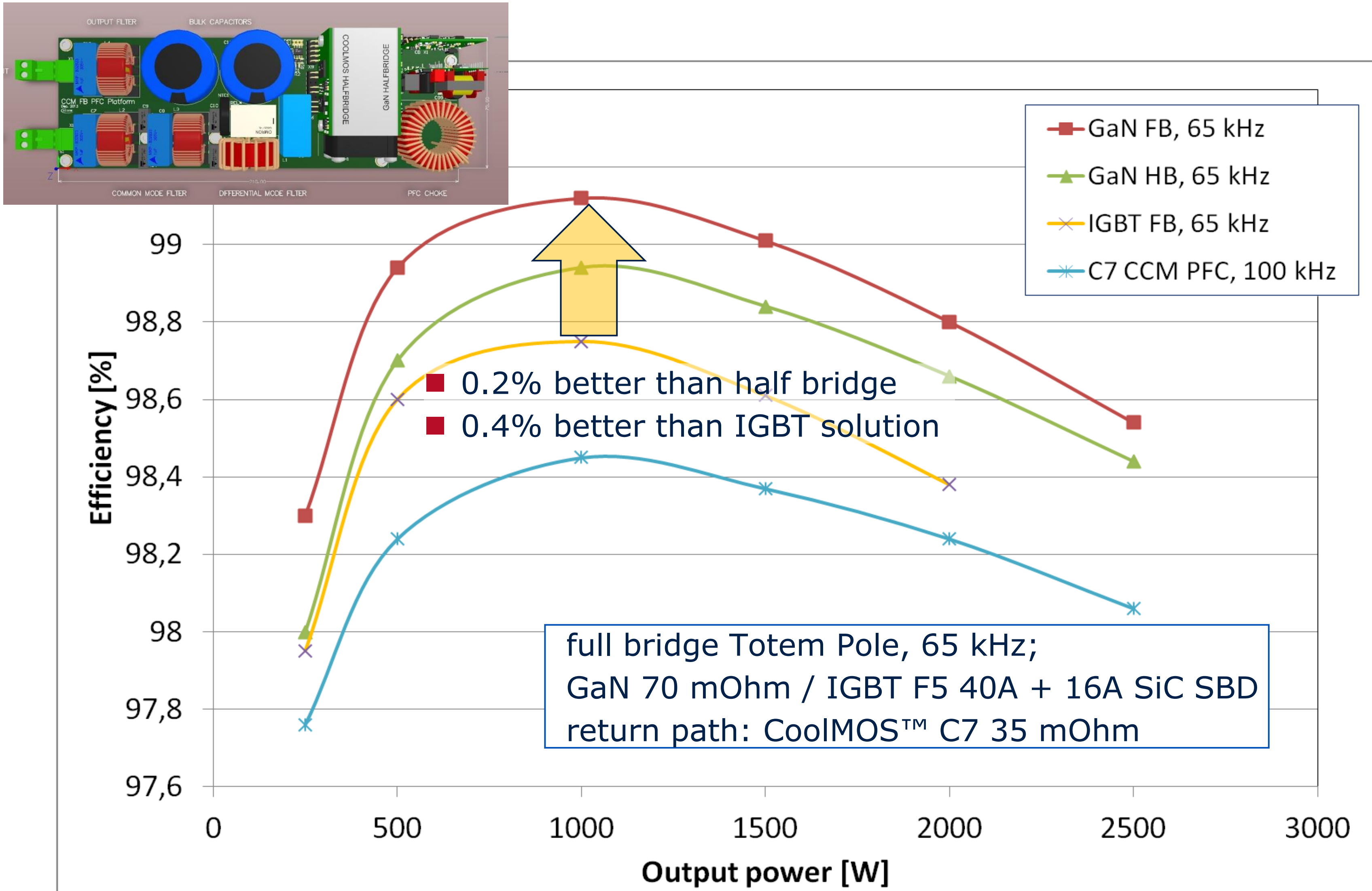




- 0.5% better efficiency

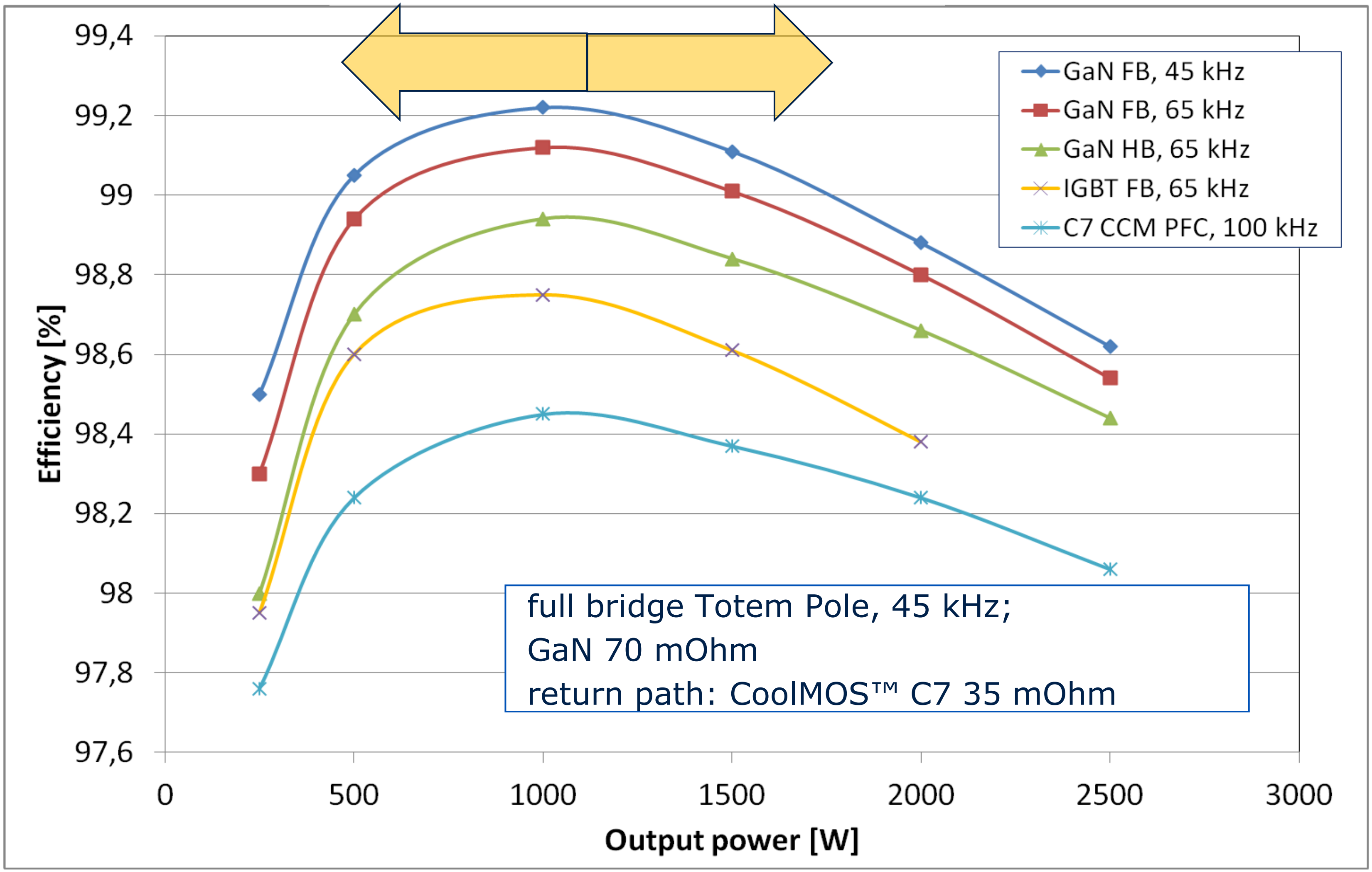
half bridge Totem Pole, 65 kHz;
GaN 70 mOhm
return path: bridge rectifier (one diode only)

Advantage of GaN: > 99% efficiency with combination of SJ and GaN in Totem Pole full bridge



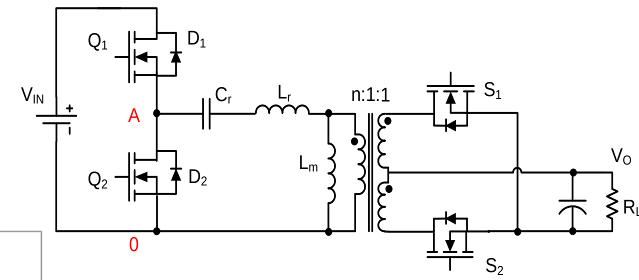
Advantage of GaN: > 99% efficiency across wide low range with low frequency Totem Pole PFC

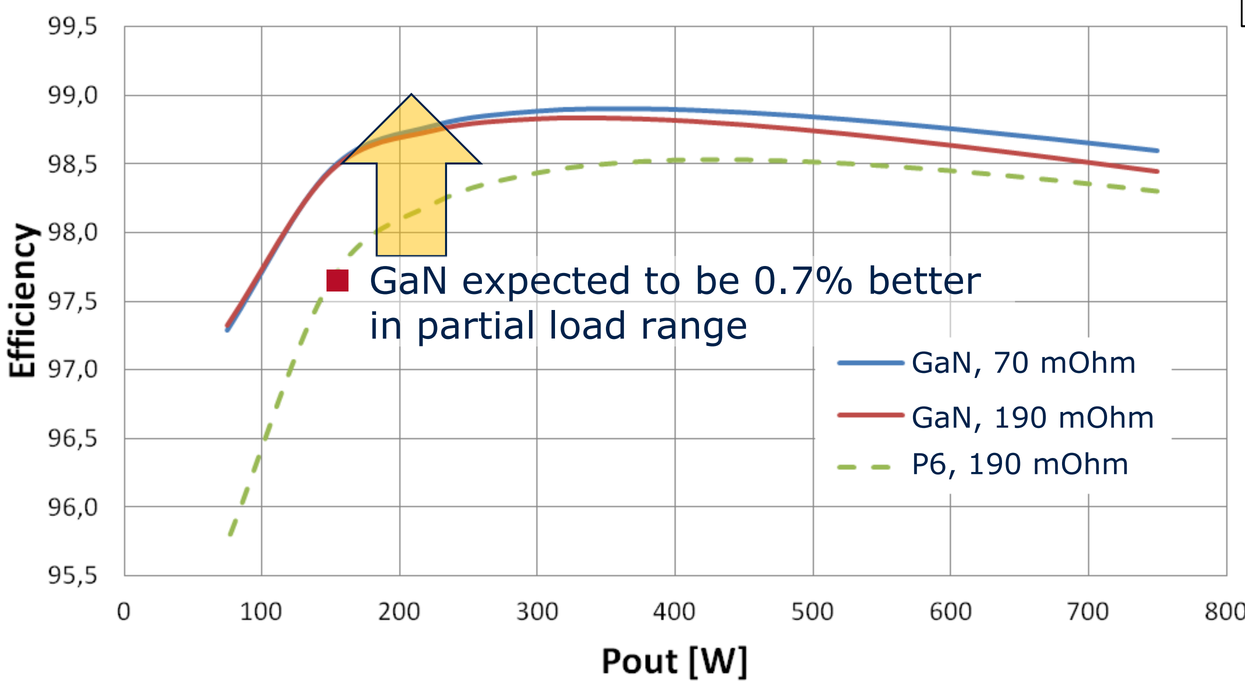
- >99% efficiency from 20..70% load
- 0.1% better than 65 kHz solution

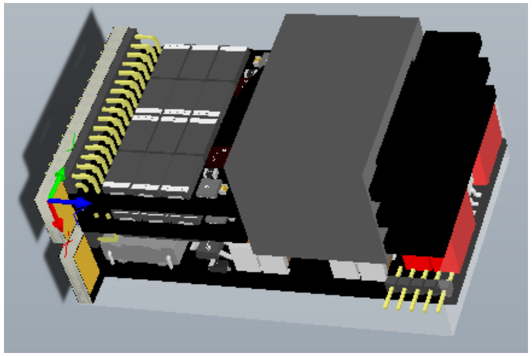


Expected performance of GaN versus latest SJ devices

- Resonant LLC DC/DC Converter (**750 W**, 400 kHz)

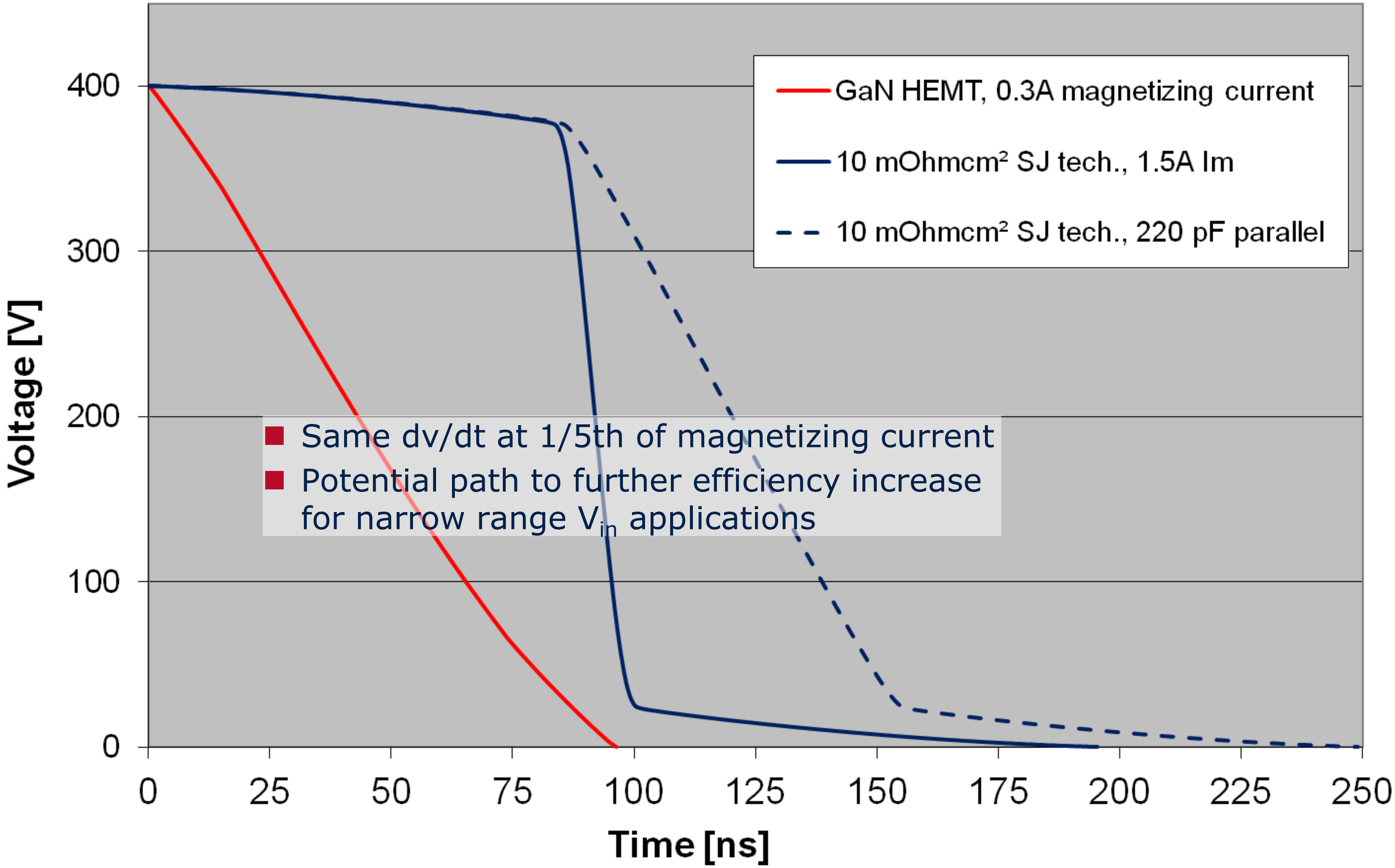






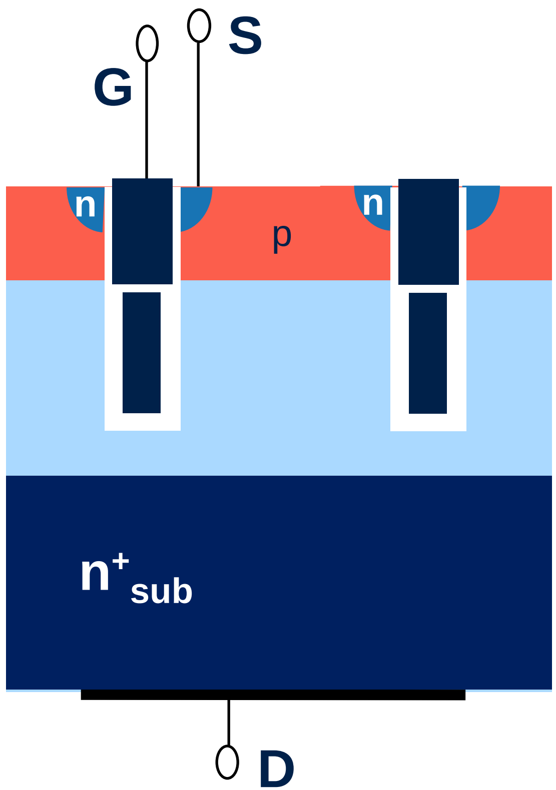
- 350V…410 V to 12 V
- Power density > 200W/in³
- Pure convection cooled

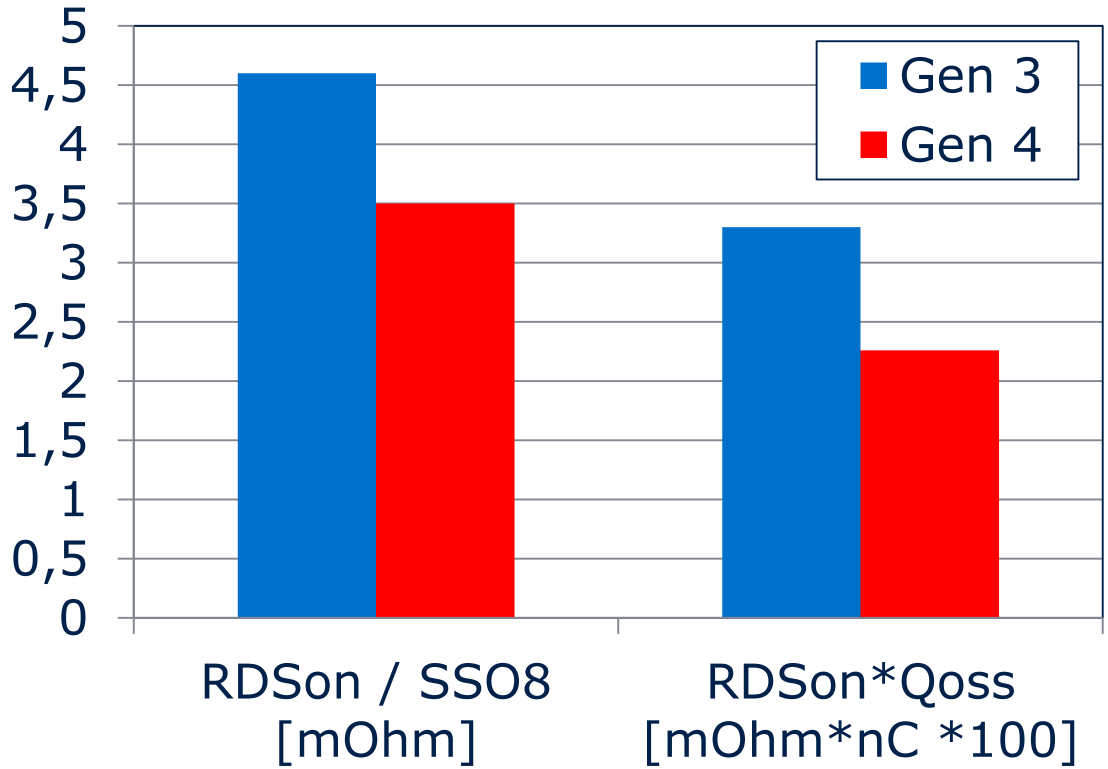
Latest SJ devices will benefit from parallel cap to counterbalance non-linearity



- Same dv/dt at 1/5th of magnetizing current
- Potential path to further efficiency increase for narrow range V_{in} applications

Last but not least! Recent improvements in key Figure-of-Merits for low voltage MOSFETs …

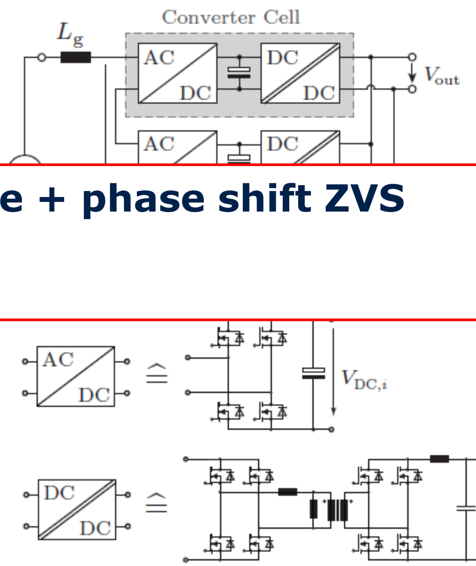




100 V MOSFET: smaller area-specific on-resistance and charges through further optimization of trench structure

… Allow new solutions by using cascaded multi-cell architectures!

- 3 kW AC/DC converter, 48V out



Cascaded converter topology, Totem Pole + phase shift ZVS
Efficiency target > 98%
100 V OptiMOS™ BSC034N10NS5

- FinSix 65 W Adapter, 19V out

Switching frequency > 10 MHz
200 V OptiMOS™ BSZ22DN20NS3

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Summary

- Superjunction devices will continue to deliver better Best-in-Class R_{DSon} devices with further improved FoM $R_{on}*E_{oss}$
- Recent improvements in low voltage devices FoMs allow to rethink classic architectures and consider the use of LV devices in HV applications
- The use of good layout practice, transition to 4pin packages and finally to SMD packages will become more and more important and is mandatory for GaN
- GaN offers specifically advantages both in terms of power density and efficiency at hard switching topologies with continuous use of the reverse characteristic and at very high switching frequencies in resonant converters

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SECURITY

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