

Simple turn-off description of Trench- Field-stop IGBT – IGBT³/3.3kV

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Abstract

New IGBT generations, i.e. Trench-Field-stop devices show significant difference in control characteristics in comparison to Power MOSFETs [1]. The reason is the large amount of stored charge, which builds up in the conduction mode. In this paper this storage effect is described by an additional element in an equivalent circuit, i.e. a capacitance at the output. A simple equivalent circuit contains the output characteristics, CGC-, CGE-, and the new CCE-capacitance. This circuit describes principal switching and control characteristics. Characterization of these elements is done by special test configurations, which allow excluding parasitic capacitance of the package. As an additional outcome of the work the stored charge IGBT³/3.3kV and its dependence on conduction time is received and will be presented.

Introduction

The Turn off of standard power MOSFETs under inductive load starts with a drop of gate voltage to the threshold for the actual load current. Then the gate voltage stays at that level while the drain voltage is rising and the drain current continues to flow. When the drain voltage reaches the DC-bus voltage the drain current starts to fall controlled by the gate voltage, now drop from the threshold level (Miller plateau) to the off state. The turn-off is completely controlled by the gate voltage – see solid traces of Fig. 1. Super-Junction MOSFETs can differ from this behavior.

Turn-off description of trench field stop IGBT

The Trench-Field-stop IGBT is well suited for inverter circuits, which benefit from low conduction losses. These low losses are achieved by significantly increased carrier density compared to former generations. During turn-off against inductive load, such devices don't require an open MOS-channel all the time to carry the load current. For a short period of time the stored charge is feeding the load current. This behavior occurs at the end of the Miller plateau, where the gate voltage shows a dip (Fig. 1), i.e. the MOS-channel closes while the load current is still running. During this period the collector voltage is rising according to the decay of stored charge.

Fig. 3 illustrates the turn-off under different load currents. The dV/dt of the collector voltage varies with the amount of load current in a way similar to loading a capacitor by a constant current. This leads to the equivalent circuit of Fig. 2, which represents the switching of a Trench-Field-stop IGBT by the output characteristics to describe the static characteristics, a collector-gate-voltage dependent capacitance a constant gate emitter capacitance and an additional output capacitance C_q , which is much larger than the usual junction capacitance between collector and emitter. The tail current is described by an R-C element. The additional output capacitance varies with the amount of stored charge, which depends not only on load current but also on the time the IGBT was in conduction mode. The charge, which is

stored in conduction mode and is extracted during collector voltage rise until $V_{CE}=V_{DC}$, is presented in Fig. 4 with reference to on-time of the IGBT.

A further stored charge influence on the switching behavior can be shown by variation of the gate turn-off resistance. Fig. 5 illustrates the turn-off under different gate resistors. For gate resistors ranging from 1 to 30 Ohm, the dV/dt of the collector voltage is constant. The dV/dt is intrinsically limited. The reason is the stored charge controlling the voltage rise. For gate resistors of more than 30 Ohm the dV/dt becomes reduced at controlled by the gatedrive condition, i.e. R_G . The Miller plateau duration is stretched. During the stretched Miller plateau a significant amount of stored charge is withdrawn and resulting in a higher dI/dt during current fall. This can be detected by an increased over voltage (Fig. 5).

The additional output capacitance C_q (Fig. 2) shall describe the self limitation of dV/dt and the effect of stored charge, whereas $C_q(V_{CE})$ is a function of $V_{CE}(t)$. During turn-off the collector current divides into MOS-channel and stored charge current. The amount of the MOS-Channel current can be detected by measurement of gate emitter voltage and calculated using the transfer characteristics of the IGBT. The difference between collector current and the MOS-channel current is the share of the stored charge. In the phase of turn-off where the MOS-channel current is neglect able (for low R_G) the output capacitance C_q carries the whole load current and determines the dV/dt . The characterization of C_q for the whole range of Gate resistors, currents, V_{DC} and t_{on} allows to describe the turn-off with respect to more or less stored charge. As an example this calculated capacitance for different load currents is presented in Fig. 6 with reference to the collector voltage of the IGBT.

For the characterization of the IGBT a special test setup (Fig. 7), which prevents package capacitance, was used. Fig. 8 shows a sectional view of the IGBT on the substrate and the circuit diagram for the test. A further benefit is that only one IGBT chip without free-wheeling diode was tested. This reduced the total capacitance which must be charged and discharged during dV/dt of the collector voltage and no paralleling effects between two or more IGBTs occur. For the measurement of the true gate emitter voltage the internal gate resistor is shorted. This test setup allowed a pure characterization of the static and dynamic parameters without influence of the package parasitic capacitance.

Conclusion

A simple behavior model is presented which is easy to establish by characterization and implementation in circuit simulators. It allows better understanding of gate drive and turn-off characteristics of new IGBT generations. The model is applied to the recently introduced IGBT3/3.3kV.

Literature

- [1] Pfirsch, Bayerer: MOS-gesteuerte Leistungsschalter: Konzepte und Schaltverhalten, ETG 2006, Bad Nauheim, Germany
- [2] Bayerer: Switching Behavior of Power Switches (IGBT, MOSFET), ECPE-Seminar 29&30-Jun-2011, Electronics around the Power Switch, Gate Drivers, Sensors u Control, Munich, Germany

Figures

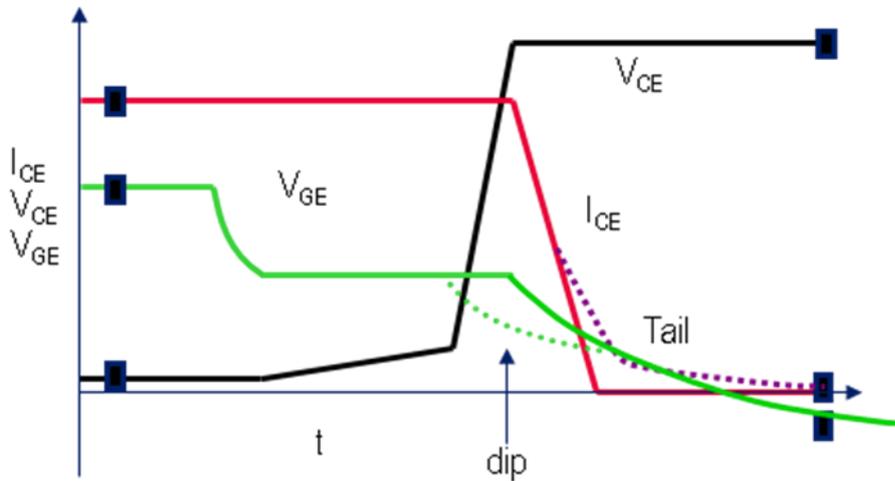


Fig. 1: Turn-off of MOS-devices. Solid traces apply to standard MOSFET. Dashed deviations apply for IGBTs. Dip in gate voltage means the collector current is carried on by stored charges.

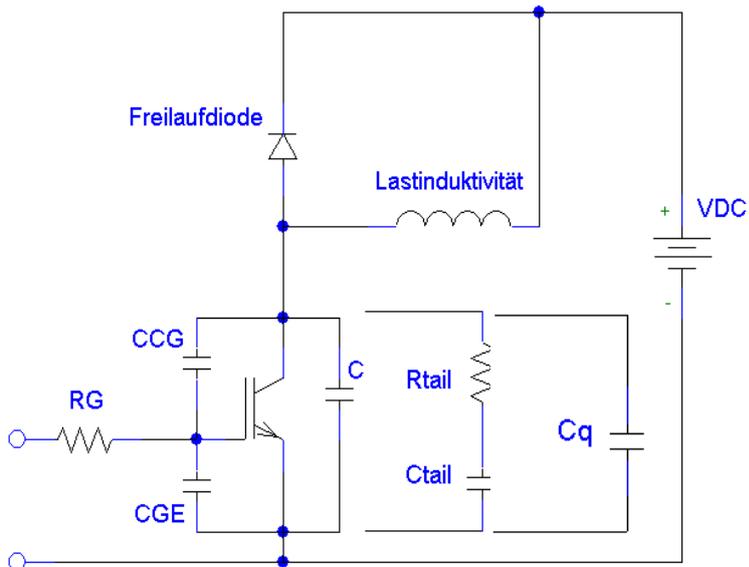


Fig. 2: Equivalent circuit describing Turn-off of Trench-Feldstop-IGBT under inductive load. The IGBT symbol stands for the static output characteristics $I_{CE}(V_{CE}, V_{GE})$. $CCG(V_{CE})$, CGE and C are well known elements for MOSFETs and IGBTs, C_q , C_{tail} and R_{tail} are introduced here to describe the bipolar behavior of the IGBT

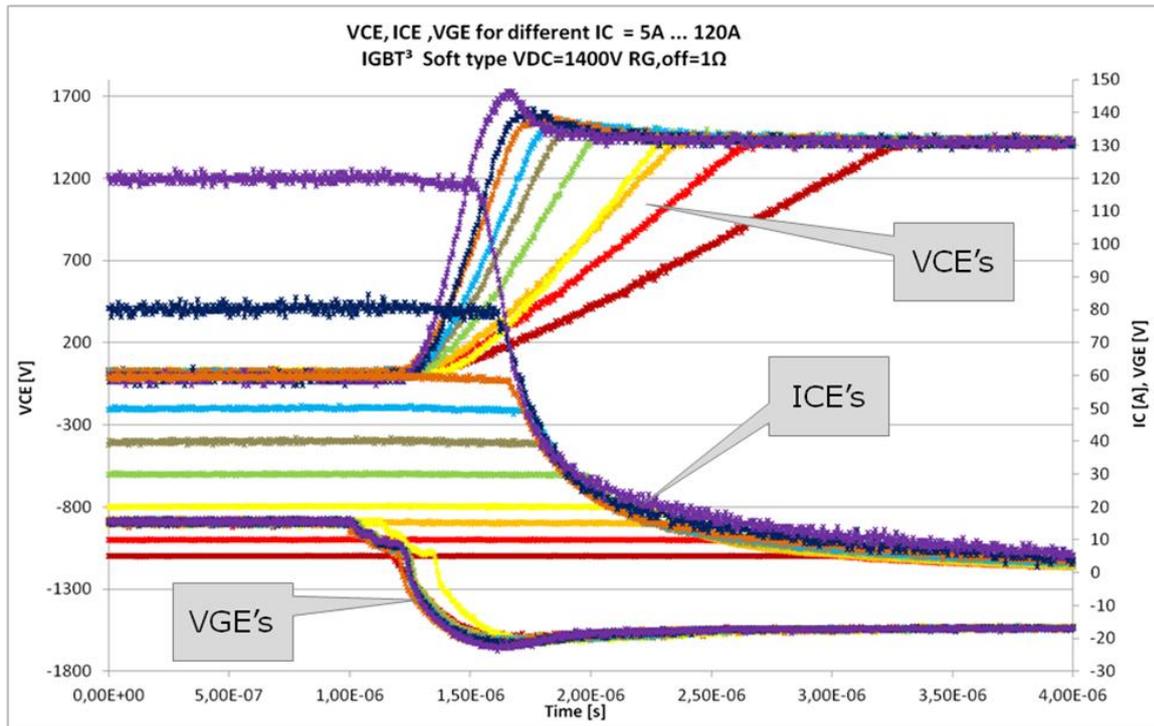


Fig. 3: Turn-off of 3.3kV-IGBT3, single chip under different load currents. See the variation in dV/dt with changing collector/load current. At low gate resistance (1 Ohm) the gate voltage drops before collector voltage has risen to $VDC=1400V$.

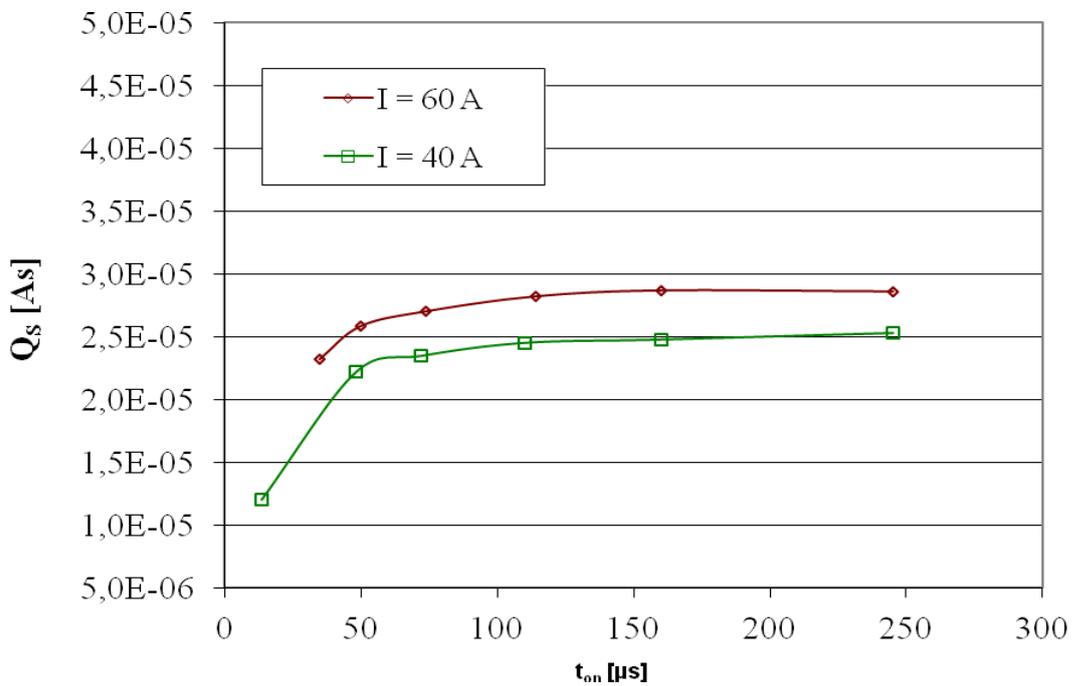


Fig. 4: Charge stored in 3.3kV/IGBT3 - single Chip - as a function of on-time, $Q_s=f(t_{on})$. $IC=40A$, $t_{on}=14...245\mu s$ and $IC=60A$ $t_{on}=35...245\mu s$, $VDC=1400V$, $RG=1\Omega$

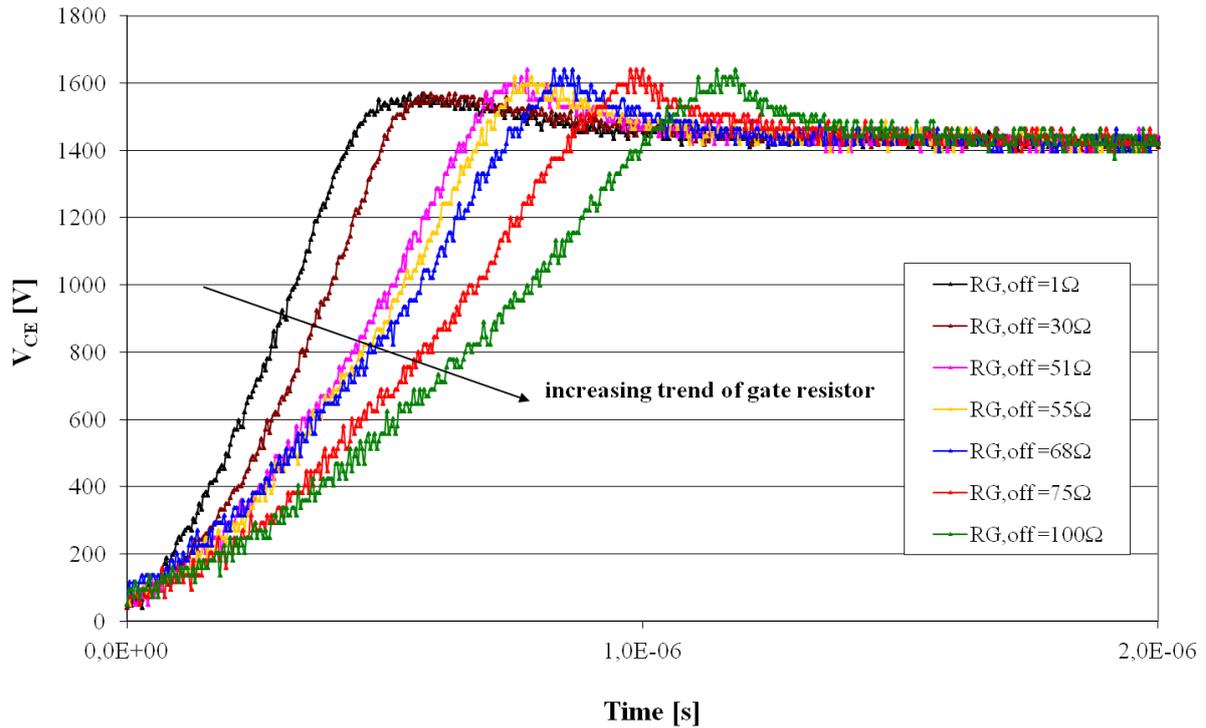


Fig. 5: Turn-off of 3.3kV-IGBT3, single chip switched with different gate resistors. See the variation in dV/dt with changing the resistor. $V_{DC}=1400V$, $I_C=60A$, $t_{on}=100\mu s$

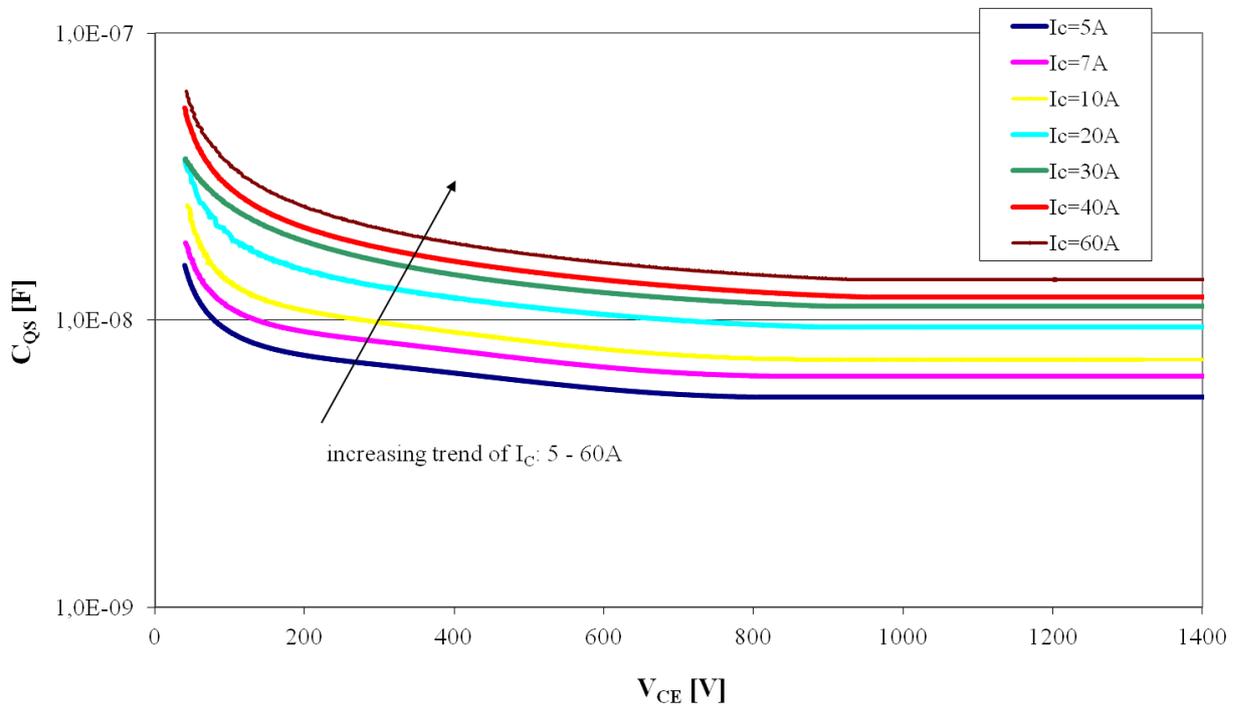


Fig. 6: Calculated additional output capacitance C_q for different load currents - as a function of the collector voltage. $V_{DC}=1400V$, $R_G=1\Omega$

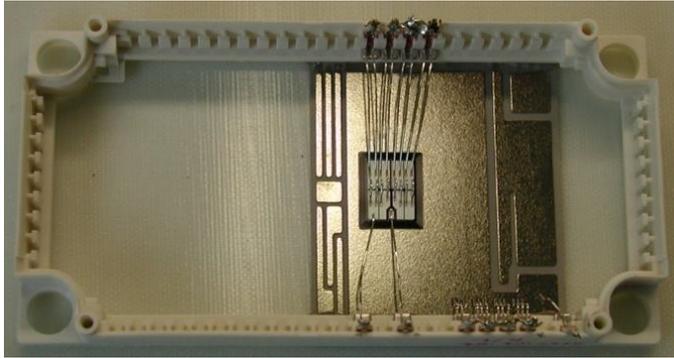


Fig. 7: Single IGBT chip on a substrate, which prevents package capacitance.

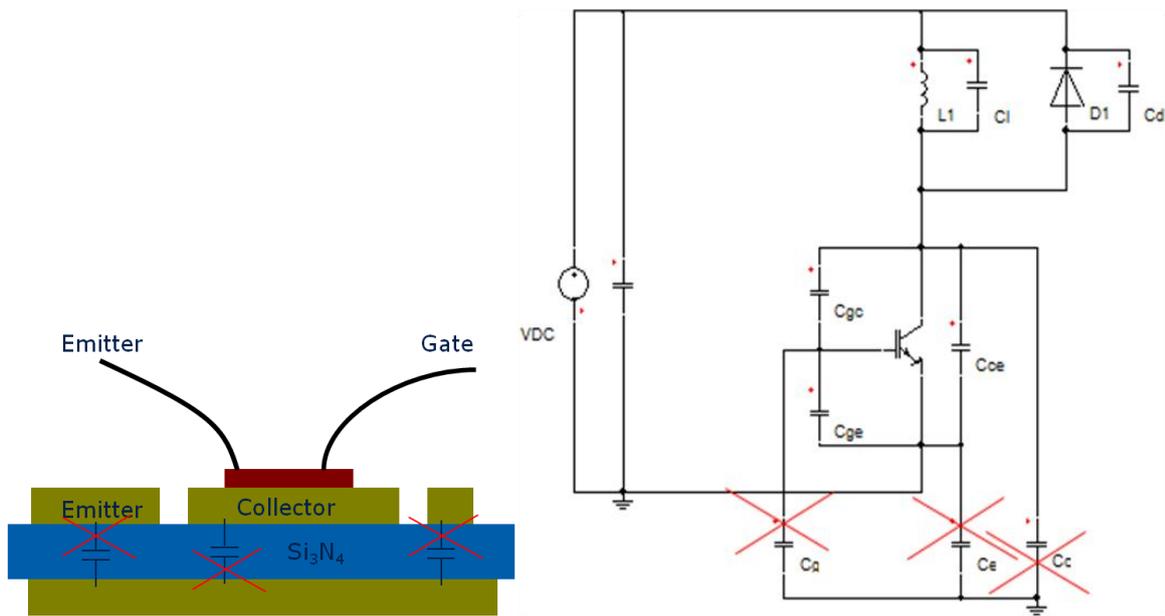


Fig. 8: left: sectional view of the IGBT on the substrate right: test circuit diagram