Optimizing layout for paralleling power discrete semiconductor devices

About this document

Scope and purpose

In high-power applications, such as industrial motor drives or renewable energy systems (e.g. Solar, Energy Storage Systems), it is a common practice to employ multiple IGBTs in parallel to distribute the load. This method permits a significant increase in the power handling capacity. However, it also introduces a set of challenges that require meticulous management to ensure that the system operates in a dependable and effective manner.

One crucial aspect to consider is the proper distribution of current among the paralleled devices. Paralleling challenges can be overcome by utilizing IGBTs with closely matched characteristics, particularly with respect to thermal and layout aspects. Guaranteeing a balanced current distribution is essential for optimizing the performance of a parallel IGBT configuration.

This comprehensive application note presents an overview of the challenges associated with unbalanced parallel devices in both symmetrical and unsymmetrical printed circuit board (PCB) layout configurations. It also delves into the specific impact of TO-247 4-pin devices on paralleling. Furthermore, this document provides detailed insights and recommendations that are applicable to a wide range of converter designs, including discrete IGBTs or discrete SiC MOSFETs.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems. The primary target are design engineering seeking to parallel discrete devices.

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1 Introduction

Paralleling discrete devices has emerged as a solution to the escalating demand for handling higher currents and power levels that surpass the capability of a single device. IGBTs have gained significant traction in high-power applications such as motor drives, power converters, and induction heating. Consequently, the practice of connecting discrete devices in parallel has become more prevalent. This approach, however, is not limited to discrete devices, it is also useful in modules where multiple chips are interconnected in parallel.

Despite its widespread adoption, a high-power design presents several challenges that necessitate thorough consideration [1] [2]. These challenges include:

- Requirement for a symmetrical PCB layout to ensure optimal performance
- Implementation of effective thermal management strategies
- Management of device characteristics that can lead to current imbalance if the parameters are not precisely matched or if the layout lacks symmetry

1.1 Current imbalance

The imbalance in current sharing among parallel devices can result in increased power dissipation and higher component temperatures. Implementing a symmetrical loop design for power and gate signals on the PCB can address this issue. It will also ensure a consistent signal propagation time for parallel devices and minimize the impact of current imbalance on the performance of paralleled converters.

Temperature variations in the semiconductor can lead to fluctuations in the current flowing through the IGBT (I_c) and affect the threshold voltage ($V_{GE(th)}$). Therefore, it is crucial to analyze the influence of junction temperature (T_j) on $V_{GE(th)}$ and $V_{CE(sat)}$ thoroughly and implement effective design techniques to minimize the current imbalance.

Balanced characteristic curves for all devices are essential for the proper functioning of parallelized IGBTs. Current imbalances during IGBT switching, caused by temperature and delay time variations, become more pronounced at higher switching frequencies. Addressing factors that contribute to thermal imbalances and utilizing layout and thermal design can significantly reduce variations.

The direct impact of the current imbalance on device reliability and system output power in parallel connections cannot be overlooked. An imbalance may lead to high current overshoot in some devices, potentially pushing them beyond the safe operating area (SOA). This can result in overtemperature, thermal runaway, and stability and security challenges for the entire system. Therefore, effective mitigation of the current imbalance is crucial for enhancing device reliability and overall system stability.

1.2 Boundary conditions

In power electronic systems, parallelization is used for increasing their overall capacity by boosting the power capacity of converters and ensuring a balanced current. However, it is hard to achieve the perfect balance due to various factors that interact with each other and lead to unavoidable current imbalances. Minimizing this imbalance is important because it can arise from switching losses or temperature variations that can affect the reliability of the system and reduce the power output.

IGBTs, which are widely used to power electronic semiconductors, are often used in parallel designs as separate devices, individual cells, or power modules. It is important to understand how they behave and how factors such as temperature, device differences, driver circuits, power layout, and other electrical components affect parallelization.

Some IGBT technologies have a narrow range of parameters across different voltage and current levels. This makes it easier to pick the right devices during the design process. However, getting a perfectly balanced design can be challenging because of other component's thermal considerations and the placement of passive components when using multiple distinct devices together.

This document provides different layout ideas for designers and discusses how current imbalances can affect different power loops. It also offers suggestions on how the device's electrical traits are distributed and how the gate loop influences current sharing, even though these topics are not the focus of the document. Additionally, the document briefly talks about the importance of the Kelvin pin in TO-247 4-pin packages.

2 Circuit description

This application note investigates a half-bridge topology employing discrete devices connected in parallel. The initial investigation focuses on assessing the current sharing in the half-bridge circuit, as shown in Figure 1. The simulation results from a system utilizing four IGBTs in parallel are analyzed in a later chapter. The simulation model comprehensively incorporates the parasitic inductances and resistances of all interconnections within a PCB layout optimized for symmetrical current sharing. These details are not depicted in the simplified schematic.

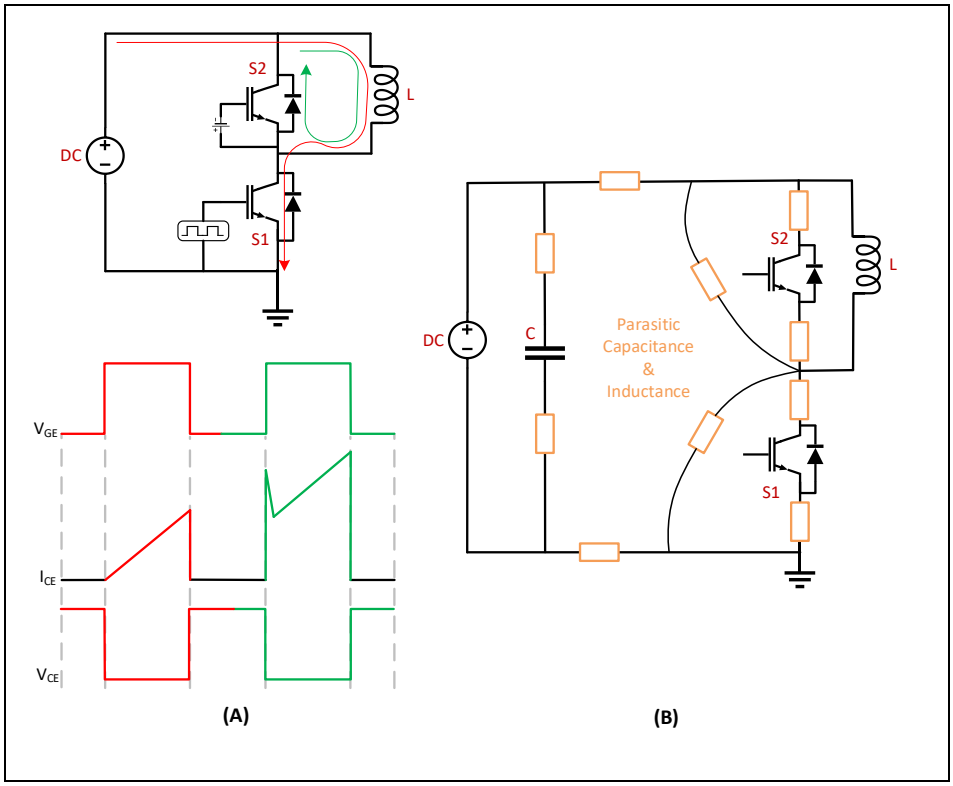

Figure 1 (A) A simplified half-bridge circuit (B) Parasitic elements in the half-bridge circuit

In high-frequency power electronic circuits such as the half-bridge hardware, meticulous attention to the PCB layout is imperative. Mitigating stray inductance (L_s) in the device's current (I_c) path is essential for preventing overvoltage transients when the device turns off. Stray inductance typically encompasses the DC-bus capacitor lead inductance (L_c), DC-link inductance (L_{dc}), and device-lead inductance. While certain inductances, such as package inductance, are beyond the designer's influence, it is important to minimize the rest for optimal performance.

The design of the circuit significantly influences the losses in parallel IGBT devices. Key factors affecting these losses include current sharing, switching losses, conduction losses, and parasitic elements in the layout. Inadequate PCB layout, i.e., unequal trace lengths and widths, can introduce varying resistance that can lead to uneven current distribution. This discrepancy in current sharing can elevate conduction losses that are directly proportional to the square of the current and the resistance of the devices.

$$P = I^2 * R$$

The presence of parasitic inductance in the gate and power loop can also impact the switching losses of the devices. These losses are contingent upon factors such as the gate resistor, synchronized switching, switching frequency, voltage, and current. To mitigate the impact of parasitic inductance and capacitance, use of a solid ground plane and decoupling capacitors is recommended. Note that the dissipated energy stored in the parasitic inductance contributes to overall switching losses.

$$E = \frac{1}{2}LI^2$$

These parasitic inductances have significant implications on the performance and dependability of parallel devices. Particularly in high-power applications where even minor levels of inductance can prompt voltage overshoot, oscillation, and higher switching losses. When combined with parasitic capacitance, the parasitic inductance can form LC resonant circuits that generate oscillations at high switching frequencies. This can lead to electromagnetic interference (EMI) and additional switching losses.

2.1 Equivalent model of a half-bridge

When designing converters with high power density, **it is common to utilize discrete components due to their fast switching speed, high conversion efficiency, and favorable thermal characteristics.** However, the rapid switching speed can lead to voltage overshoots during transitions, resulting in EMI and potentially impacting system reliability. Therefore, it is crucial to include the capacitances and loop inductances of a system in simulations to assess and mitigate EMI early in the design process.

One major challenge is that most device manufacturers do not provide detailed information on loop inductance in their datasheets. This section will discuss the 2-level half-bridge and explore the impact of parasitic properties.

A standard half-bridge comprises seven terminals. Three of those are related to the power delivery loop (high-side power terminal, low-side power terminal, and output terminal). The remaining four are associated with the gate control loop (high-side gate terminal, high-side gate return terminal, low-side gate terminal, and low-side gate return terminal).

Figure 2 shows the equivalent circuit model of a half-bridge with seven terminals. It incorporates two gate driver paths for the switch, the equivalent gate resistances to the high-side and low-side devices (RGH and RGL, respectively), and equivalent loop inductance and resistance in the high-side (LH and RH) and low-side (LL and RL) power loops.

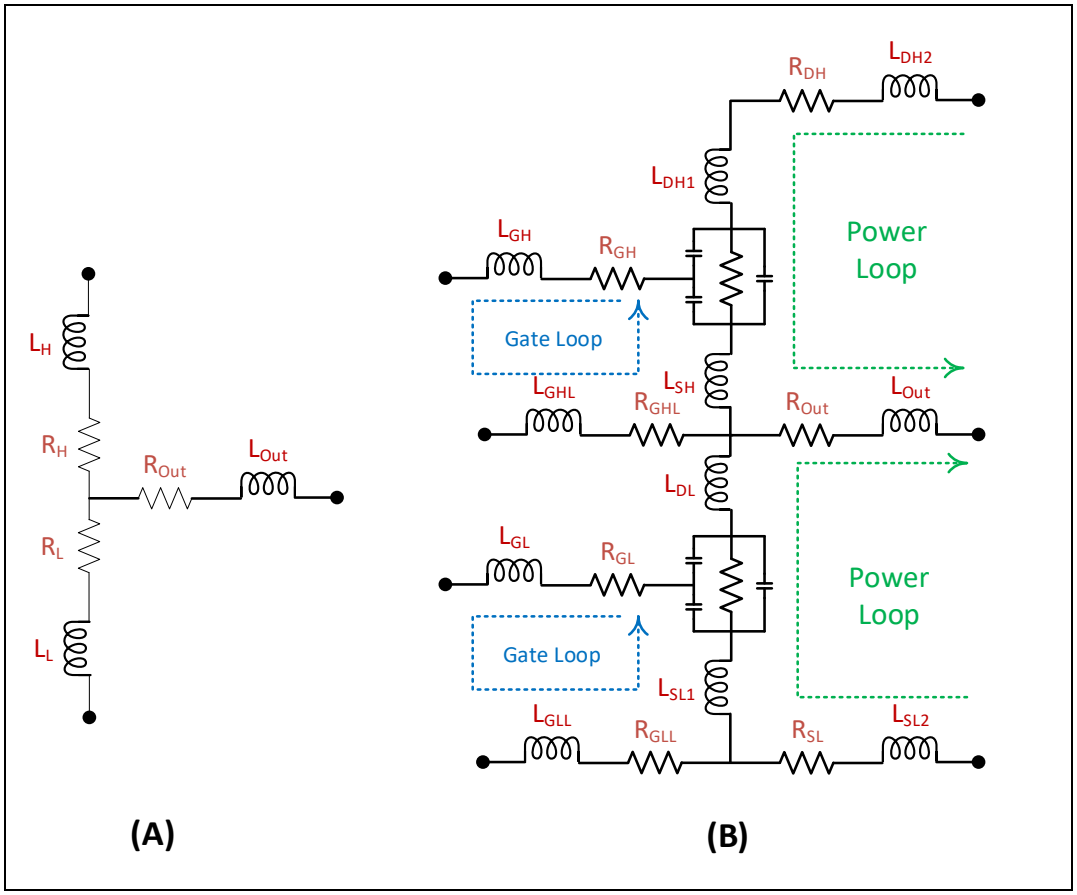

Figure 2 (A) A simplified circuit model, (B) An equivalent model of a half-bridge with gate loop

It is important to note that the model takes into account the internal structure of the device. During the switching transition, a surge of drain-to-source voltage (V_{DS}) occurs due to the resonant interaction between parasitic inductance and capacitance. This surge increases the power loss and creates adverse EMI effects. Minimizing parasitic inductance is crucial to reducing this VDS surge. Additionally, the high-side and low-side devices periodically form a short circuit, indicated by Id on the low side and ID on the high side, oscillating in antiphase with nearly equal absolute values.

The next chapter will discuss the impact of parasitic inductance by analyzing and comparing parasitic inductances in the conventional half-bridge configuration through simulation.

3 Impact of parasitic elements

This chapter provides an exhaustive **analysis of the impact of parasitic elements, leveraging the comprehensive capabilities of the SIMetrix simulation tool.** Through this detailed analysis, we aim to refine the circuit layout and gain a thorough understanding of the voltage and current waveform dynamics during switching events.

Parasitic elements like inductance, resistance and capacitance in a PCB design becomes critical when paralleling multiple discrete devices like MOSFETs, IGBTs, or diodes because they will introduce unwanted behaviors that affects circuit performance like uneven current sharing, switching noises, thermal unbalance, and some signal integrity problems. Figure 3 and Figure 4 shows the key four important parasitic elements in circuit.

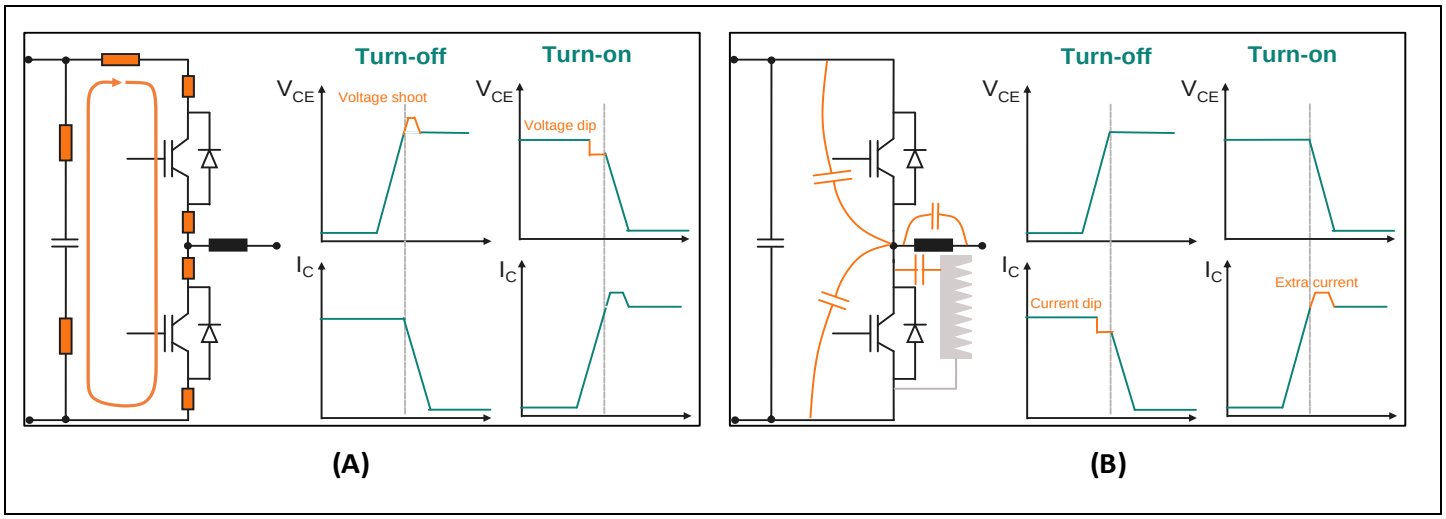

Figure 3 (A) Commutation loop inductance, (B) Midpoint capacitance

Commutation loop inductance refers to the inductance present in the circuit loop which is involved in switching. It plays a crucial role in switching performance by determining the voltage and current behavior during turn-on and turn-off phase. During turn-off the current through the commutation loop stops due to the loop inductance which causes voltage overshoot across the switch. On the other hand, during turn-on the inductance resist the rapid rise if current, leading to voltage dip across switches leading to circuit instability.

Midpoint capacitance refers to the parasitic capacitance that exists between midpoint of two switches and the ground or other circuit elements like PCB layout traces and ground, or nearby passive components. During the turn-off the capacitance slows down the voltage rise as it charges during the transition, the current will see a dip due to the discharge of the capacitance. On the other hand, during turn-on the midpoint capacitance resists the voltage change and cause uneven voltage between parallel device due to the charge and discharge of the capacitance there will be current overshoot leading to stress on the devices or increased losses.

Inductive feedback refers to the unwanted voltage spikes due to the influence of the parasitic inductance. This effect is significant when current flowing through the inductance changes rapidly. This can be mitigated by optimizing the PCB layout or right choice of the package will play an important role. In a 3-pin package, the emitter terminal is shared between the gate loop and power loop, the voltage induced in this path feeds back into the gate-emitter voltage which controls the switching. On the other hand, 4-pin package or a package with kelvin emitter provides an isolated connection between the gate loop and power loop, this ensures that the gate-emitter voltage will not affect.

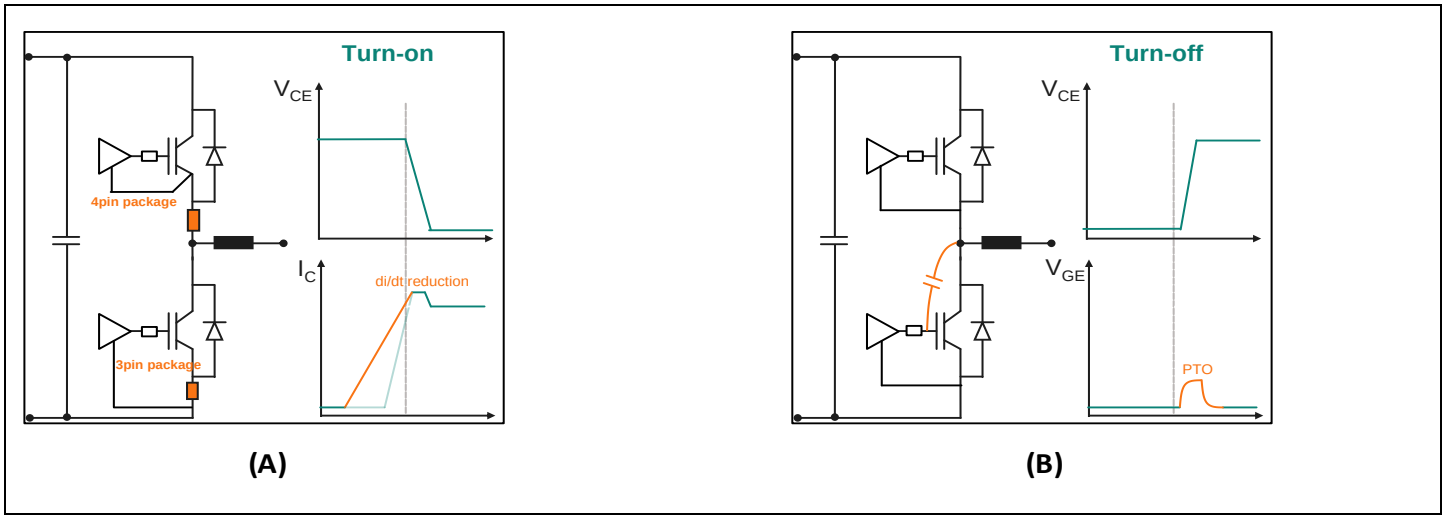

Figure 4 (A) Inductive feedback, (B) Capacitive feedback

Capacitive feedback refers to the intrinsic capacitance present between the terminals, like gate-collector capacitance and gate-emitter capacitance which couples the voltage changes between collector to gate or gate to emitter. During switching the voltage across the collector-emitter rapidly which induces a displacement current through gate-emitter capacitance. This capacitive coupling cause unwanted voltage spike leading to parasitic turn-on.

The parasitic elements are not intentionally designed into the circuit but emerge as a consequence of the physical dimensions and layout of the conductors, including PCB traces, component leads, interconnections, and loop areas. As the focus of this application note is on the power loop, our examination will be centered exclusively on the commutation loop inductance. Extensive research has elucidated the far-reaching implications of parasitic inductance in circuits, highlighting its significant influence on circuit behavior.

To demonstrate the associated effects, we will use a circuit with two discrete devices in parallel, offering a tangible representation of switching losses and current imbalance, as shown in Figure 5. These inductances can be broadly classified into three major types, providing a nuanced perspective on their impact:

- **Gate inductance** (L_G): This consists of stray inductances of driver chip, layout, and device
- **Collector inductance** or converter loop inductance (L_C): This consists of stray inductances of the DC-link capacitor, layout, and device
- **Common-emitter inductance** (L_E): This is the trace between the external source terminal and the source pad of the die. The package design will influence the L_E if the 4-pin devices with Kelvin emitter are used. In that case, L_E will reduce

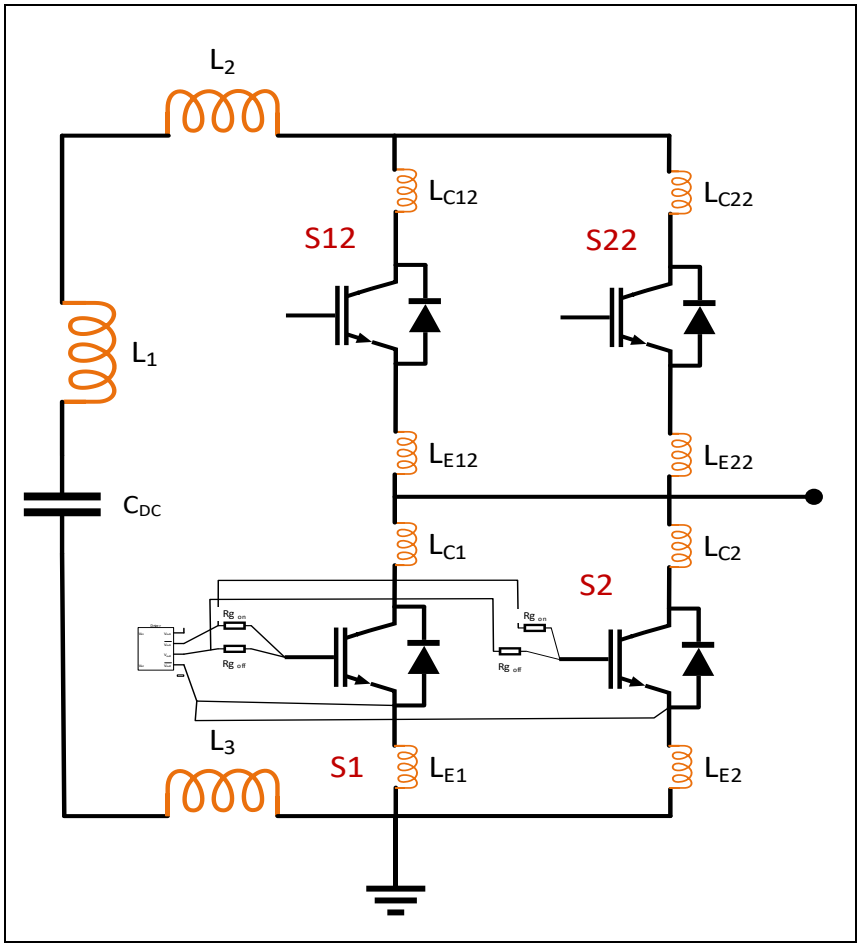

Figure 5 Influence of the parasitic inductance L_E, L_C, and L_G in a half-bridge circuit

In the field of electronics, it is widely acknowledged that the proximity of the gate driver to the transistor is essential for minimizing the likelihood of resonance phenomena associated with inductors and capacitors, which are generated by gate inductance and capacitance. While this application note primarily focuses on the design of the power loop, it is imperative to consider the following key recommendations for the gate loop design:

1. Adoption of a Unipolar Gate Driver: It is recommended to employ a unipolar gate driver to eliminate variations in $V_{GE(th)}$ throughout the operational lifetime of the device. The application of a negative gate voltage may induce stress on the gate oxide, thereby jeopardizing the reliability and longevity of the transistor.

2. Utilization of a Discrete Active Clamp (BJT): Rather than utilizing a gate driver with an integrated active clamp, it is advisable to implement a discrete active clamp employing a BJT placed in close proximity to the gate. This approach facilitates enhanced control over critical design parameters, such as clamp voltage and timing, thereby leading to a more customized and effective configuration for the gate loop.

By adhering to these design principles, one **can significantly improve the reliability and efficiency of electronic circuit designs.**

3.1 Impact of collector inductance in paralleling

In circuits with power devices, the switching process involves different stages, including a delay period, change in current over time (di/dt) period, change in voltage over time (dv/dt) period, and oscillation period. During the di/dt period for a field-effect transistor, the current flowing through the channel is affected by the gate-to-source voltage. The voltage in the gate loop depends on the gate-driver voltage and gate-loop circuit parameters. The collector

current includes both the channel current and the displacement current through the output capacitance. Ensuring that the gate driver and gate loop components are the same helps in balancing the drain current during the di/dt period.

The role of collector inductance is important in parallel IGBT operation, especially during switching events. The main effects of collector inductance include the following:

- During switching transitions, especially at turn-off, the current passing through the collector encounters parasitic inductance. According to Faraday's law, any change in current (di/dt) induces a voltage across the inductance. In parallel configurations, the devices switch at the same time, and any differences in the collector inductance between the devices can cause varying voltage spikes. Collector inductance can lead to overvoltage conditions on certain IGBTs, potentially exceeding their voltage ratings and causing breakdown
- Differences in collector inductance among paralleled devices can result in marginal uneven current distribution. Loop with lower collector inductance exhibit faster current rise due to reduced impedance during switching event, on the other hand the loop with higher collector inductance causes current imbalance or slower current decay and prolonging the conduction period. This uneven current distribution can lead to thermal imbalances
- Collector inductance, especially in high-speed switching applications, can contribute to higher levels of EMI. The high-frequency voltage spikes caused by the interaction of collector current with parasitic inductance creates an electromagnetic noise that can affect other components in the circuit or nearby systems. The elevated EMI makes it more challenging to comply with electromagnetic compatibility (EMC) standards, especially in automotive and industrial applications

External coupling gate-collector capacitance (C_{gc}) contributes to the ringing caused by the device and PCB layout. This external capacitance, along with parasitic inductances, induces resonance, leading to gate oscillation during rapid device switching. This can result in gate oscillations during turn-on and turn-off, potentially causing gate oxide damage or impairing the EMI performance. Therefore, reducing external coupling C_{gc} is important to minimize gate oscillations.

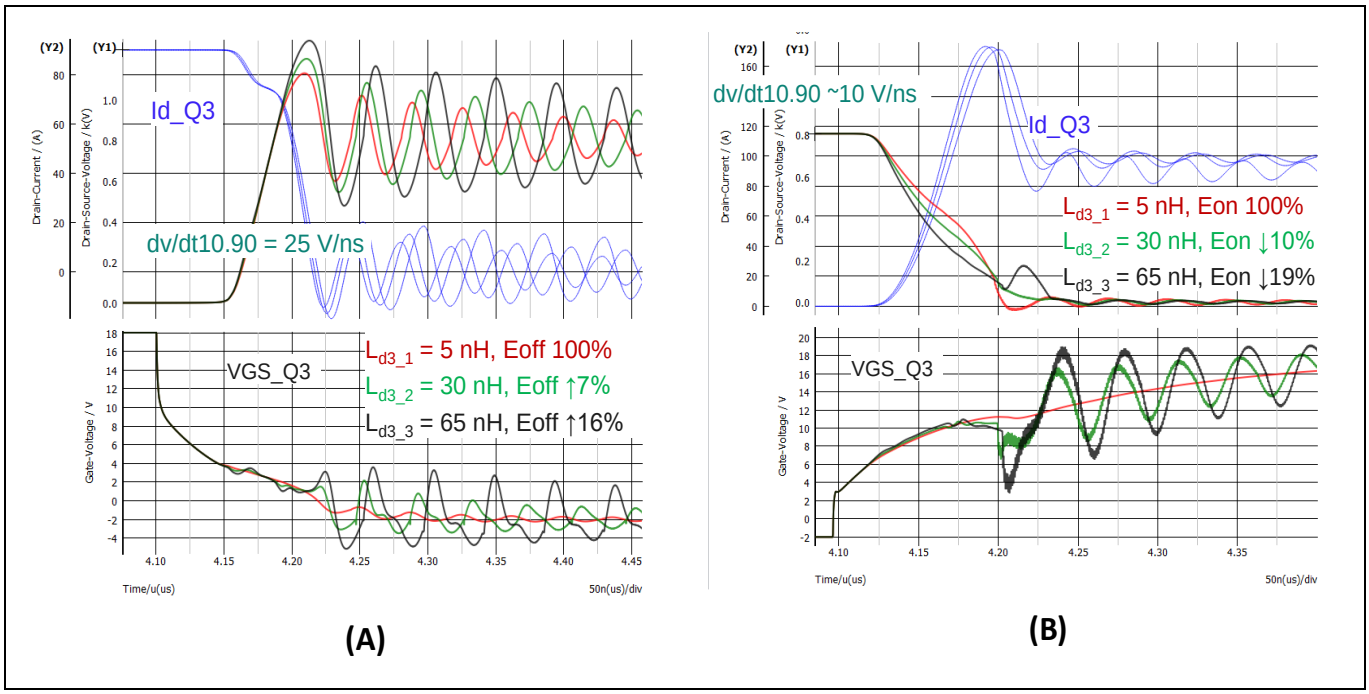

Figure 6 Asymmetry in drain inductance (A) Turn-off (B) Turn-on

Simulation results under different L_c (5 nH,30 nH, and 65 nH) connections and same L_E (5 nH) connections are shown in Figure 6. The results highlight a 16% increase in turn-off losses at 65 nH compared to a system with 5 nH on the collector side due to the reduced di/dt and higher voltage overshoot at increased L_c, on the other hand during turn-on there is a reduction of 32% in losses at increased L_c this is due to the voltage drop during current rises.

Furthermore, L_c significantly influences the current sharing during the turn-on stage. The inductive clamped circuit causes the device collector current to ascend before experiencing a drop in the collector-emitter voltage. This yields two cross points between the collector current of the paralleled devices due to the dv/dt feedback via parasitic components. Devices with reduced L_c exhibit a larger current during the di/dt period, a smaller current during the dv/dt and transition period, and a larger current during the steady state.

3.2 Impact of emitter inductance in paralleling

The operation of paralleled IGBTs is significantly influenced by emitter inductance, directly impacting the gate drive signal and switching behavior. Source inductance leads to voltage drops during high-current switching events, causing a dynamic impedance that resists changes in the gate-emitter voltage (V_{GE}). Consequently, this results in varied gate voltages for each IGBT, impeding switching transitions and causing imbalanced current sharing in a parallel configuration.

The prolonged presence of both current and voltage, attributable to delayed switching caused by source inductance, amplifies switching losses, particularly in high-frequency applications, ultimately impacting system efficiency. Delayed switching due to emitter inductance can also result in nonuniform heating, worsening current-sharing imbalances, and potentially triggering a thermal runaway. In a thermal runaway, the IGBT experiencing higher current undergoes increased on-state resistance and subsequent heating, culminating in device failure. Additionally, emitter inductance may induce gate-drive signal oscillations, resulting in noisy switching behavior, increased EMI, and reduced system efficiency.

The parasitic inductance on the emitter side of the switching devices is an integral part of the commutation loop, particularly with respect to the switch and ground. Its significant impact on performance is demonstrated by delays in switching events and timing mismatches between devices, leading to elevated switching losses. In high-power circuits, the influence of parasitic inductance in both emitter and collector paths on circuit performance is conspicuous, with emitter inductance assuming heightened criticality. It directly influences the rise and fall times of collector current, with its effect being directly proportional to the total emitter inductance.

The specified variation of 60 nH in L_E within two paralleled branches was validated through a simulation, results of which are shown in Figure 7. It is noteworthy that during the turn-on period, due to the current imbalance resulting from L_E mismatch, L_{E1} carries more current, but during the turn-off period, it carries lesser current than L_{E2}. This imbalance gradually diminishes as the paralleled circuit reaches a steady-state condition. When the difference in inductance between branches is around 60 nH, the turn-off losses can increase by approximately 120%. On the other hand, the turn-on losses at higher L_E (65 nH) will be 70% lower due to the slower switching behavior caused by the negative feedback loop which reduces the effect of V_{GE} reducing the current slew rate.

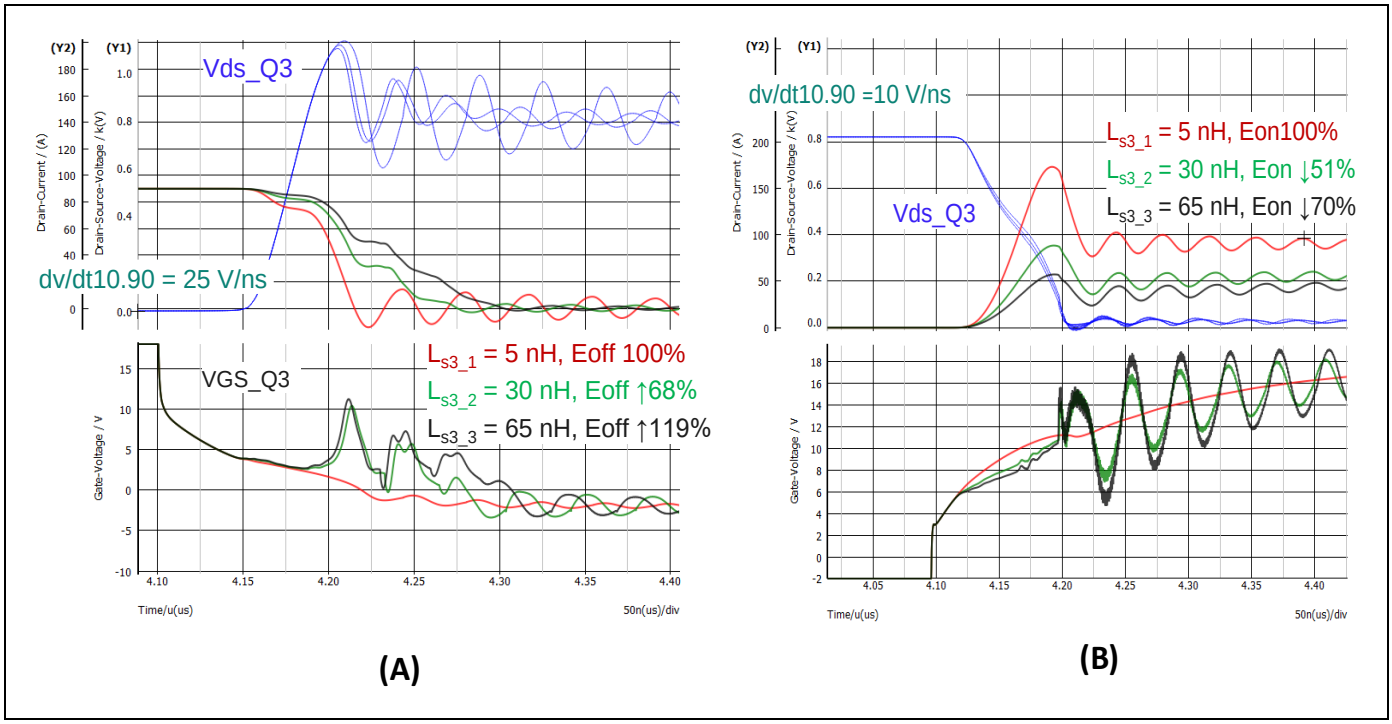

Figure 7 Asymmetry in source inductance (A) Turn-off (B) Turn-on

When IGBTs are paralleled, the interaction between the emitter and collector inductances can amplify current imbalance issues. If either the emitter or collector inductance is different between the paralleled devices, it causes variations in both the gate drive voltage and the current paths. These variations lead to unequal switching characteristics and unbalanced current sharing. For instance, if one loop has a slightly higher L_E, it will switch on slower and carry less current, while another loop with a lower L_E will switch faster and handle more current. Similarly, differences in L_C can cause uneven voltage spikes, making it harder for the devices to share current equally.

As the devices operate, this imbalance causes the IGBT carrying the larger share of the current to overheat, potentially leading to premature failure. The imbalance becomes more pronounced at higher switching frequencies, where di/dt is larger, and the effects of parasitic inductances are magnified.

To summarize, **in paralleled power semiconductor circuits, both emitter and collector inductance play a crucial role in determining the performance, reliability, and efficiency of the system**. **L_E affects the gate drive signal and switching speed, leading to imbalance in current sharing, and higher switching losses. L_C on the other hand causes voltage spikes, EMI, and further current imbalance.** A meticulous PCB design, symmetrical layouts, and mitigation techniques such as Kelvin connections and decoupling are essential to minimize the adverse effects of these parasitic inductances. By managing these inductances effectively, designers can improve current sharing, reduce thermal stress, and ensure the long-term reliability of parallel power systems.

4 Hardware description

In this chapter, we will explore the Q3D simulation technique utilized for extracting the parasitic properties of the target setup. We will also analyze the test results pertaining to the switching waveform measurements at various inductance levels.

4.1 Q3D simulation

Ansys Q3D Extractor represents a sophisticated 3D quasi-static electromagnetic simulation software tool. Its functionalities encompass the computation of fields, equivalent circuits, S parameters, inductances, resistances, and capacitances. Q3D integrates three solvers (CG, DCRL, ACRL) designed to operate within the graphical user interface (GUI) of the Ansys Electronics Desktop (AEDT) environment. Notably, Q3D is proficient in addressing the parasitic aspects of 3D arbitrary circuits, as shown in Figure 8.

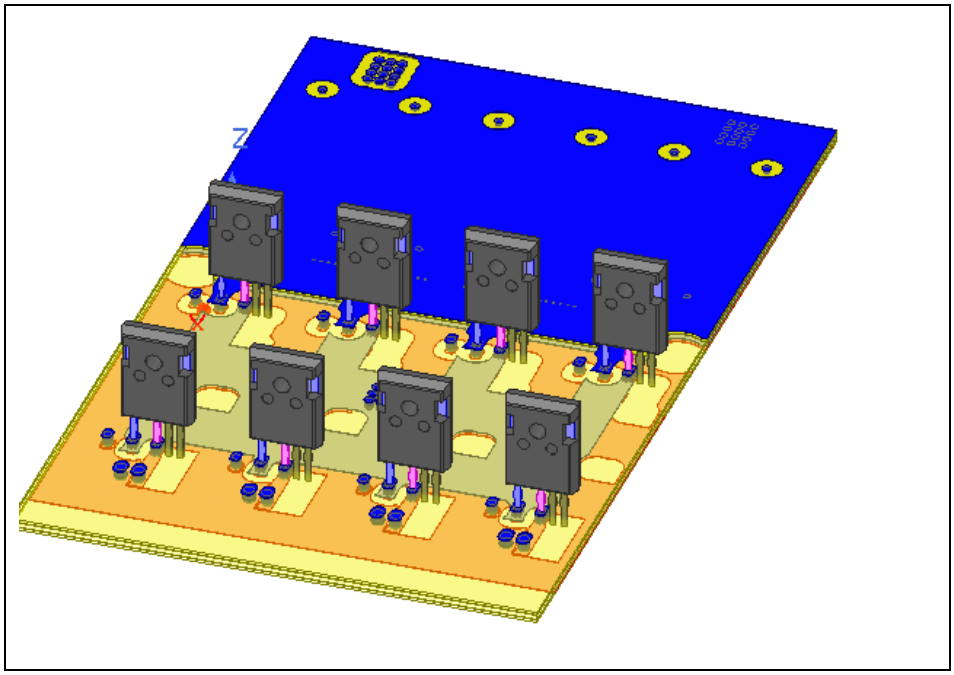

Figure 8 Q3D Extractor

The Q3D approach leverages a surface grid for effectively computing the high-frequency parameters of conductive structures, thus enabling the extraction of frequency-dependent inductance, resistance, and capacitance. This methodology is particularly applicable in quasi-static field scenarios [6]. When modeling partial inductances, the Q3D Extractor distinguishes between distinct current paths defined by the position of the devices. This covers capacitive coupling between nets and the self-capacitance of a net with respect to ground, while omitting the modeling of distributed capacitance within a single net. Q3D excitation ports are represented as equipotential surfaces, defining each current path relating to a Q3D net between the two ports.
In our modeling exercise, we utilized a half-bridge board featuring four devices in parallel, as shown in Figure 9. Employing the Q3D Extractor, we constructed a 3D geometry model of the board to determine the inductance [L] and resistance [R] of the commutation loop between the DC+ and DC-terminals. The aggregate inductance and resistance of the current path between DC+ and DC-were simulated through the modeling of TO-247 4-pin devices in a half-bridge configuration. To compute the distributed inductance and resistance in Q3D, the current path was subdivided into three sub paths: L_{DC}+, Lout, and L_{DC}-.

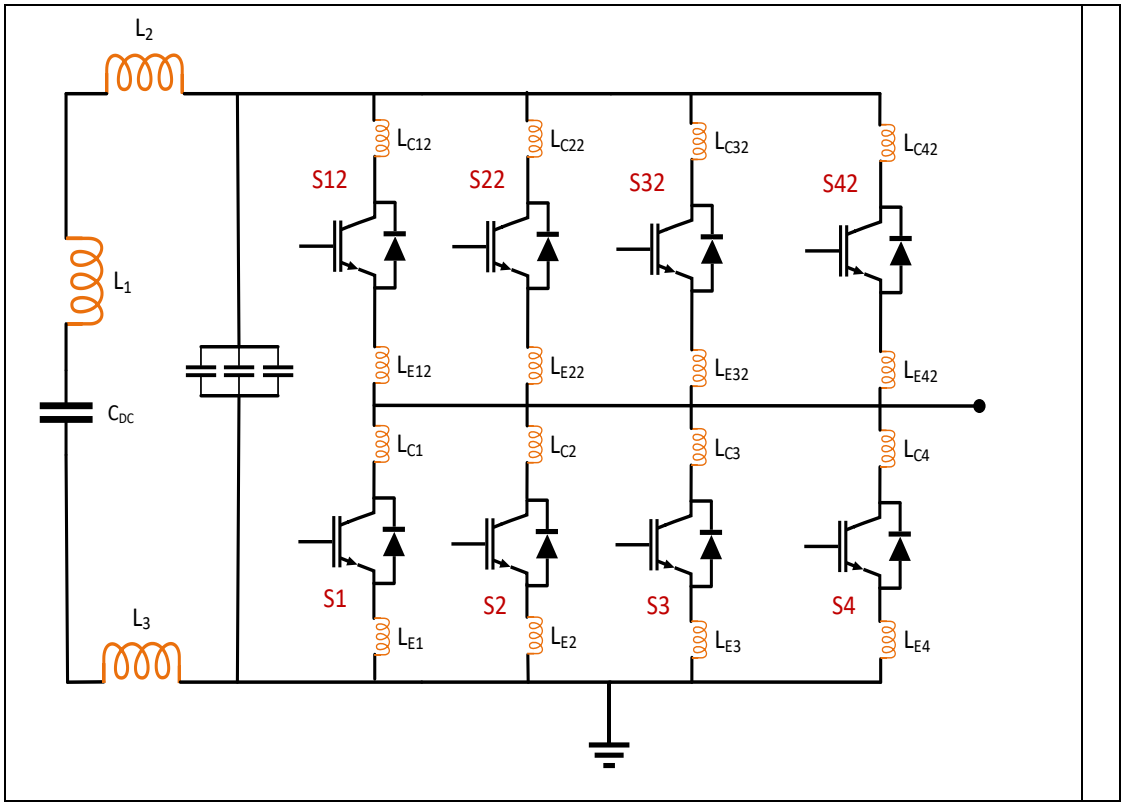

Figure 9 Parasitic inductance in half-bridge 4 x parallel design

The two inner switches, Q12-Q2 and Q42-Q3, have a symmetrical layout design. The two outer switches, Q1-Q22 and Q4-Q32, have a slightly higher parasitic inductance compared to the inner switches. The extracted parasitic inductance of the test setup is shown in Figure 10. From the chart, the layout can be divided into inner (second leg and third leg) and outer paths (first leg and fourth leg) with respect to DC+, DC-, and output. The parasitic in the inner path of L_{DC}+ (high-side collector to DC+) is 17.83 nH, L_{DC}- (low-side emitter to DC-) of 38.77 nH, and L_{OUT} (output to midpoint) is 17.55 nH. For the outer path of L_{DC}+ (high-side collector to DC+) is 22.54 nH, L_{DC}- (low-side emitter to DC) is 43.48 nH, and L_{OUT} (output to midpoint) is 23.79 nH.

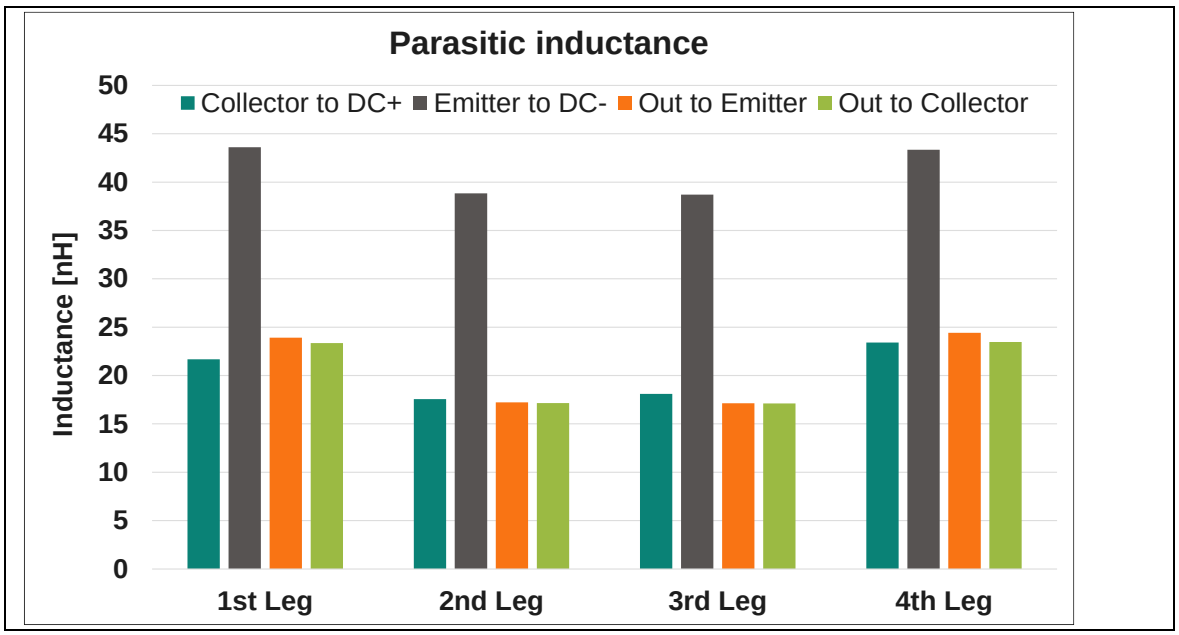

Figure 10 Extracted parasitic inductance of different legs in a paralleled board at 1 MHz

4.2 Current hardware

To evaluate high-power applications, a half-bridge system with parallel discrete devices, as shown in Figure 11, was used to examine the current sharing, switching performance, and thermal management. This configuration includes four high-side and four low-side switches connected in parallel to handle rising currents effectively. The gate driver circuit is designed to accommodate either a single stand-alone device or multiple devices operating simultaneously. To regulate the switching speed and minimize oscillations, individual turn-on and turn-off resistors are integrated. DC-bus capacitors were placed near the IGBTs to filter voltage spikes and reduce ripples. The current through each device can be measured using an individual shunt or sensor.

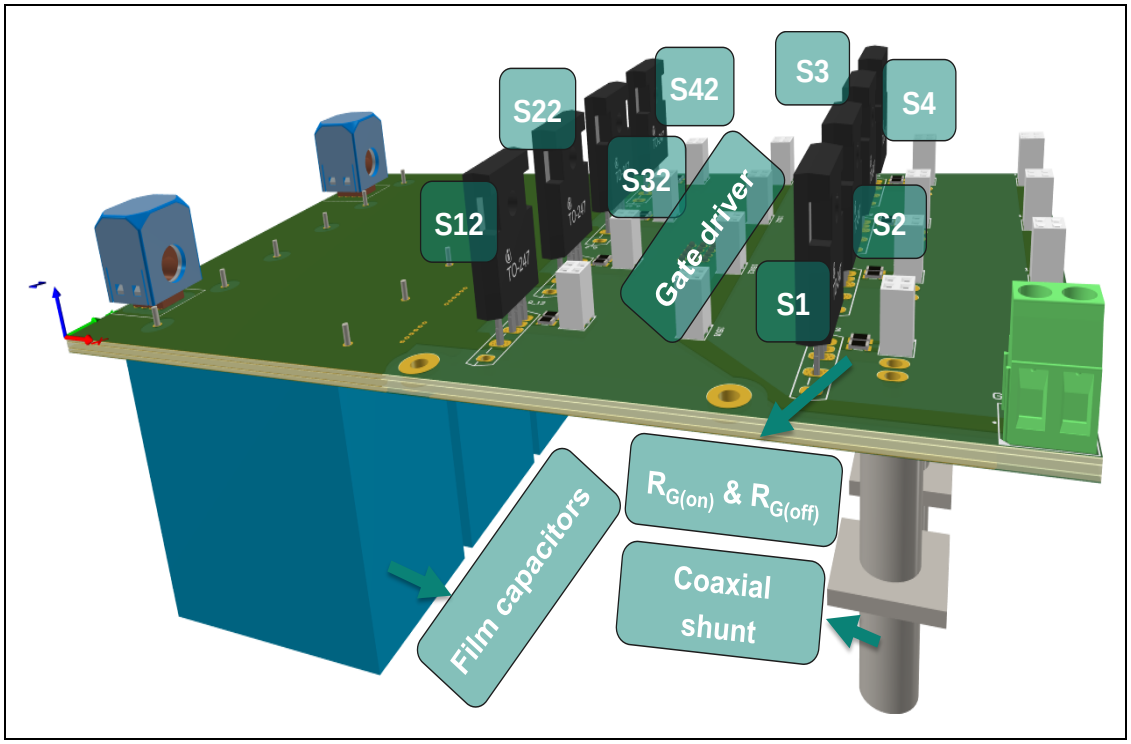

Figure 11 Test setup with four devices in parallel

The circuit parameters are listed in Table 1. To understand the switching behavior of the paralleled devices, the layout is divided into inner and outer paths. This division helps in observing the turn-on and turn-off switching behavior under different operating conditions.

Table 1 Circuit parameters

Parameter	Symbol	Value
Gate-resistor turn-on	$R_{G(on)}$	6 Ω
Gate-resistor turn-off	$R_{G(off)}$	6 Ω
DC-bus capacitance	C_{DC}	220 uF
DC-bus supply voltage	V_{DC}	600 V
Gate-driver supply voltage	V_{GE}	15 V
Case temperature	T_{case}	25°C

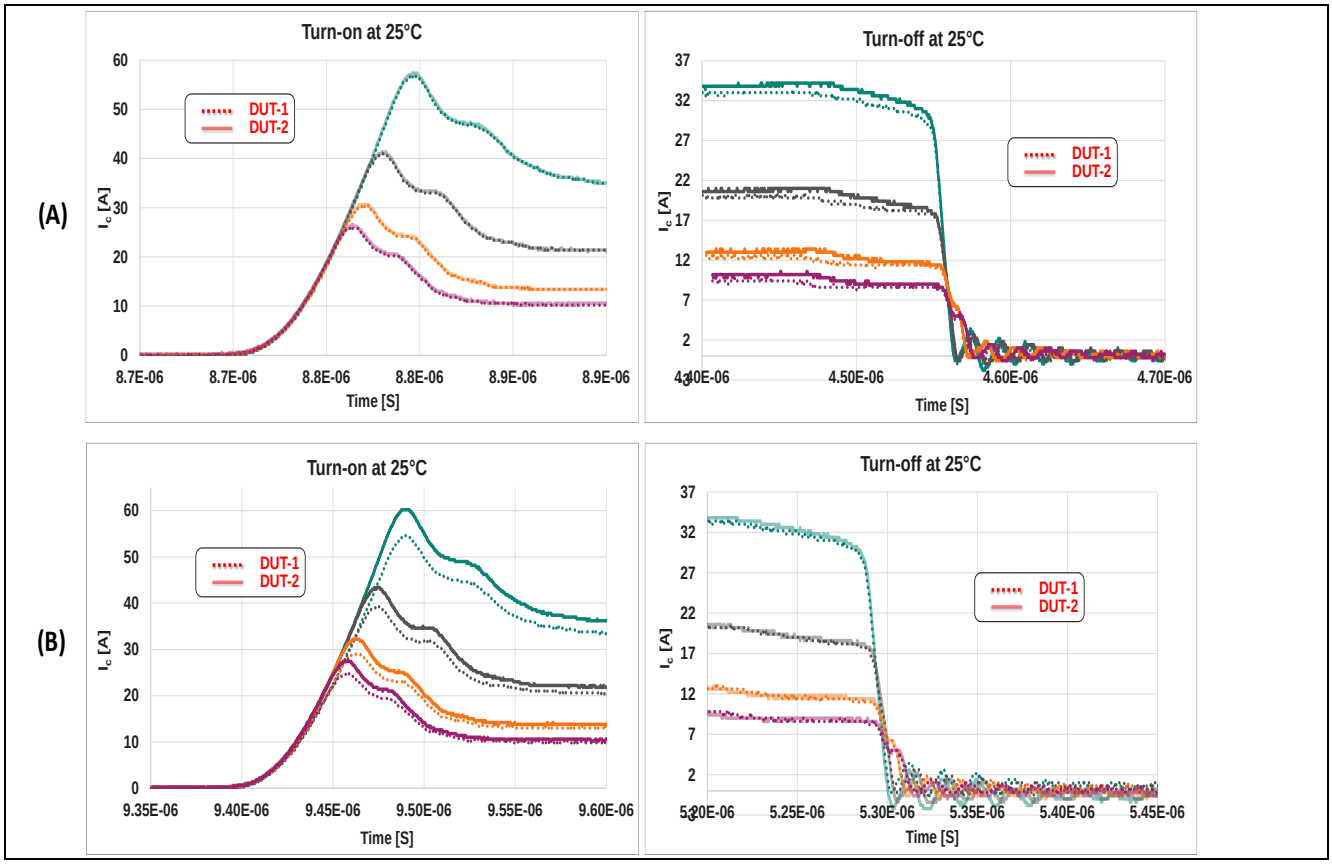

Figure 12 (A) Symmetrical layout turn-on and turn-off (B) Asymmetrical layout turn-on and turn-off

Figures 12 and 13 offer detailed insights into the performance of two devices under test (DUTs) with different layouts (symmetrical and asymmetrical) for turn-on and turn-off operations at 25°C during switching events. Figure 12 showcases the distinctive current profiles of DUT 1 and DUT 2 during turn-on and turn-off operations. The asymmetrical layout exhibits notable differences in current profiles compared to the symmetrical layout, with DUT 2 demonstrating a higher current-handling capacity than DUT 1. These differences in current profiles can potentially have implications on the long-term reliability and losses of the devices.

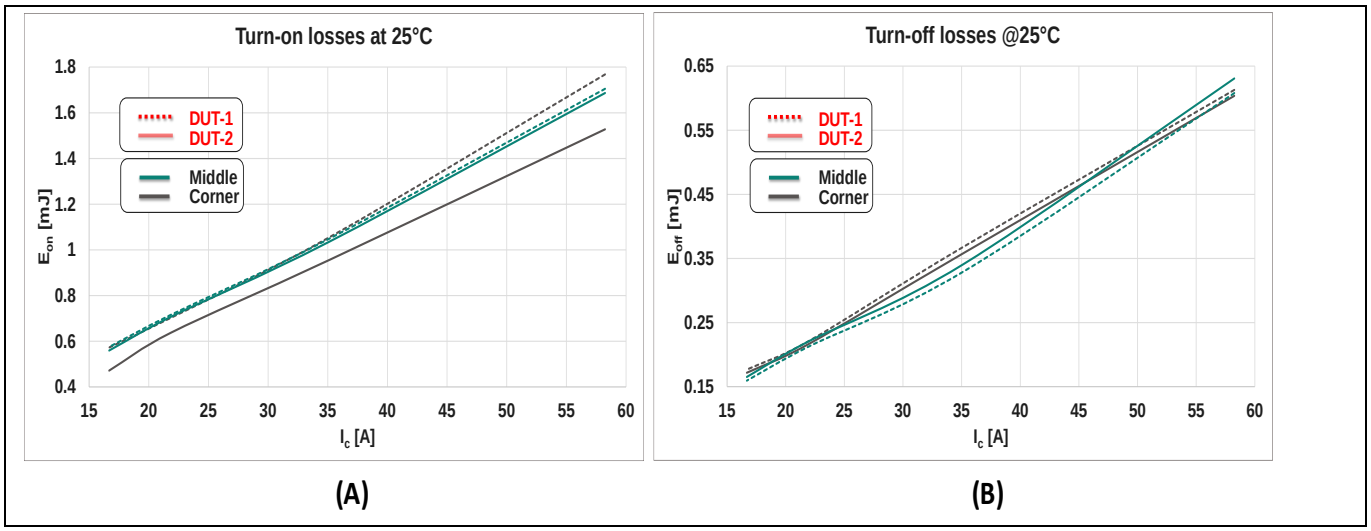

Figure 13 (A) Turn-on losses (B) Turn-off losses

Figure 13 provides a detailed breakdown of the turn-on and turn-off losses of the DUTs at 25°C. The DUTs were tested in two different positions: “Middle” (symmetrical layout) and “Corner” (asymmetrical layout). The results indicate that turn-on losses are more sensitive to inductance than turn-off losses. Also, the turn-on losses of the asymmetrical layout are higher with the collector current for both DUTs.
In summary, both sets of data highlight the influence of layout configurations and inductance on the energy efficiency and performance of the DUTs during switching operations. This information underscores potential areas for optimizing the designs and layout of power devices to enhance overall performance and reliability.

5 Customized designs

In this chapter, we will explore how parasitic inductance can significantly impact the performance of two custom-made designs. Both these designs use four separate devices working together. We will also analyze the parasitics that we have figured out using Q3D. Through custom designs, we hope to give a clear picture of how this inductance affects our designs.

5.1 PCB layouts

When designing **PCBs for paralleling power semiconductor devices, such as MOSFETs and IGBTs, the layout plays a critical role in ensuring optimal performance, reliability, and efficiency**. Different PCB layout strategies can significantly influence the current sharing, switching behavior, thermal management, and electromagnetic compatibility (EMC) of the paralleled devices. The various PCB layout strategies for paralleling power devices, along with their advantages, challenges, and considerations are as follows:

Symmetrical layout

The symmetrical layout ensures that each paralleled device has an equal-length electrical path and identical parasitic elements (resistance, inductance, and capacitance). This layout strategy is essential to balance the current sharing and reducing parasitic imbalances. All devices should have equal trace lengths for their gate, source, and drain connections to minimize discrepancies in switching times. The layout should mirror components on either side of a central point to maintain symmetry. The traces connecting the power devices to the power buses (for the drain) and the ground (for the source) should have similar parasitic inductance.

Symmetry ensures that each device experiences similar electrical conditions, leading to a more uniform current sharing. Equal trace lengths minimize gate delays and ensure synchronized switching, reducing stress on individual devices.

Symmetrical layouts can require more space on the PCB, especially for high-current applications, which may not always be feasible in compact designs. Maintaining symmetry across multiple PCB layers can be challenging.

Star layout

In the star layout, the power bus (drain/collector) and ground (source/emitter) connections are routed from a central point, with equal-length traces radiating outward to each paralleled device. This ensures that all devices have an equal electrical path to both the power supply and the ground. A single central point serves as the hub for the power and ground connections to all devices. Equal-length traces from the central point to each device minimize variations in parasitic inductance.

The star layout minimizes path imbalances, ensuring uniform current distribution. The centralized power and ground points make it easier to add or remove devices in parallel without significantly affecting the system performance.

Routing traces from a central point can lead to a congested PCB layout, particularly in systems with many parallel devices. This layout may not use the PCB real estate efficiently, especially in high-density designs.

Kelvin source layout

In the Kelvin source layout, a separate source connection is provided specifically for the gate drive signal, distinct from the main power current-carrying source connection. This helps isolate the gate drive from the high-current switching paths, reducing the impact of parasitic inductances on the gate signal. Each MOSFET has two source connections – one for the gate drive circuit and one for the main current path to the power bus. The gate drive signals experience minimal interference from the switching current, thus improving the switching performance.

By isolating the gate drive from the source current path, the layout minimizes the parasitic inductance seen by the gate driver, reducing gate-source voltage variations (gate bounce) during switching. The gate drive circuit is less affected by high di/dt currents in the main power path, allowing for faster and more stable switching transitions.

The Kelvin source layout requires additional routing for the separate source connections, which can complicate the PCB design. The need for separate source connections increases the space required on the PCB, making it less compact.

Busbar layout

The busbar layout involves large, low-impedance metal bars or planes to distribute current to the paralleled devices. Busbars provide very low inductance and resistance paths, making them ideal for high-current applications. Thick, wide metal bars (usually copper) are used to connect the power and ground terminals of the paralleled devices. The large cross-sectional area of the busbars minimizes the parasitic inductance and resistance compared to traditional PCB traces.

Busbars offer highly efficient current distribution with minimal voltage drops and heat generation. The low inductance and resistance make busbars suitable for very high current applications where standard PCB traces would be inadequate.

Integrating busbars into a PCB layout requires careful mechanical design and can complicate the assembly process. The use of thick copper busbars increases material costs, especially in large-scale productions.

Distributed layout

In the distributed layout, the paralleled devices are spread out across the PCB, with multiple smaller parallel groups rather than a single large one. Each group has its own local decoupling capacitors and gate drivers, distributing the switching and thermal load more evenly across the board. Devices are grouped into smaller parallel clusters with independent gate-drive circuits and decoupling capacitors. Each group also has localized power planes and capacitors to minimize the parasitic inductance and resistance in the power paths.

By distributing the devices across the PCB, heat is spread more evenly, reducing the risk of hotspots. The smaller groups have shorter power paths and more localized decoupling, reducing the effects of parasitic inductance on current sharing.

Distributing the devices requires careful planning to avoid long traces, which could introduce additional parasitic elements. Ensuring that all paralleled groups switch at the same time requires precise synchronization of the gate-drive signals.

Selecting the right PCB layout strategy for paralleling power devices depends on various factors, including current levels, switching frequency, thermal requirements, and system complexity. **Symmetrical layouts and star configurations are ideal for maintaining balance and equal current sharing, while busbars and multilayer PCBs offer low inductance paths for high-current systems. Kelvin source connections and distributed layouts help improve switching performance and thermal management**. By carefully choosing and optimizing the layout strategy, designers can minimize parasitic effects, reduce power losses, and ensure reliable operation in paralleled power device configurations.

5.2 Custom design 1 versus custom design 2

In the domain of PCB design for paralleling power semiconductor devices such as MOSFETs or IGBTs, the impact of parasitics holds significant importance in determining the system’s performance, reliability, and efficiency. These inherent parasitic elements, stemming from the physical structure of the PCB encompassing traces, vias, and components, exhibit heightened effects in high-power, high-frequency, or high-speed switching applications.

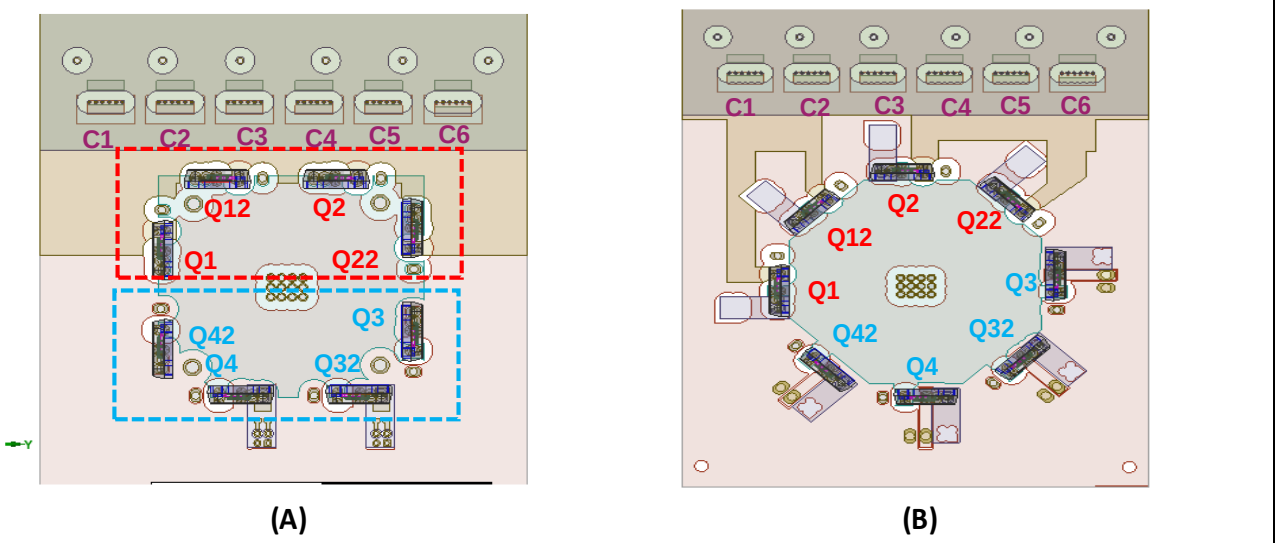

Figure 14 (A) Custom design 1 (B) Custom design 2

A detailed Q3D extraction was undertaken to analyze the parasitic inductance and capacitance in two distinct custom-designed PCBs, each accommodating four devices in parallel. These designs, namely custom design 1, and custom design 2, are visually represented in Figure 14. Custom design 1 adopted a rectangular configuration, while custom design 2 featured a circular configuration.
For applications characterized by moderate parallelism, such as power converters or battery management systems, in which maintaining uniform current distribution is paramount, a star layout was implemented.
The analysis included an examination of the high-side devices Q1, Q12, Q2, and Q22, as well as the low-side devices Q4, Q42, Q3, and Q32. Using the Q3D simulation, the parasitic inductance originating from the coupling capacitor to the collector, emitter, and output side was carefully determined. The findings from the simulation are shown in Figures 15, and 16.

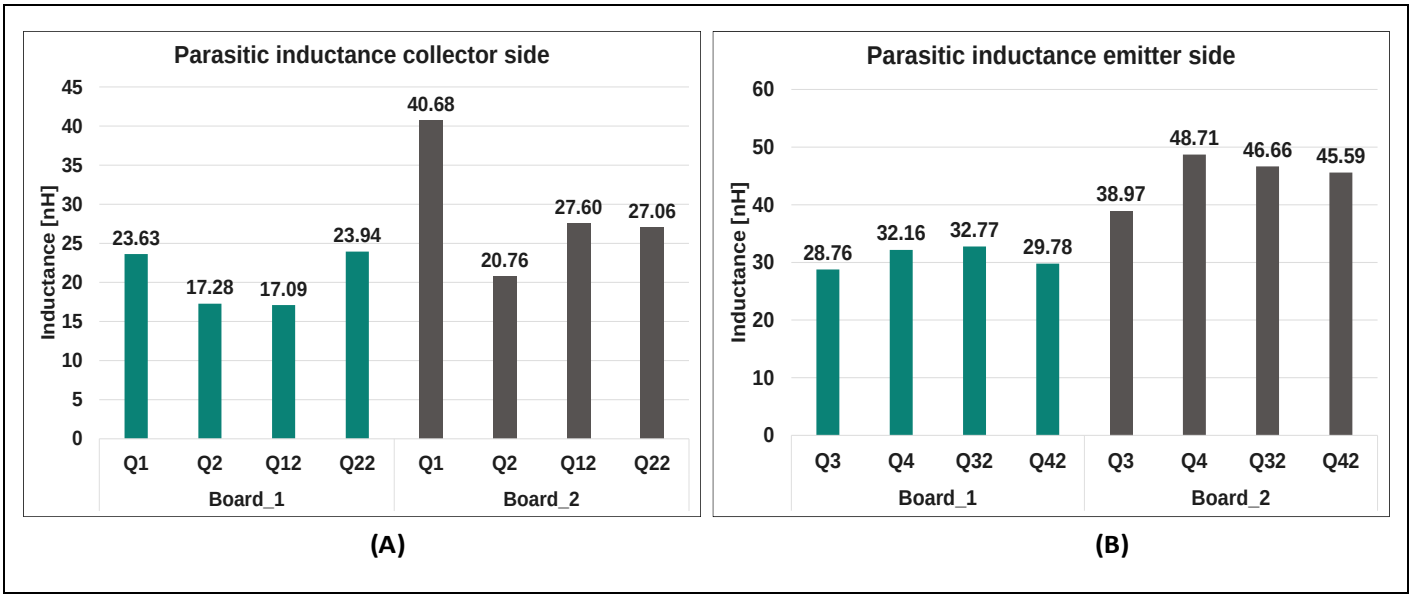

Figure 15 Extracted parasitic inductance from (A) high-side collector to the coupling capacitor (B) low-side emitter to the coupling capacitor

Figure 15 (A)shows the parasitic inductance extracted from the high-side collector to the coupling capacitor. It was observed that Board 1 had lower inductance and better symmetry between switches, with a 5 nH difference between switches. On the other hand, Board 2 exhibited a higher inductance deviation, with a 20 nH difference. These results suggest that the 5 nH inductance variation in Board 1 will have minimal impact on current imbalances, while the 20 nH variation in Board 2 could have a more significant effect. Figure 15(B) shows the parasitic inductance extracted from the low-side emitter to the coupling capacitor. As can be seen, Board 1 exhibited lower inductance and improved symmetry between switches, with a difference of 4 nH, while Board 2 displayed a higher variation in inductance, with a difference of 10 nH. These findings emphasize that Board 1 has lower inductance and a more balanced loop compared to Board 2.

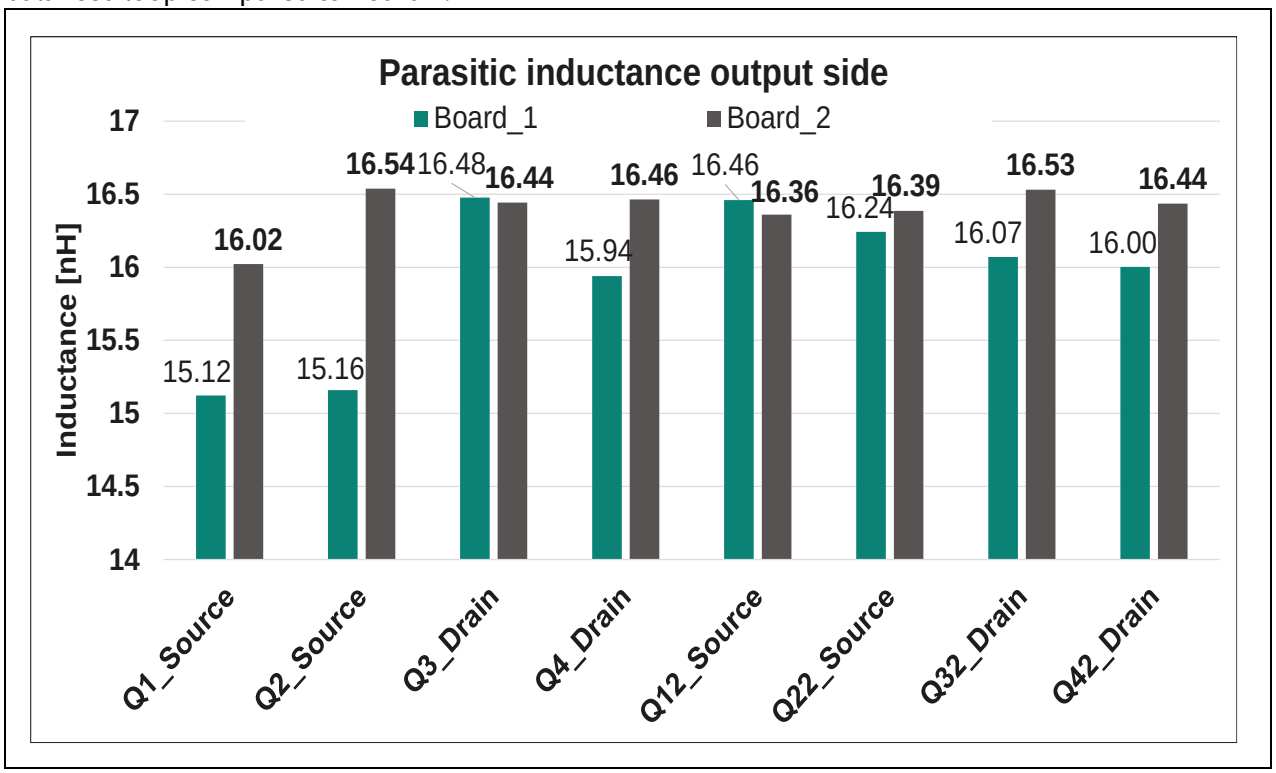

Figure 16 Extracted parasitic inductance from the high-side source to the low-side collector to output

The star layout configuration of custom design 1 and custom design 2 ensures that their outputs are perfectly centered. Figure 16 reveals that both boards have symmetrical parasitic inductance, with only a minor 1.2 nH variance in Board 1, which can be deemed negligible.

It is also evident that custom design 1 (rectangular configuration) is better suited for paralleling due to its minimal current imbalance and superior thermal behavior. The asymmetrical design and lower inductance of custom design 1 support the expectation of minimal influence on the current imbalance.

6 Impact of package

In power semiconductor devices, the choice of packaging plays a critical role in influencing performance, thermal management, and design complexity. Figure 17 shows the range of discrete packages available in the market. The standard 3-pin configuration, consisting of the collector, emitter, and gate devices, impacts system performance differently than the 4-pin configuration, which includes the collector, emitter, Kelvin, and gate elements and has the potential to enhance system performance. Incorporating a Kelvin connection can mitigate the impact of emitter inductance, leading to an improved switching and thermal performance.

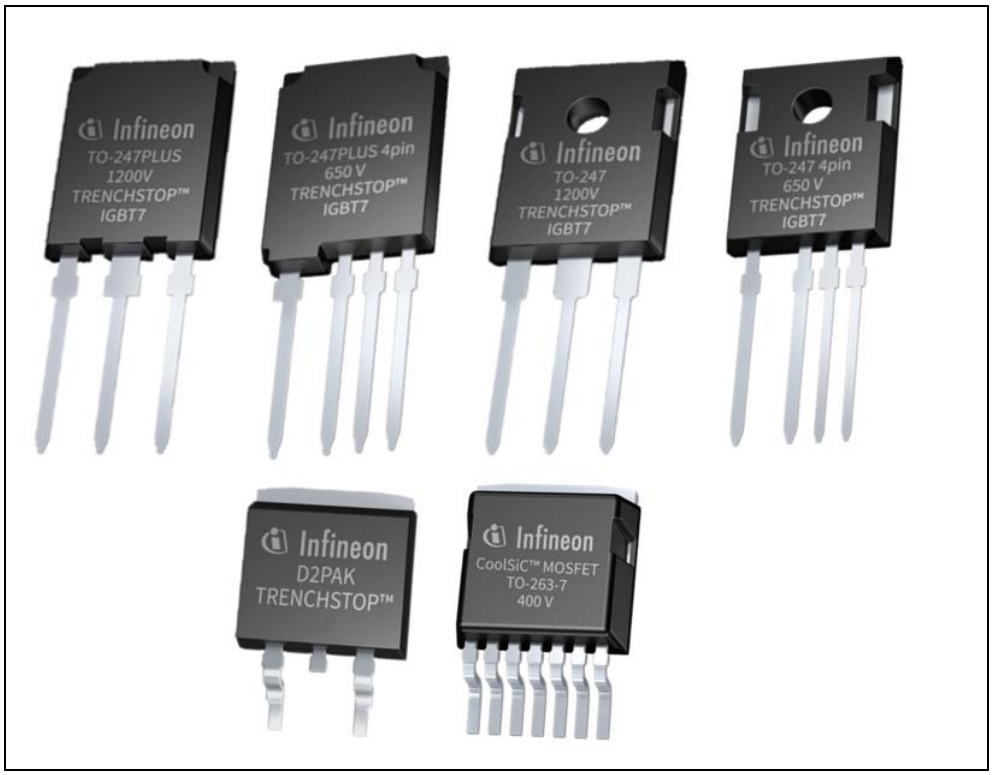

Figure 17 Discrete packages

When working with electronic components, it is essential to consider the differences among various discrete packages such as TO-220, TO-247, DPAK, and others carefully before integrating them into a circuit. These packages have distinct physical and electrical attributes that can significantly affect the overall circuit performance. It is also crucial to take into consideration the thermal resistance, parasitic inductance and capacitance, physical dimensions, installation methods, and reliability and lifespan characteristics associated with each package.
Different package types exhibit varying thermal resistances. For example, the TO-220 package generally has higher thermal resistance than the TO-247, resulting in less effective heat dissipation. Connecting components with different thermal resistances in parallel can lead to imbalances in current load distribution.
Larger packages occupy more space on the PCB and may require different heat sink configurations. When combined with smaller packages, this can complicate the PCB layout and thermal design, potentially causing uneven cooling and higher thermal gradients. Due to various thermal and electrical stress profiles, components in different packages may age at different rates. For instance, a device in a smaller package might degrade faster due to higher junction temperatures, potentially leading to early failure and unbalanced load sharing.

6.1 The TO-247 3-pin package versus the TO-247 4-pin package

In a 4-pin configuration, commonly known as a Kelvin connection, the presence of the fourth pin allows for more precise control by minimizing the influence of parasitic inductance and resistance in the main current path on the gate-drive signal. This is achieved because the gate-drive signal has a separate return path from the main current, reducing the impact of parasitic elements on the gate signal. On the other hand, in a 3-pin configuration, the gate-drive signal shares the same return path as the main current, which can lead to parasitic inductance and resistance affecting the gate signal, especially in high-speed switching applications.

These differences in configuration can result in voltage drops that affect switching performance, potentially causing slower turn-on/turn-off times and higher switching losses in 3-pin setups. This can lead to timing mismatches during parallel operation, where one device may switch slightly earlier or later than the other switches, resulting in uneven current sharing and increased stress on some components. In contrast, the 4-pin configuration with a separate gate return (Kelvin connection) minimizes the influence of the main current path's parasitic inductance and resistance on the gate-drive signal. Thus allowing for more precise switching control and more consistent performance when the components are paralleled. This setup helps reduce timing mismatches and facilitates balanced current sharing among parallel devices, mitigating the risk of one component dominating the current load.

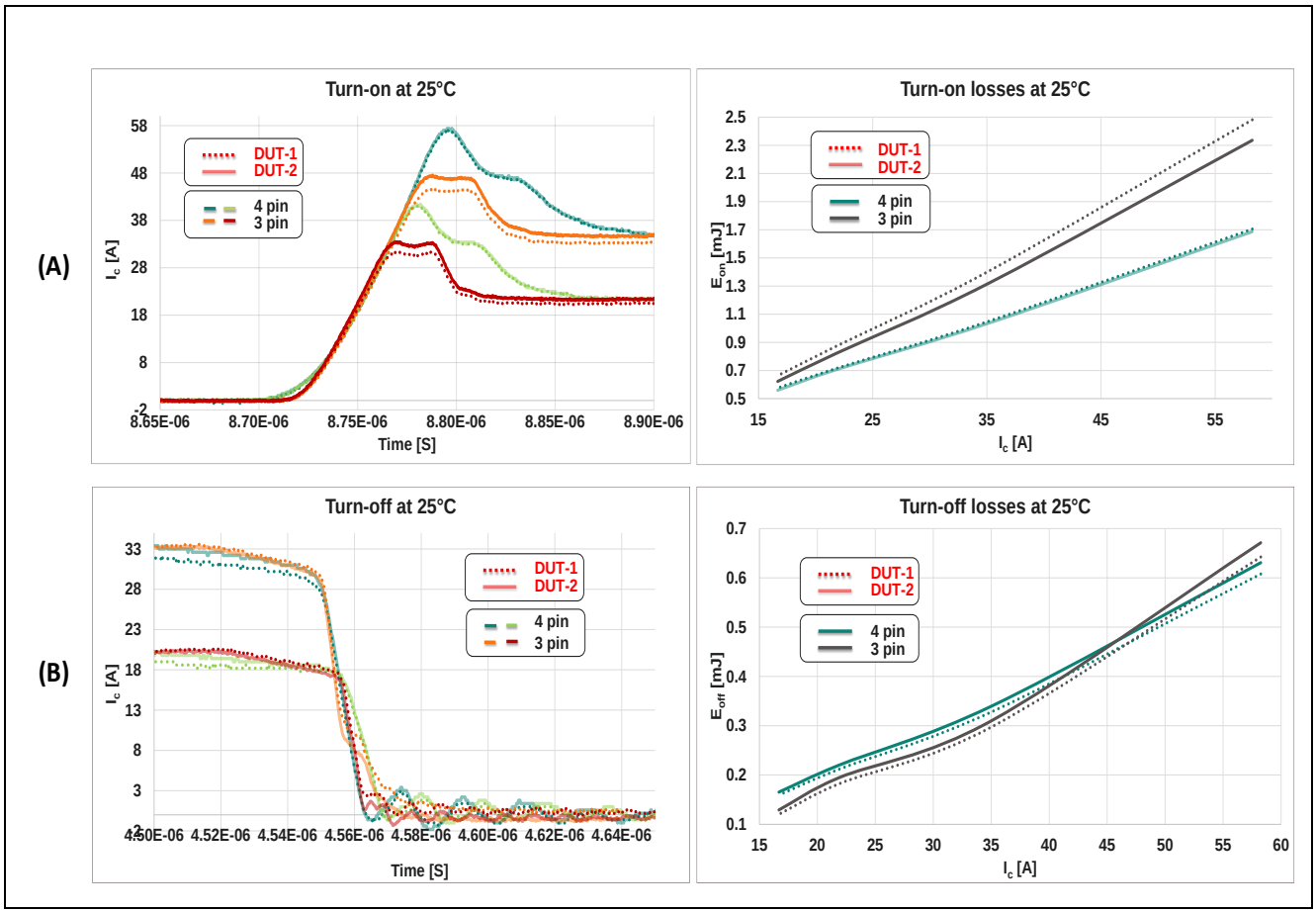

Figure 18 (A) 3-pin vs. 4-pin turn-on waveform and losses (B) 3-pin vs. 4-pin turn-off waveform and losses

A comparison of the turn-on and turn-off waveforms along with losses between the two packages is shown in Figure 18. It highlights that the 4-pin devices have symmetrical behavior between two parallel devices, while the 3-pin devices have unbalanced current, specifically during turn-on. On the other hand, there is no significant impact on the turn-off behavior.

Achieving precise control over the switching characteristics of each device can be challenging, often necessitating current-sharing resistors or other balancing techniques to achieve even distribution. **The Kelvin connection in 4-pin devices enhances the current-sharing accuracy, thus reducing the need for additional balancing components and bolstering the reliability of the parallel configuration.** Additionally, the reduced impact of parasitic on the gate signal allows for faster, more precise switching, particularly in high-frequency applications. This rapid and synchronized switching minimizes losses and enhances the thermal performance of the devices in parallel configurations.

Nevertheless, parasitic inductance and resistance in the shared return path must be considered in the gate-drive circuitry. This can potentially complicate the design and increase costs. Achieving consistent performance in a parallel configuration may require more sophisticated gate-drive solutions, especially in high-power or high-frequency applications. However, the Kelvin connection streamlines and enhances the gate-drive design by reducing the impact of parasitics and enabling a more concise gate drive, resulting in a more predictable and reliable performance. Overall, the improved gate-drive response in parallel configurations facilitates a more streamlined design and enhances system performance.

7 Conclusion

This application note describes the effect of parasitics in the layout when paralleling discrete components, highlighting the unbalance and thermal issues between parallel devices via product-level simulation and switching performance of discrete IGBTs connected in parallel in a half-bridge configuration.

Optimal performance and reliability are best achieved by using identical components. The effects of parameter distribution and the effect of gate loop layout were not in the scope of research. Nevertheless, there are some common factors that should be followed in the gate loop during paralleling to avoid any mismatches between the devices

- gate driver should be placed as close as possible to reduce the potential resonance from the gate loop
- common gate resistors are required to balance the gate driver signals, ensuring similar gate voltage at the same time due to any mismatch in $V_{GE(th)}$ of the parallel devices
- unipolar gate driver to eliminate variations in $V_{GE(th)}$ throughout the operational lifetime of the device

The application note shows the systematic analysis of the influence of mismatch in the parallel branches. Several important factors must be considered based on the switching performance that is assessed graphically. One of these factors is the parasitic loop inductance, which causes voltage overshoot across the switch and voltage dip due to resistance in current rise. Another critical factor is mid-point capacitance; the charge and discharge of the capacitance cause uneven voltage, leading to current overshoot.

The mismatch of the switching loop stray inductance L_E and L_C may also lead to on-state current imbalance. The mismatch of L_E is more critical compared to the impact of L_C, because L_E serves as negative feedback from the switching loop to the gate loop since during the rise and the fall periods of I_C, the voltage across L_E counteracts the change of the gate voltage, thus slowing down the current slew rate leads to imbalance in the branches. Similar to the effect of L_E , L_C slows down I_C , while the difference in the voltage slew rate is barely noticeable. Although the current slew rate decreases, the voltage stress still exhibits a distinctive increase with the greater L_C. To address these issues, it is essential to carefully plan the layout of the circuit board, select specific components, and incorporate protective measures, especially for high-speed and high-power systems.

Another critical aspect that needs to be considered in paralleling is the choice of package. The Kelvin pin ensures accurate gate drive and minimizes unwanted voltage drops caused by parasitics. The 4^{th} pin isolates the gate drive circuit from the main current path, ensuring stable gate signals. In addition, the kelvin pin provides a direct, low-impedance path, reducing the risk of oscillations in paralleled devices.

Another significant challenge when connecting components in parallel is managing heat, which can result from power consumption, cooling, and temperature imbalances. Effectively managing these concerns requires close attention to the circuit design, the circuit board's layout, and the implementation of heat management strategies.

The layout of the circuit board plays a crucial role in connecting components in parallel. For high-power systems, using a symmetrical layout is recommended when connecting two or three devices. However, ensuring an even distribution of electrical current can be difficult when connecting multiple devices. In such cases, a distributed layout can effectively resolve this issue. On the other hand, when connecting components in parallel, ensure symmetrical cooling management because uneven temperature distribution can lead to device failure, reduced efficiency, and reliability issues.

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[8] See the code examples at www.infineon.com

Appendix

Custom design 1 in a rectangular configuration and custom design 2 in a circular configuration

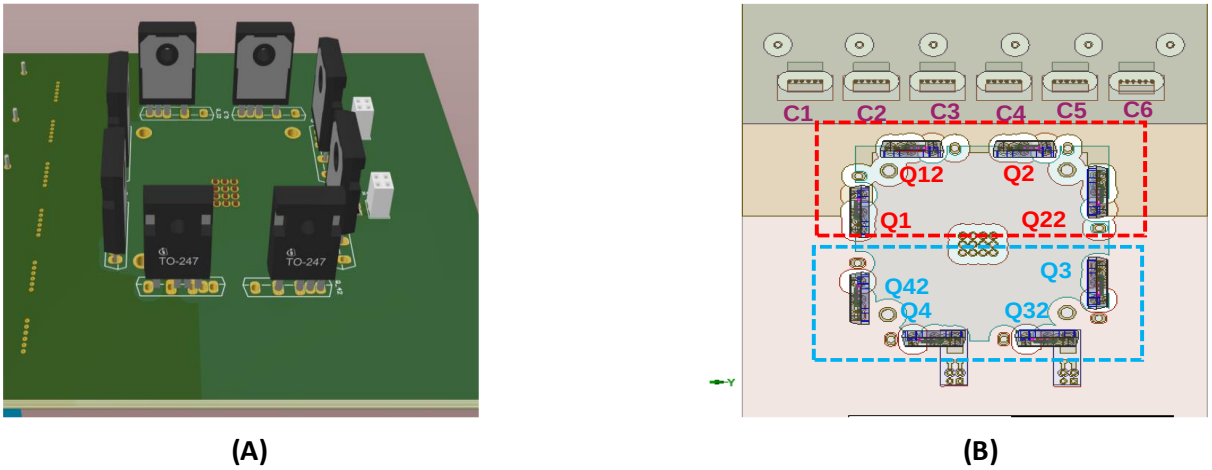


Figure 19 **Custom design 1 half-bridge 4 x parallel (A) 3D view (B) Q3D model**

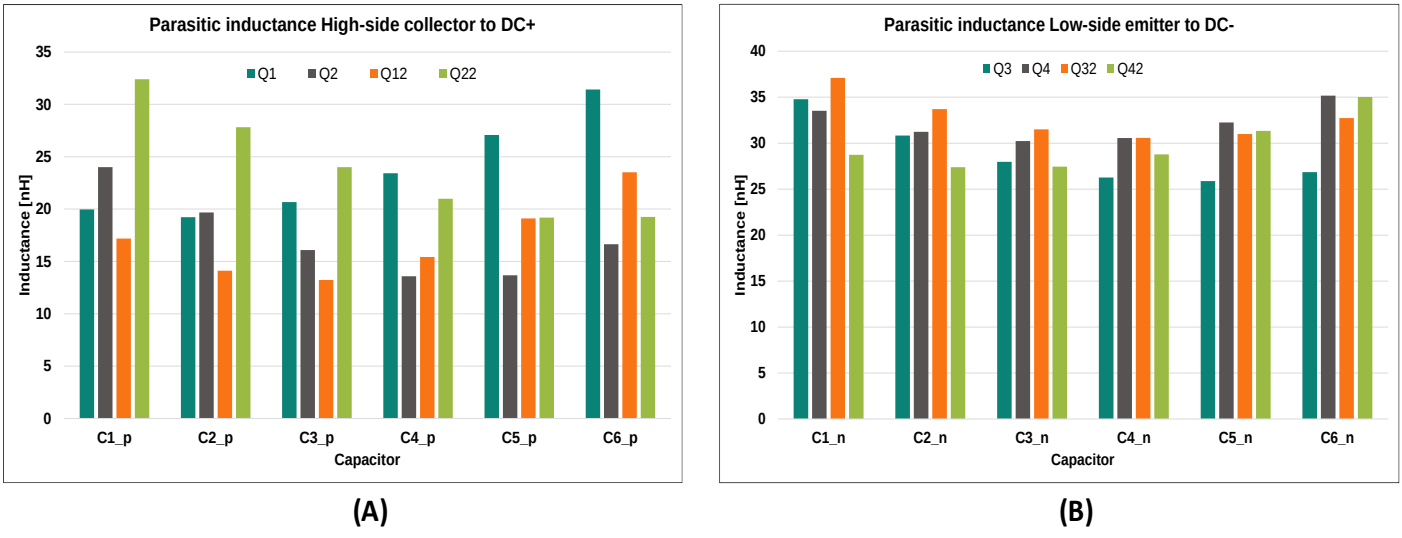
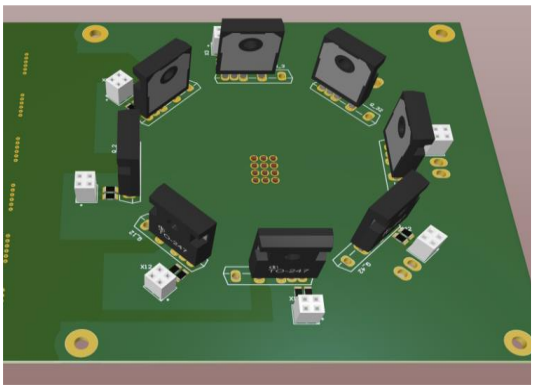
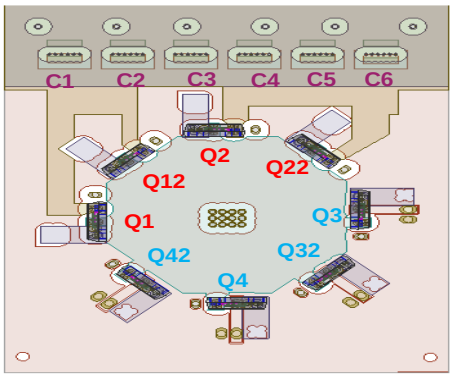


Figure 20 **Extracted parasitic inductance from DC capacitance to switches. (A) High-side collector to DC+ (B) Low-side emitter to DC-**

Custom design 2 in a circular configuration

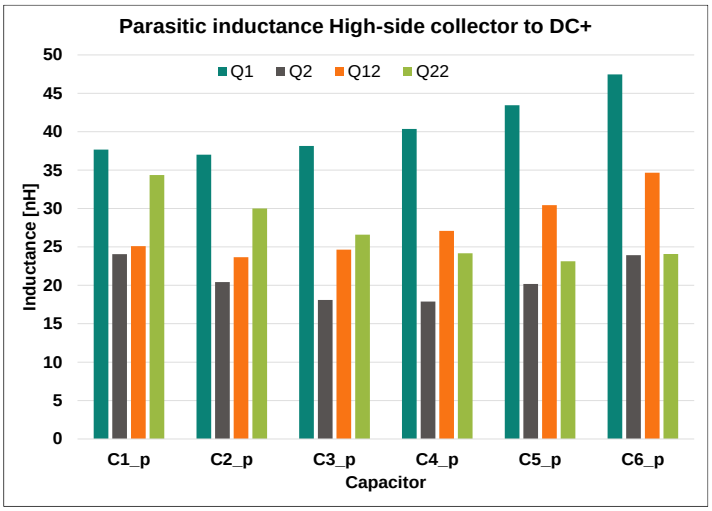


(A)

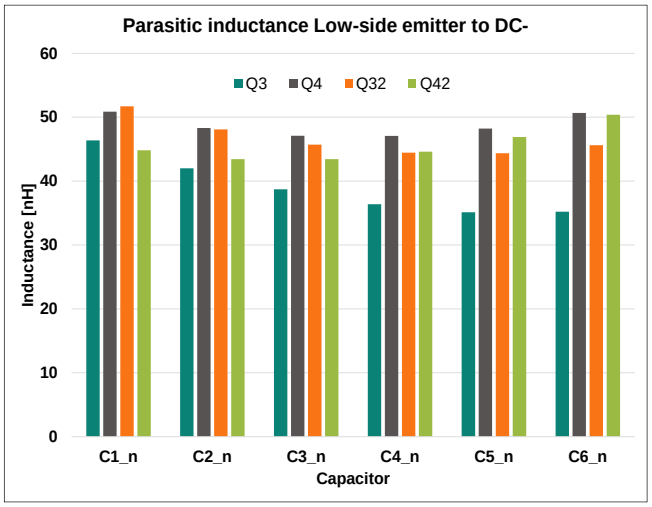


(B)

Figure 21 Custom design 2 half-bridge design 4 x parallel (A) 3D view PCB (B) Q3D model



(A)



(B)

Figure 22 Extracted parasitic inductance from the DC capacitance to the switches (A) High-side collector to DC+ (B) Low-side emitter to DC-

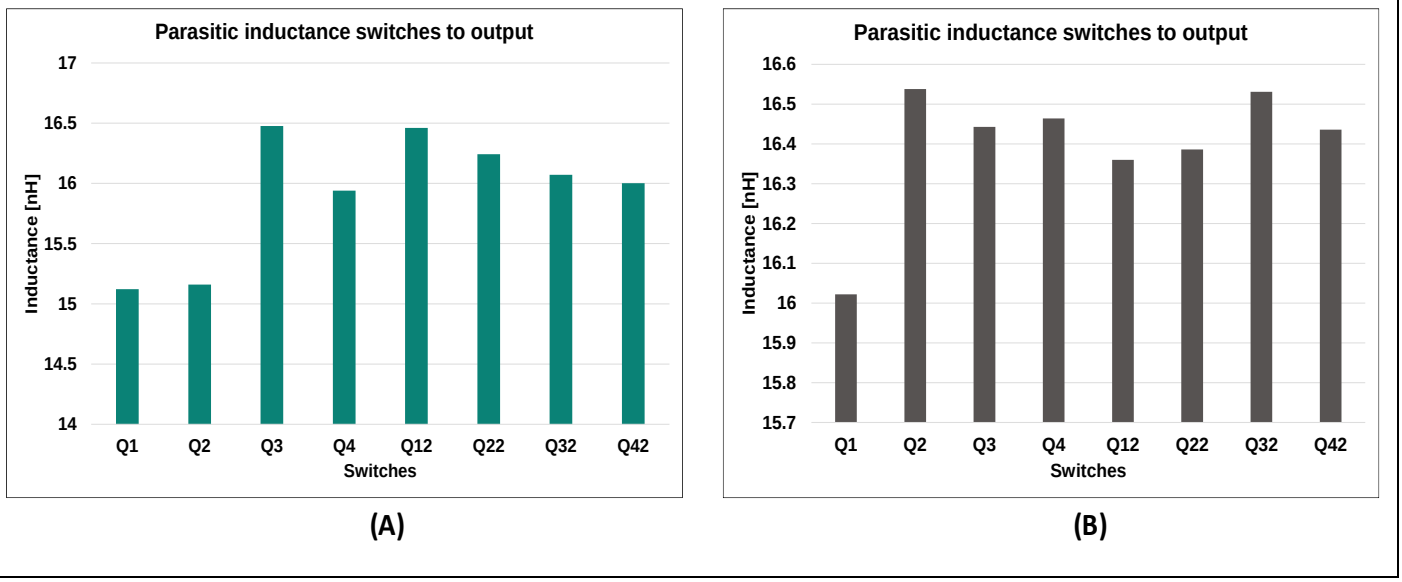


Figure 23 Extracted parasitic inductance from output to switches (A) Custom design 1 (B) Custom design 2

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