HRPWM
High Resolution PWM

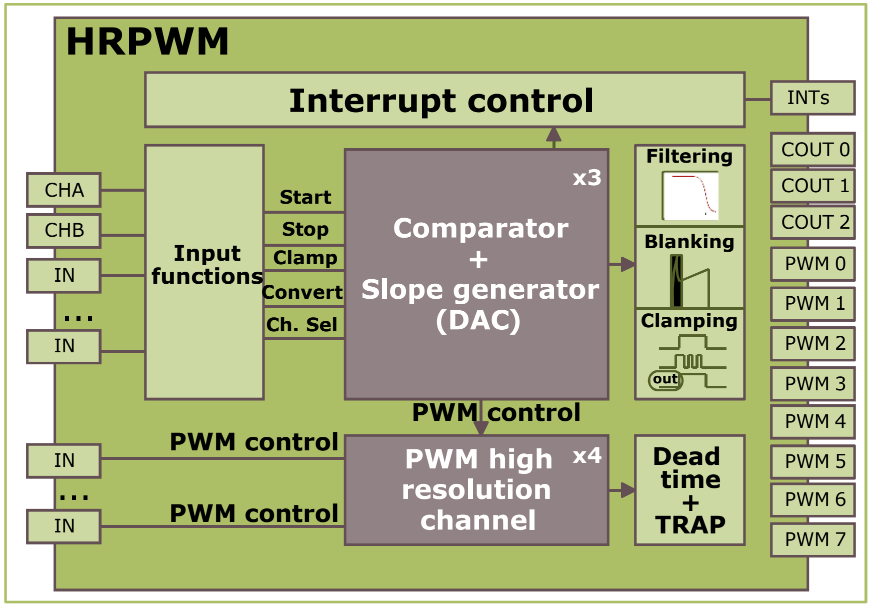
XMC™ microcontrollers
September 2016

Agenda

1. Overview
2. Key feature: comparator & HW slope generator
3. Key feature: complementary high resolution PWM outputs
4. Key feature: configurable PWM control scheme
5. System integration
6. Application examples

Agenda

HRPWM
High Resolution PWM



Highlights

The features of the HRPWM make it a must have module, for cutting edge and optimized SMPS (Switched Mode Power Supply) applications development.
With three high speed comparators and hardware slope generators plus 4 high resolution PWM generators (150 ps), it is possible to address several power conversion topologies with reduced SW interaction.

Key feature

- Comparator + HW slope generator
- Complementary high resolution PWM outputs
- Configurable PWM control scheme

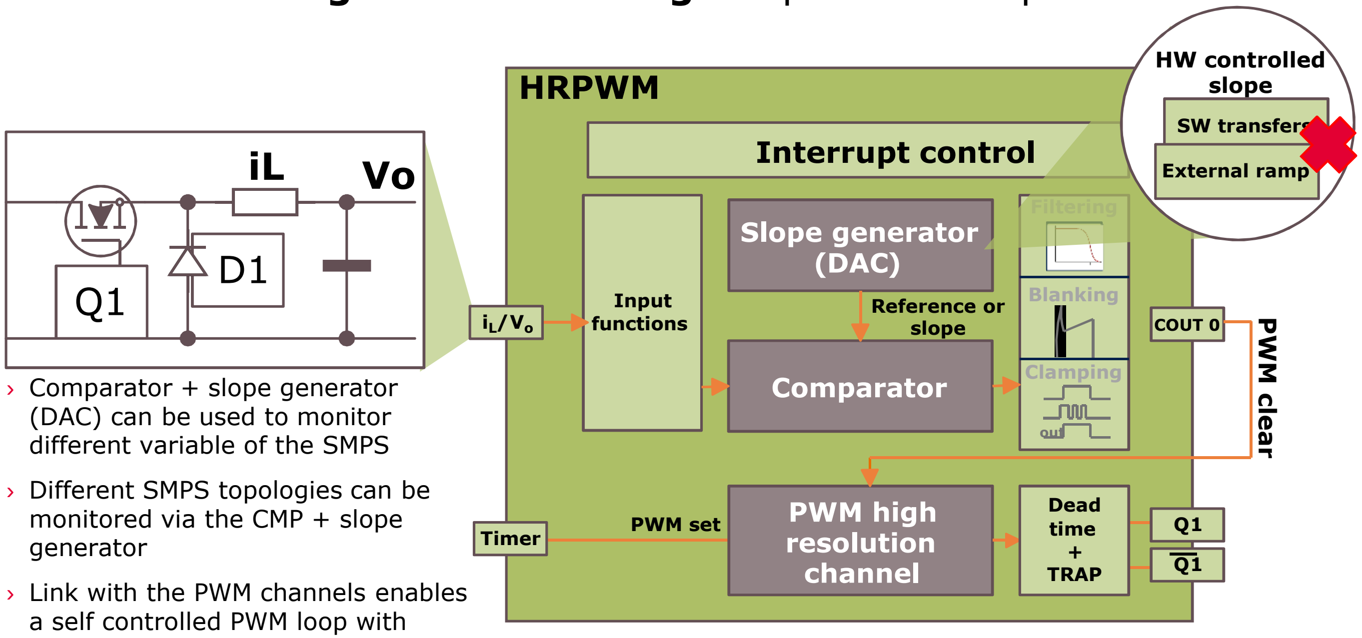
Customer benefits

- Monitor current/voltage for several SMPS topologies with reduced SW interaction
- Higher resolution enables SMPS control up to 5 MHz with 10-bit PWM or highly accurate low load scenario control
- Control of several SMPS topologies: half bridge, full bridge, resonant, phase shift,...

Agenda

HRPWM
Comparator + HW slope generator (1/2)

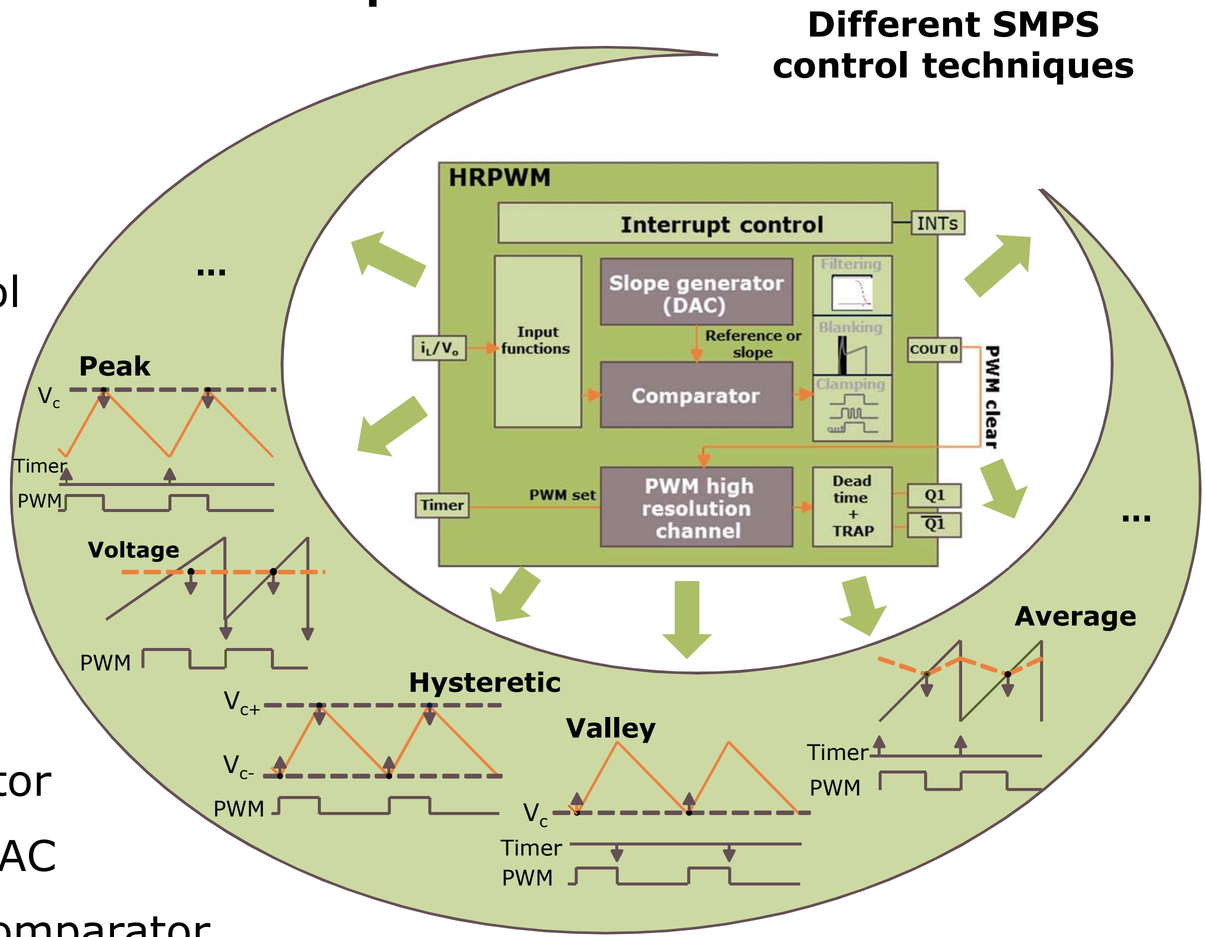
- High speed comparator (~20 ns) can be used to:
  - Monitor coil **current**
  - Monitor **voltage over the switch**
  - Monitor **voltage output**
- The slope generator with a high speed DAC (> 30 MS/s) can be used to:
  - Reference control for the comparator
  - Insert a **decrementing** or **incrementing** ramp to the comparator



- Comparator + slope generator (DAC) can be used to monitor different variable of the SMPS
- Different SMPS topologies can be monitored via the CMP + slope generator
- Link with the PWM channels enables a self controlled PWM loop with minimal SW interaction

HRPWM
Comparator + HW slope generator (2/2)

- Due to the flexible arrangement of resources it is possible to cover **several control techniques**:
  - Peak current control
  - Valley current control
  - Hysteretic control
  - Average current control
  - Voltage control
- Each slope + comparator can be used to control a different control technique
  - Decrease BOM:
    - Internal slope generator
    - Internal high speed DAC
    - Internal high speed comparator



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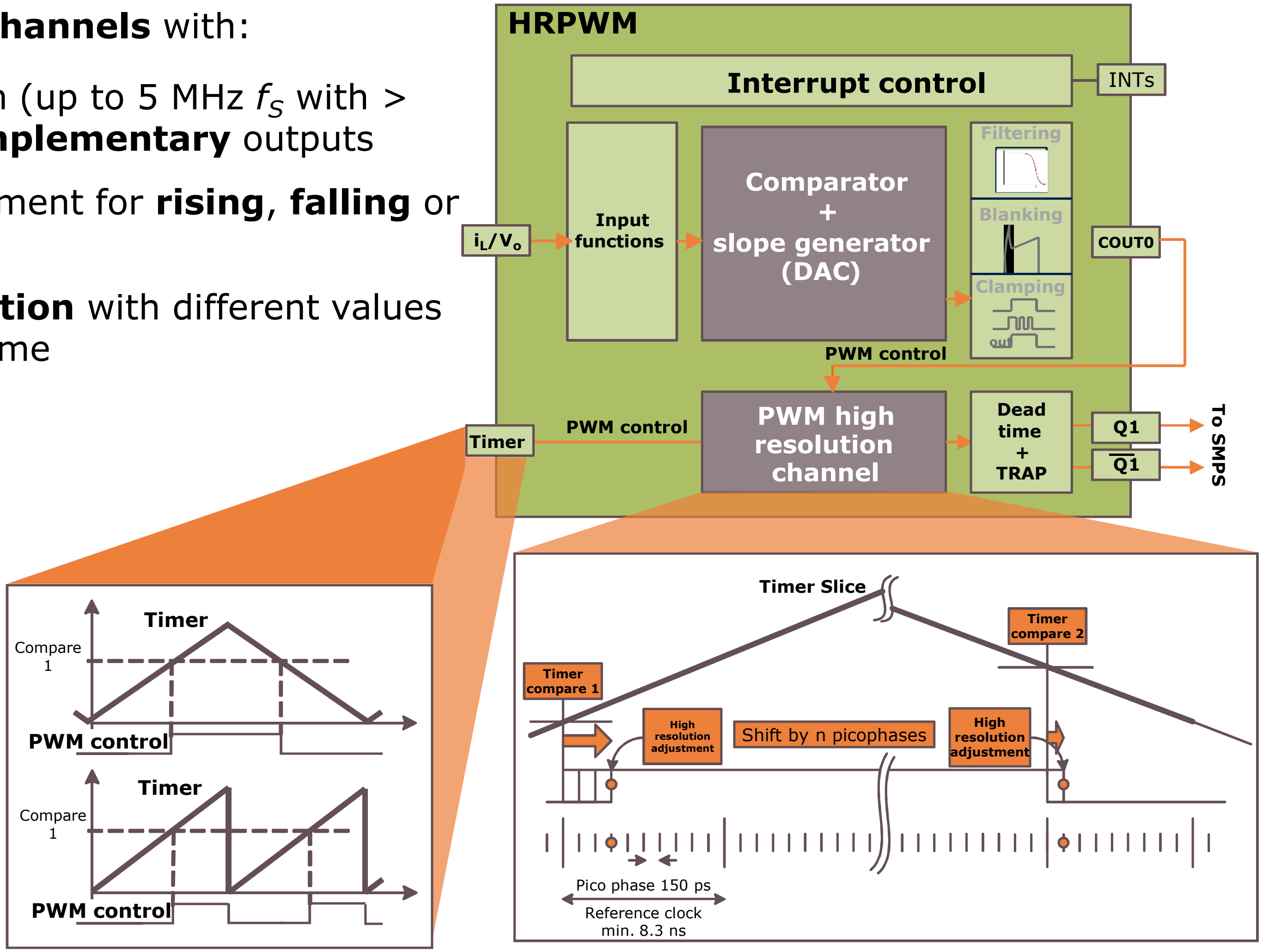
HRPWM: complementary high resolution PWM outputs (1/2)

- **4 high resolution channels** with:
  - **150 ps** resolution (up to 5 MHz f_S with > 10-bits) with **complementary** outputs
  - Resolution adjustment for **rising**, **falling** or **both**
  - **Dead time insertion** with different values for ON and OFF time
- Can be used with:
  - **CCU8** timers
  - **CMP + slope gen**
  - **Both of the above**

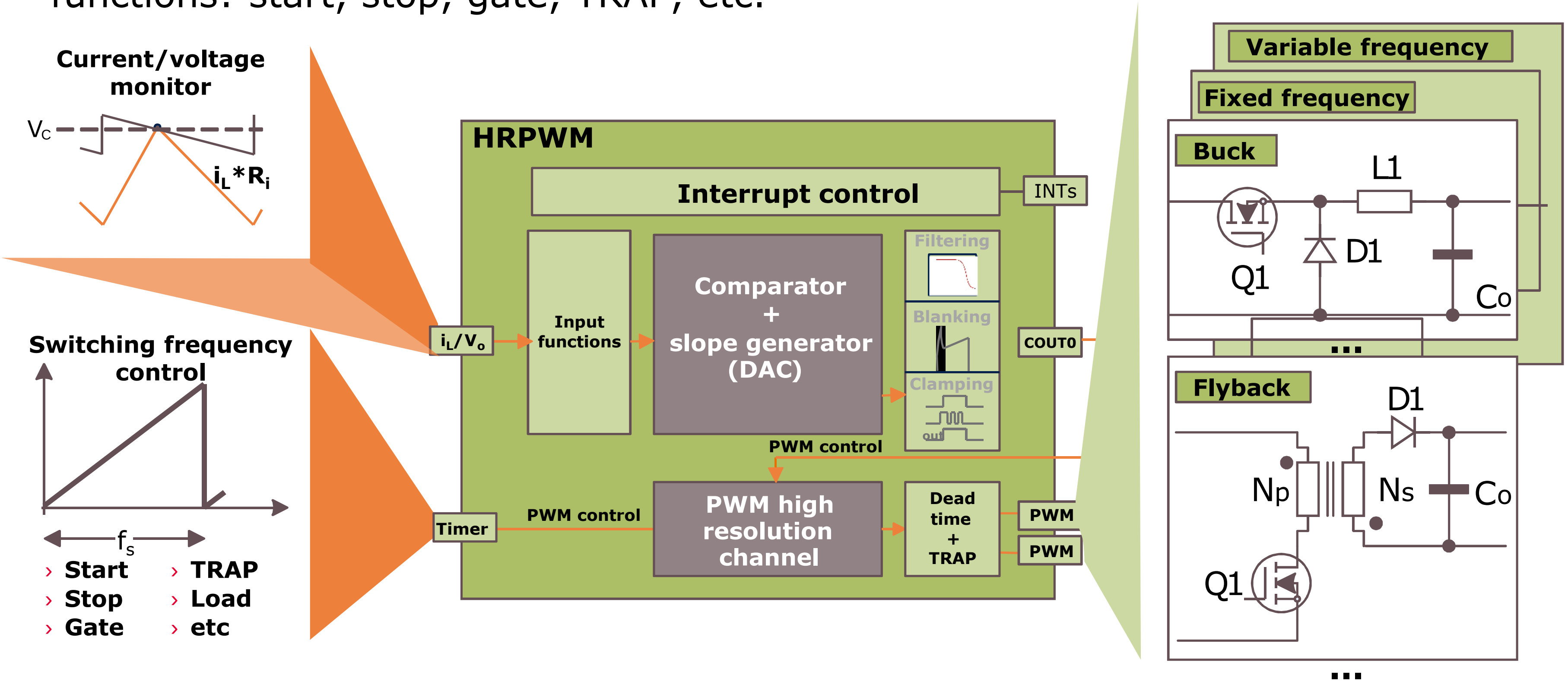


HRPWM: complementary high resolution PWM outputs (2/2)

› Each of the high resolution channels can be controlled depending on the **wanted control technique** (e.g. fixed frequency, variable frequency, etc.)

› Addressing up to **4 complementary MOSFET pairs**

› Linking with the powerful CCU8 timers enable a very large superset of control functions: start, stop, gate, TRAP, etc.



Agenda

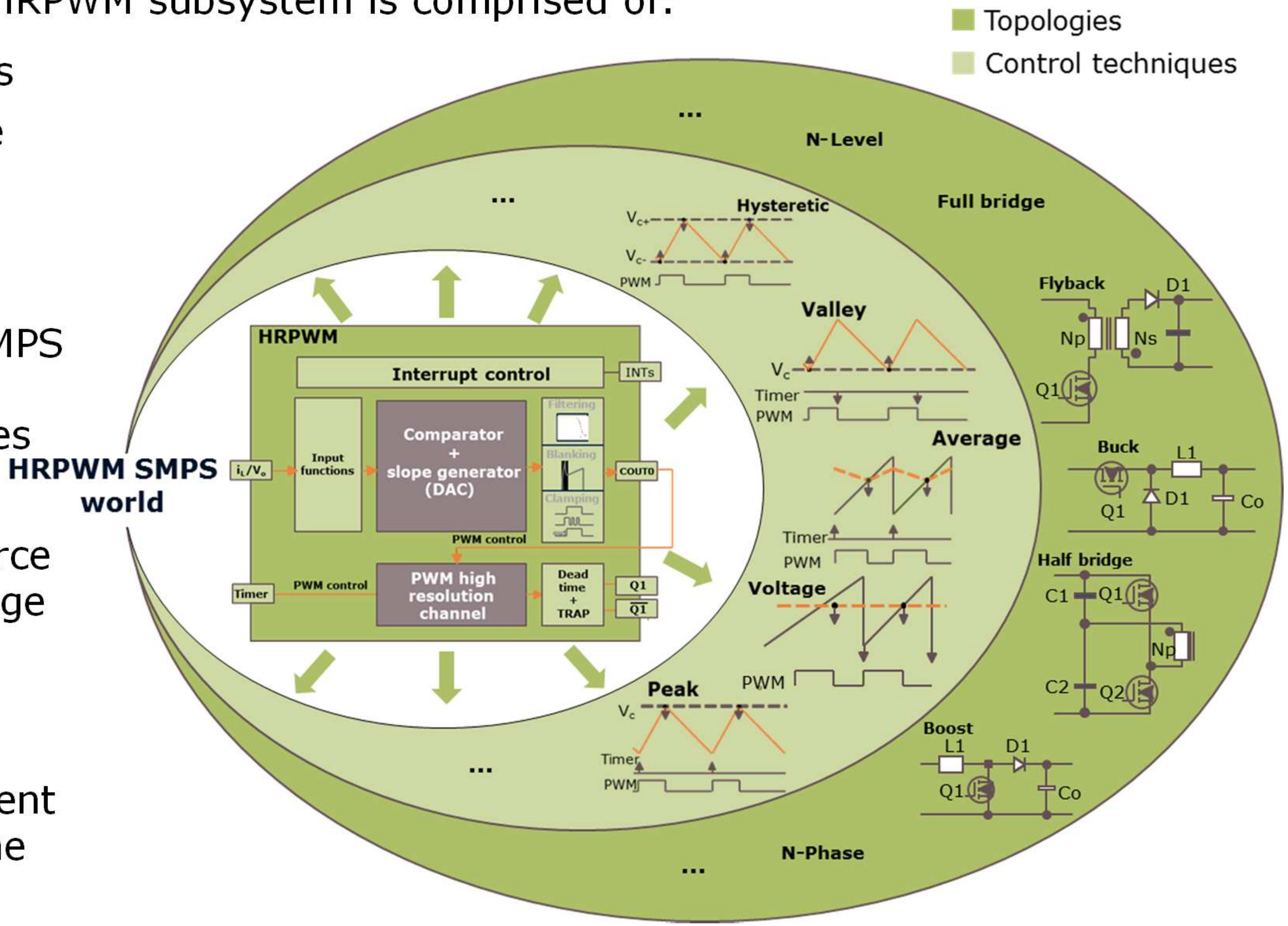
HRPWM
Configurable PWM control scheme

› The complete HRPWM subsystem is comprised of:
  – 16-bit timers
  – CMP + slope gen
  – 150 ps generators

› Covers all the SMPS topologies and control techniques

› Optimized resource organization/usage for any SMPS topology

› Possibility of controlling different SMPS in the same module



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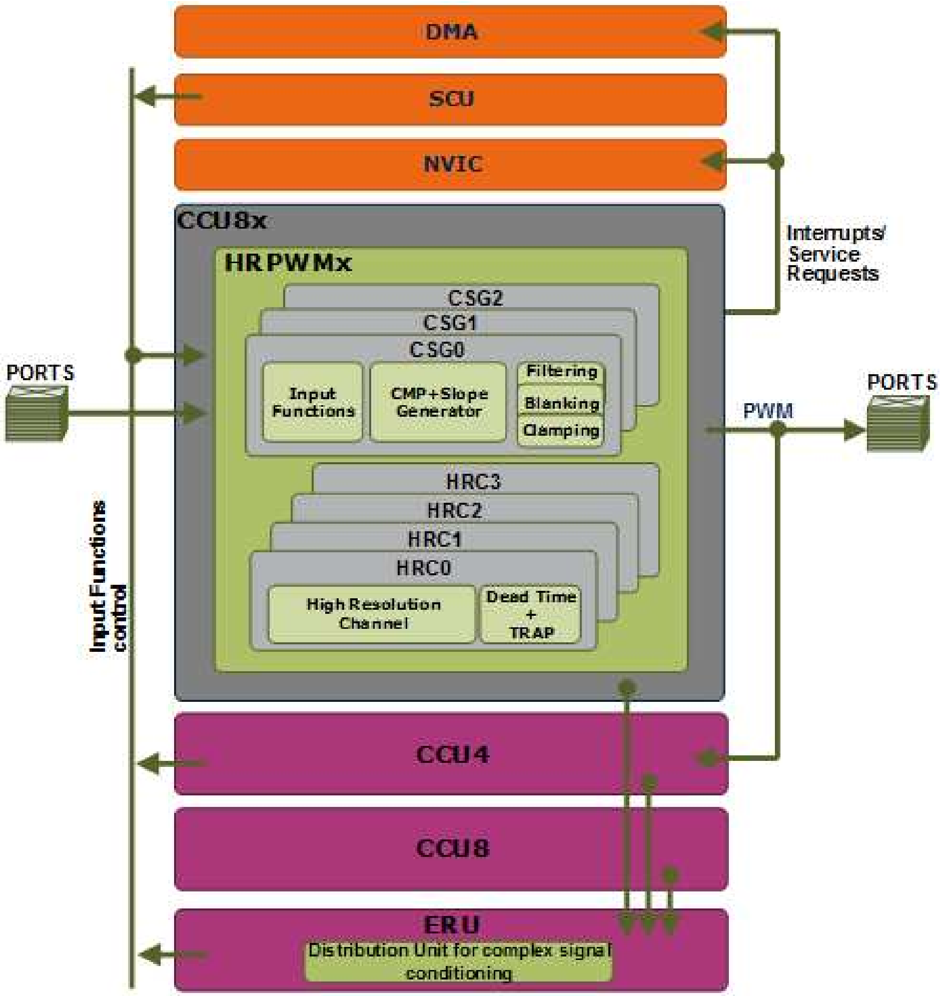
HRPWM
System integration



**Several components may be present or not depending on the device*

XMC™4100	XMC™4200	XMC™4400	XMC™4500	XMC™4700
●	●	●		

XMC™1100	XMC™1200	XMC™1300

The HRPWM system integration offers several advantages:

- Integration within a CCU8 module, offers the broad set of features available on each CCU8 timer
- Distribution bus from CCU4/CCU8 over the ERU for complex signal conditioning application cases
- Tight coupling between CSGs and HRCs to avoid SW overhead

- Target applications
  - Power conversion
  - Motor control
  - General purpose

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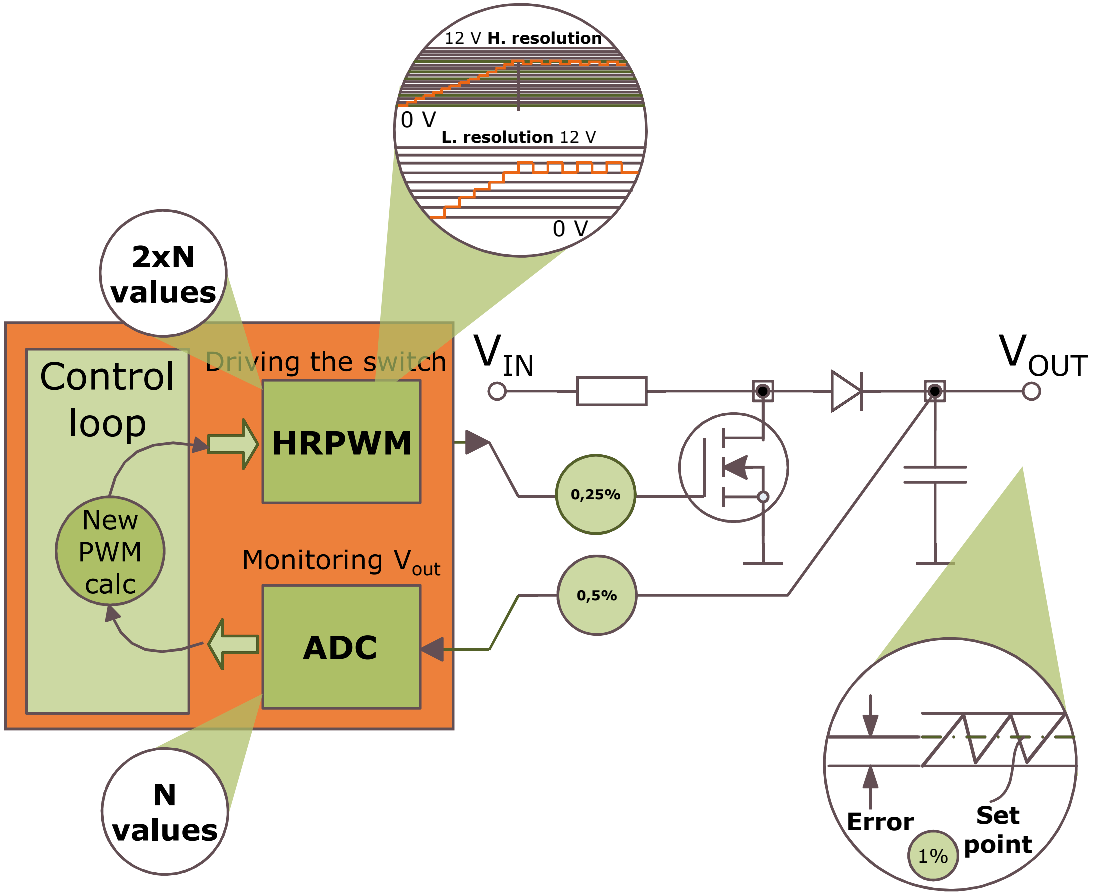
Application example
PWM resolution vs. f_s (1/2)



In brief

SMPS resolution demand for high f_S

Overview

For a standard SMPS closed loop control application, the ADC sensing resolution needs to be two times as precise as the allowed error of the voltage operating point.

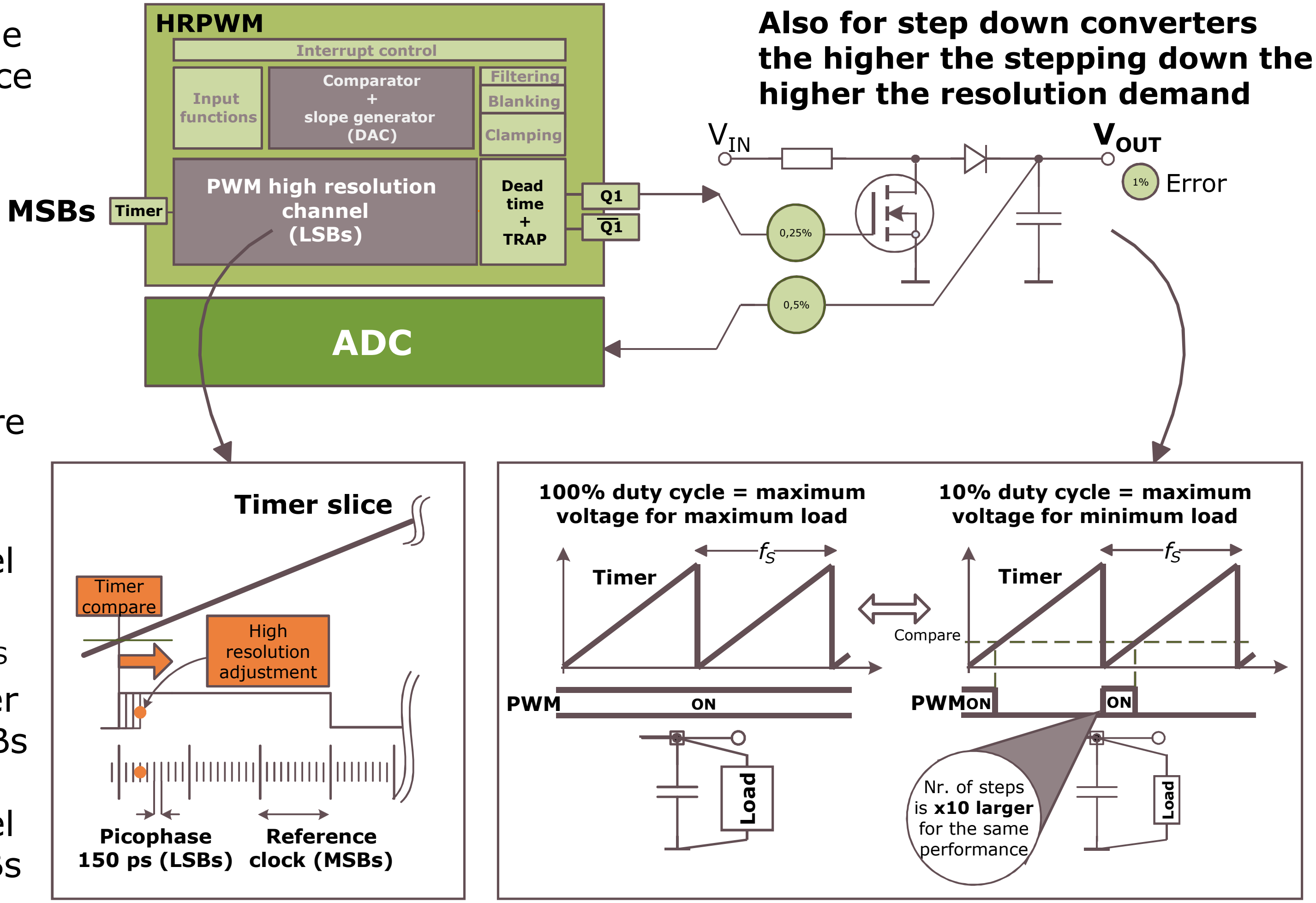
The PWM generation needs to accommodate the measurement error by offering 2x the ADC precision.

For an SMPS running at high f_S values, the normal PWM resolution is not enough.

The HRPWM enables this error compensation for f_S values up to 5 MHz.

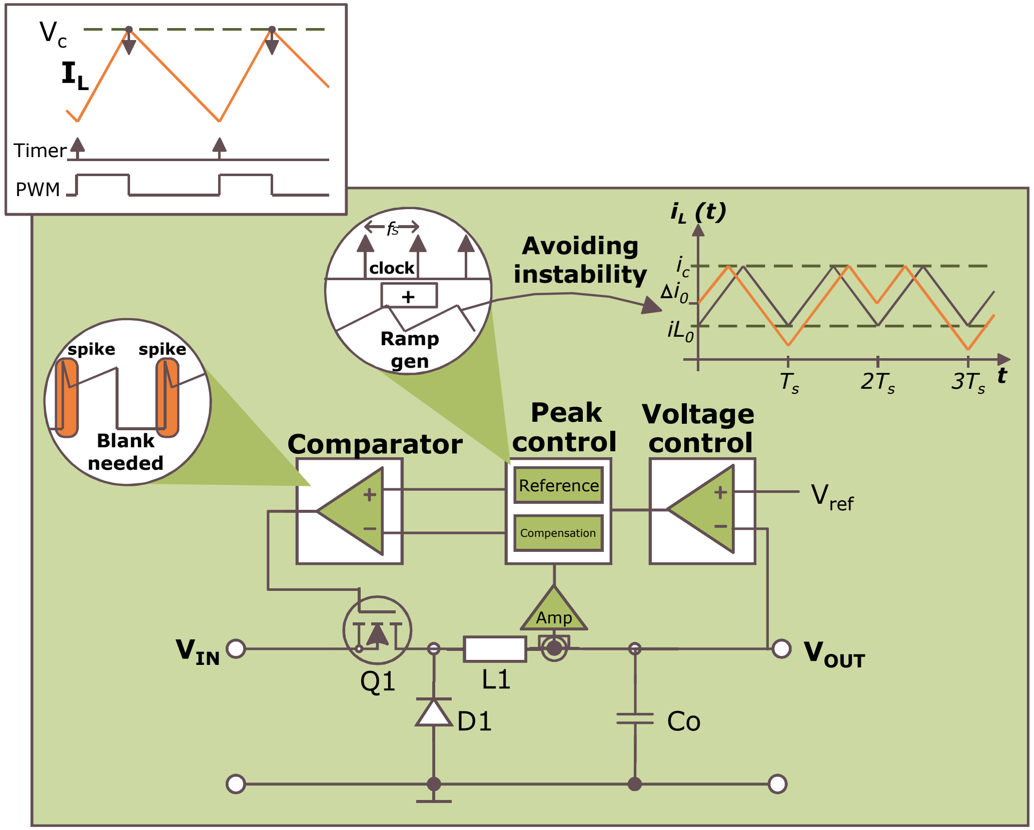
Application example
PWM resolution vs. f_s (2/2)

- Assuming the same control performance at 10% load, the number of PWM steps has to be increased by a factor of 10
- For a SMPS operating at 1.5 MHz 4000 steps are needed
- Each High Resolution Channel can generate ~ 4470 at 1.5 MHz f_S
- Normal CCU8 timer generates the MSBs while a High Resolution Channel generated the LSBs



Application example low load conditions: detailed block diagram

Application example
Buck converter – peak current control (1/2)



Overview

The **peak current** control is a common technique for a **buck converter**.

This control technique is comprised of two loops: **current** and **voltage**.

The cycle-by-cycle current loop offers a **very good response for fast load transients**. But this inner loop becomes **unstable** with high duty cycle values. To avoid this **a ramp is added** to maintain the wanted average current and avoid the instability.

A comparator with some filtering capabilities is needed to avoid the **current commutation spikes**.

In brief

Control a buck converter with peak current control with the HRPWM

Application example
Buck converter – peak current control (2/2)

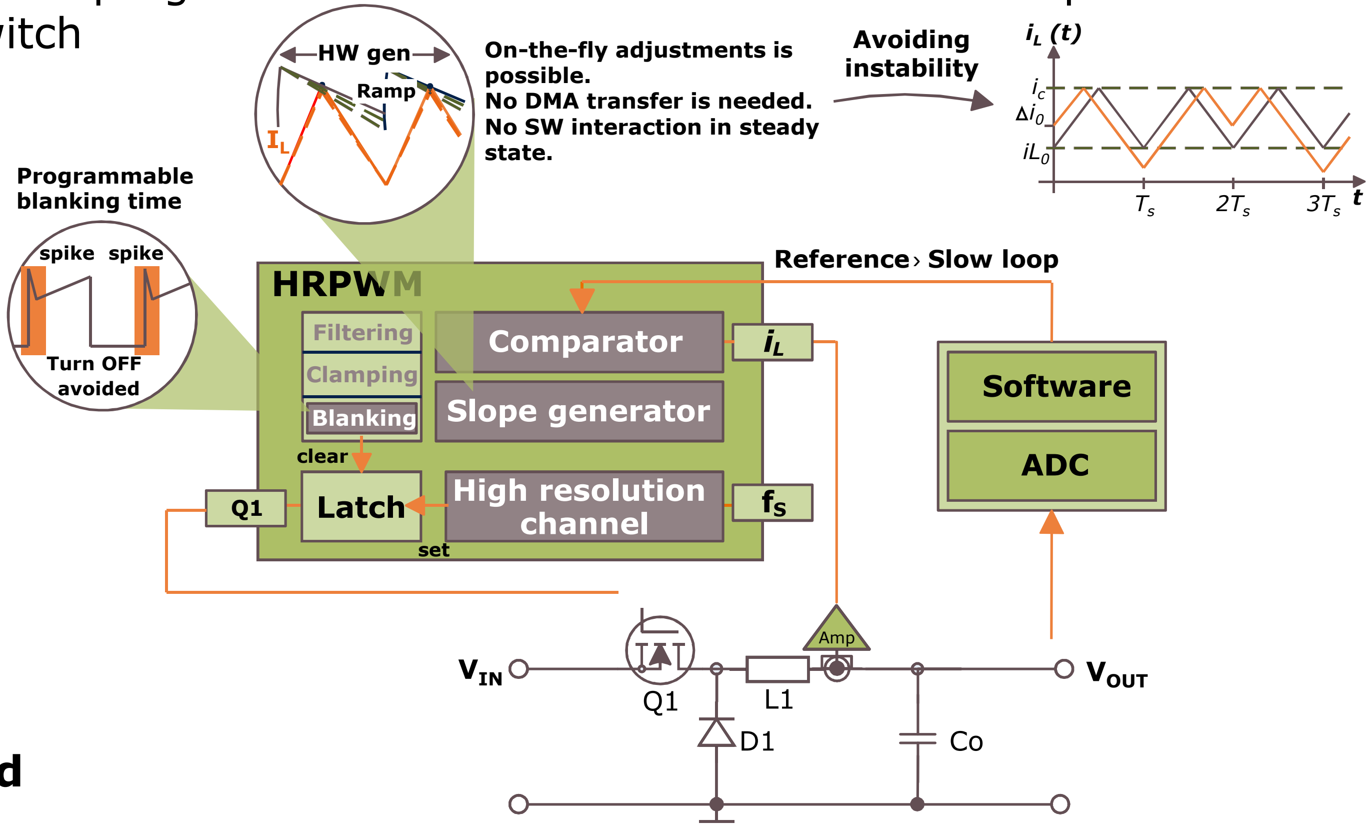
› The HRPWM slope generator is programmed with the wanted slope value (via 3 parameters)

› The blanking stage is programmed with the wanted value to avoid premature turn OFF of the switch

› Via the ADC the voltage loop is monitored

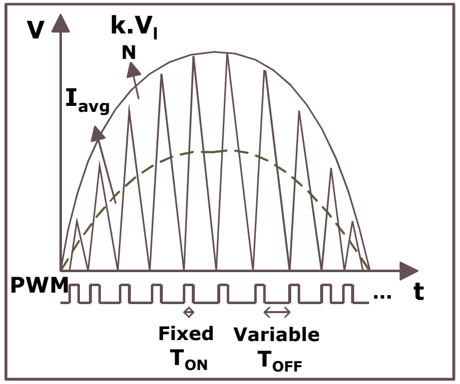
› A timer is connected to the HRPWM to control the wanted switching frequency f_S

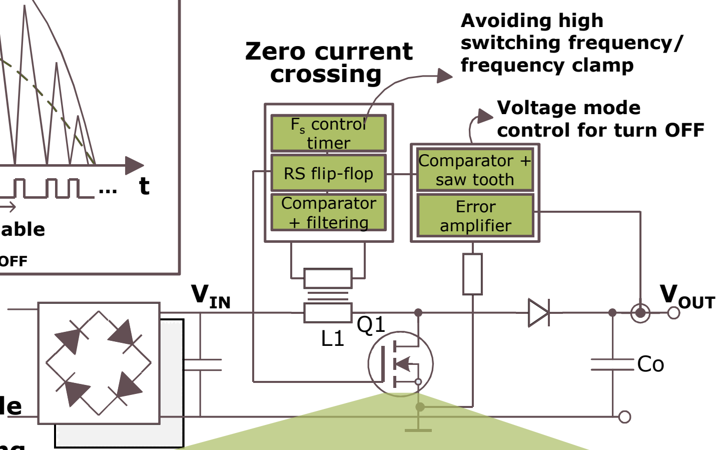
› **Decreased BOM and low CPU load**



Application example buck converter – peak current control: detailed block diagram

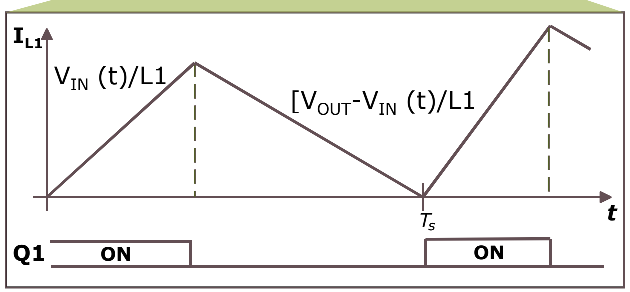
Application example: single stage PFC – critical conduction mode (1/3)





WHY CrM?

- Current loop is intrinsically stable
- Reduced switching losses because Mosfet can be turned ON at lower voltage
- Diode turn OFF without reverse recovery losses
- TON is fixed for a given line voltage and load current condition



In brief

- Single stage PFC controller

Overview

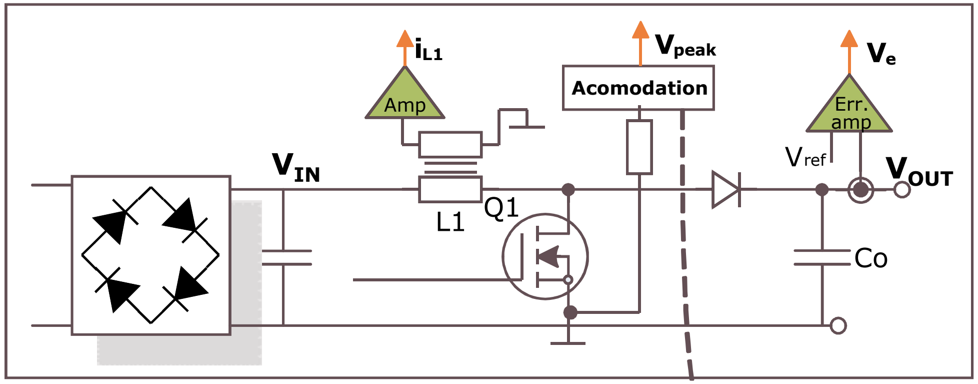
The **P**ower **F**actor **C**orrection (PFC) technique, shapes the input current of the off line power supply to **maximize the real power availability** from the mains. Additional reason to use PFC, may be the need to comply with some **regulation requirements**.

Several conditions are taken into consideration to choose the PFC topology: cost, complexity, efficiency, etc.

For small output power applications, the **boost** converter operating in **C**ritical **C**onduction **M**ode (CrM) is one of the most implemented techniques.

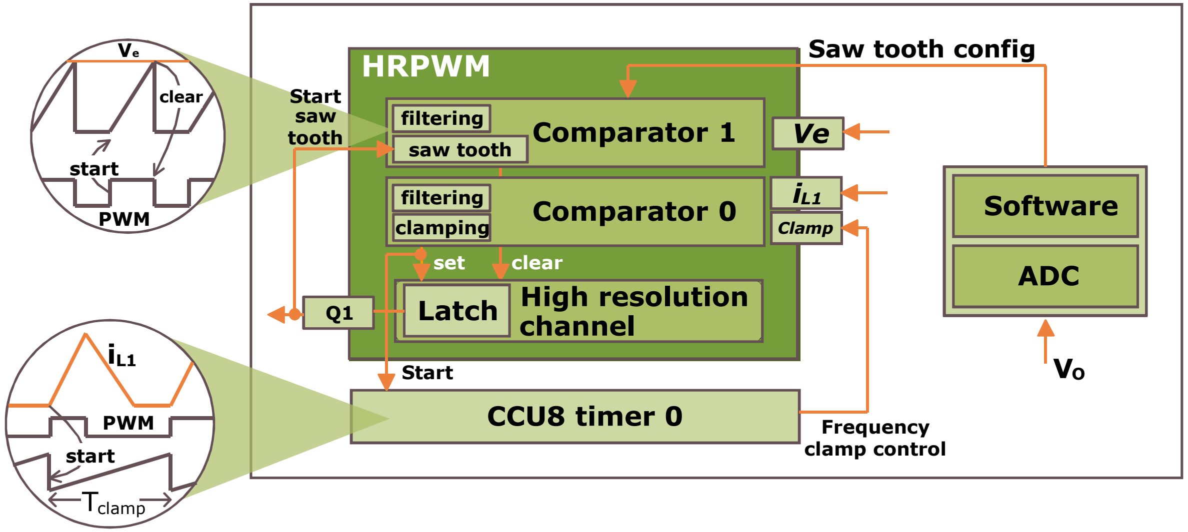
Application example: single stage PFC – critical conduction mode (2/3)

- **A complete implementation with 1:1 map with usual analog control can be done with the HRPWM**
- A **comparator** is used to monitor the set condition of the PWM signal (**ZCD**)
- A second **comparator** with the slope generation is used to monitor the turn OFF condition **(saw tooth generation is done automatically in HW)**
- A **CCU8 timer is used to perform the frequency clamping**. Avoiding high switching frequencies
- **Decreased BOM**



One-to-one map with external/ analog control

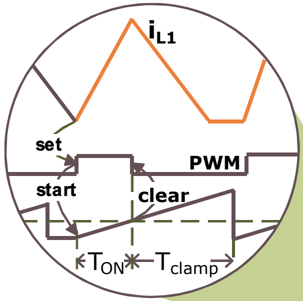
The scheme of the saw tooth can also be replaced by sensing Vpeak

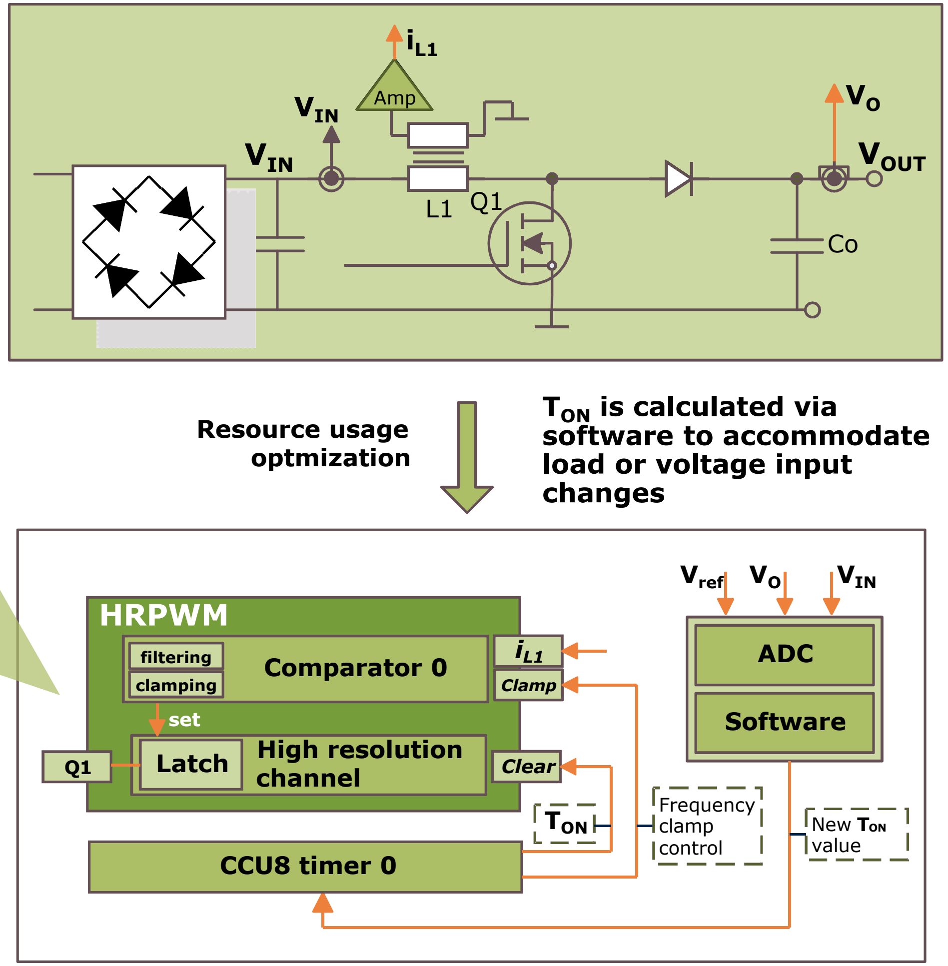


Application example boost PFC: block diagram

Application example: single stage PFC – critical conduction mode (3/3)

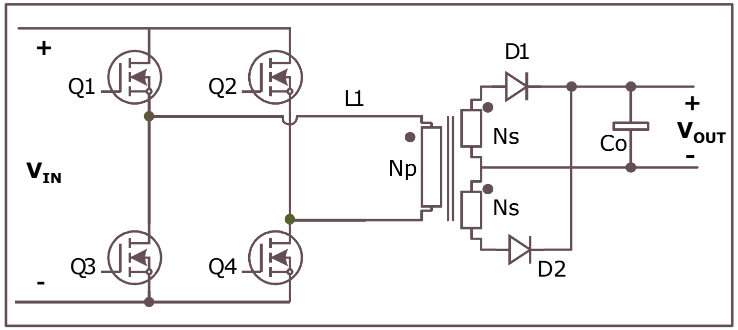
- A more resource optimized solution can be achieved, **by calculating the PWM ON time in software**
- The ADC is used to sample the **voltage error** and also the **voltage input**
- With the values sampled by the ADC, the software calculates the **new PWM T_{ON}** values accordingly
- Calculation of the T_{ON} can be done multiple times per line cycle if needed
- **Very low BOM: only current amplifier**



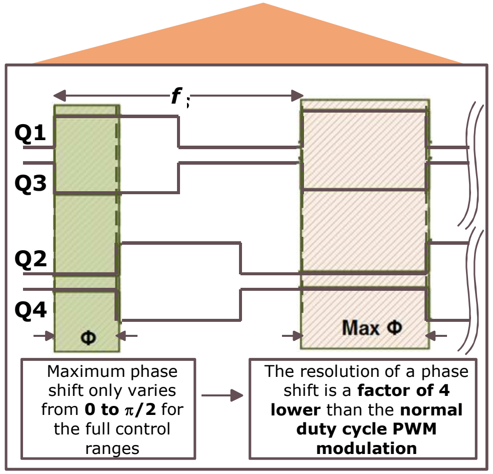


Application example boost PFC: block diagram with T_{ON} calculation by SW

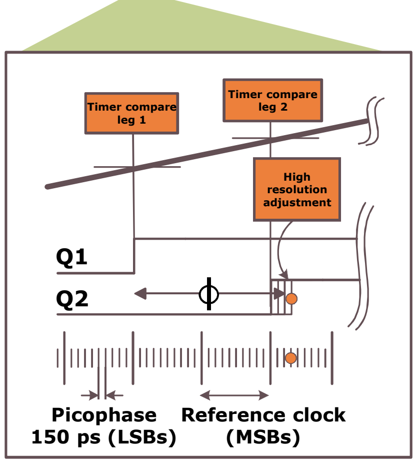
Application example
Phase shift full bridge (1/3)



The resolution loopback issue of the ADC vs the PWM signal is more severe than for the normal PWM modulation



For a 100 kHz phase shift modulation, the HRPWM can achieve 14-bits resolution. This complies with the necessity of $N_{PWM} > 2xN_{ADC}$



In brief

› Phase shift full bridge with high resolution

Overview

The **P**hase **S**hift **F**ull **B**ridge Converter (**PSFB**) offers high efficiency for high power applications. Efficiency values can easily be within 90% to 95%.

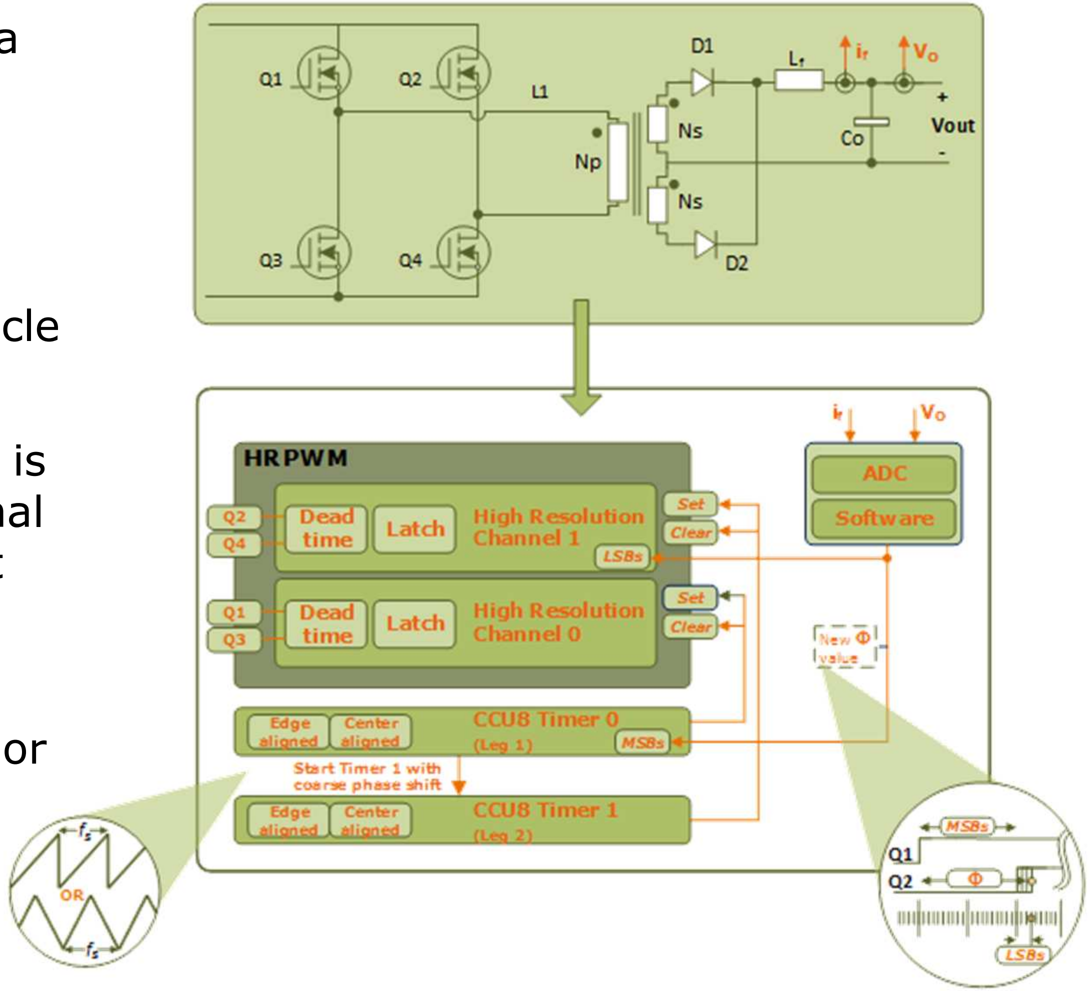
The efficiency advantage comes from the fact that the converter can achieve **Z**ero **V**oltage **S**witching (**ZVS**) with reduced conduction losses.

The phase shift PWM signals, drive **two pairs of complementary switches**, with normally 50% duty cycle with a fixed frequency.

The amount of **power transfer to the output** is then **dictated by the phase shift** introduced between the two legs.

Application example
Phase shift full bridge (2/3)

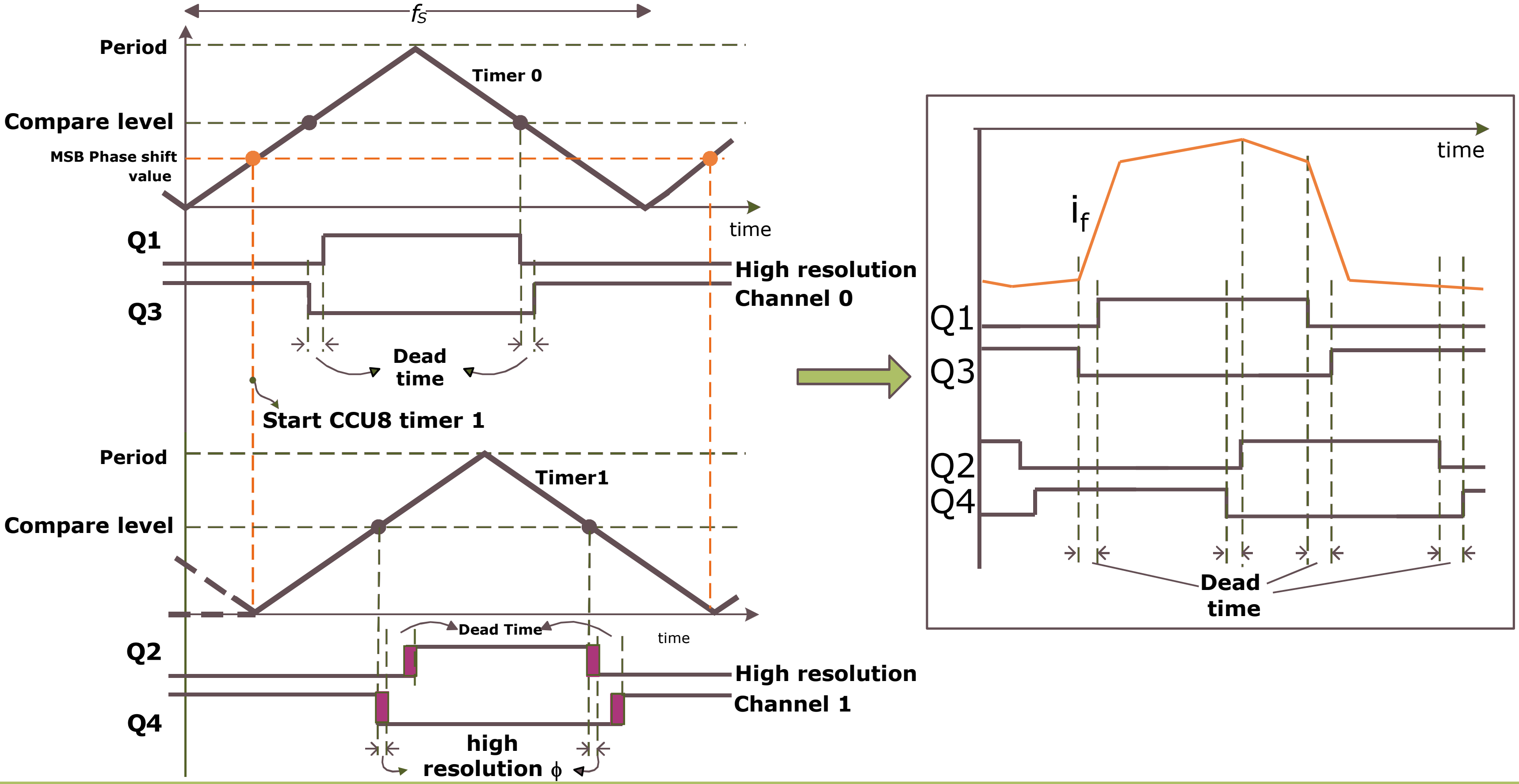
- Each PSFB leg is controlled via one CCU8 timer and one high resolution channel
- Each CCU8 timer are programmed with a fixed frequency and a fixed duty cycle (50 %)
- The high resolution channel 1 is used to introduce the additional resolution into the phase shift value
- The timer control scheme for the phase shift can be center or edge aligned



Application example phase shift full bridge: block diagram

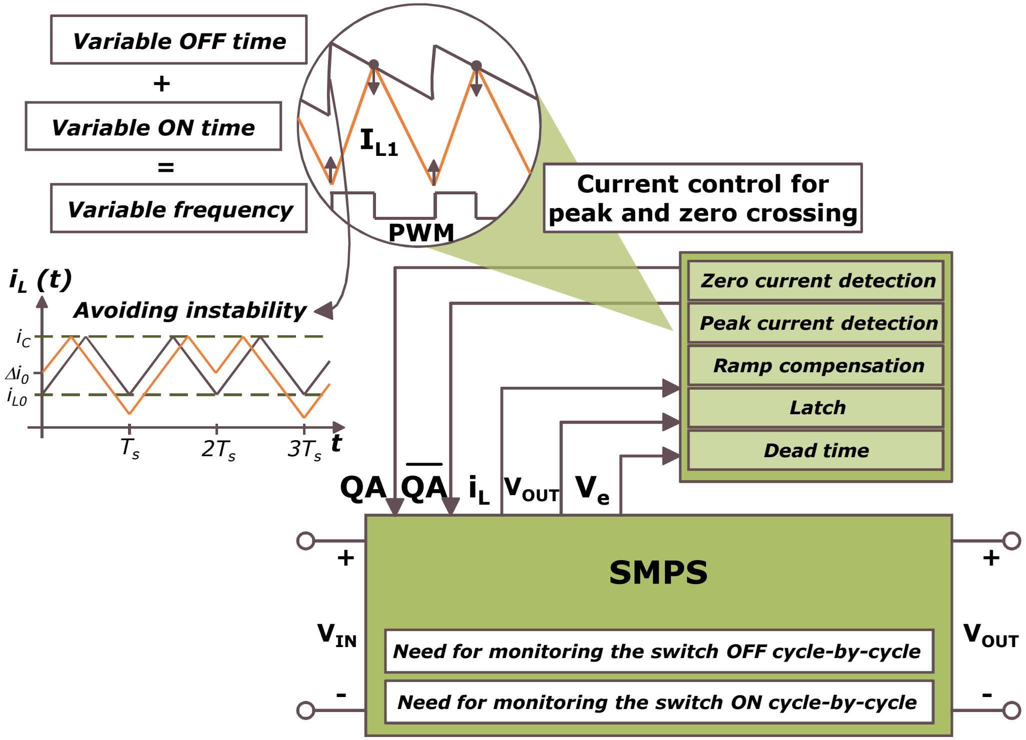
Application example
Phase shift full bridge (3/3)

- The phase shift value can be updated in every switching cycle MSBs+LSBs
- Each dead time value is completely configurable and can be adjusted in every switching cycle



Application example phase shift full bridge: timing diagram

Application example
Maximizing resource utilization for SMPS (1/2)



In brief

› Improving resource utilization for peak + ZCD

Overview

When a converter operates with a **variable ON and OFF time** for the PWM signal and a cycle-by-cycle monitor is needed, it is necessary to monitor two thresholds:

› the peak current

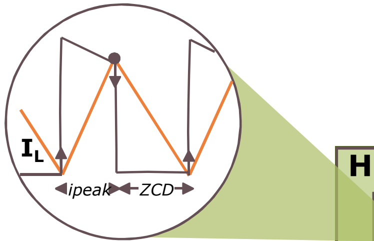
› the zero current crossing

Monitoring these two variables can be resource consuming, especially when an **additional ramp** needs to be injected to avoid instability of the current loop.

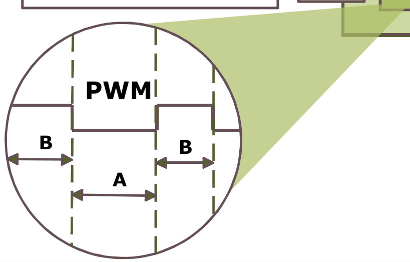
The HRPWM combines all of these three functions: ramp + peak + zero current detection in just one comparator and slope generation Unit.

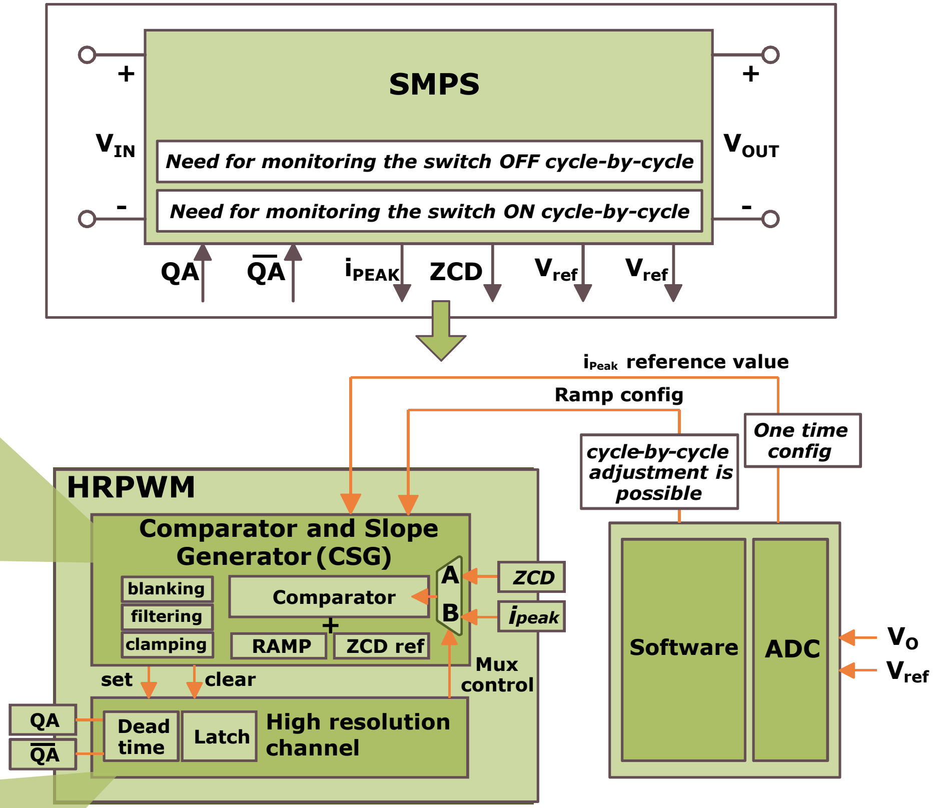
Maximizing resource utilization for SMPS (2/2)

- **Each CMP + slope generator is able to monitor both ZCD and peak current**
- The switch between the two comparator input channels is done automatically via HW
- **The slope generator is started every time that i_{peak} needs to be sensed**
- The **ZCD reference value** is monitored whenever the PWM signal is ON
- **Control up to 3 SMPS** with very low CPU interaction



With just one comparator and slope generator it is possible to monitor both ZCD and peak current

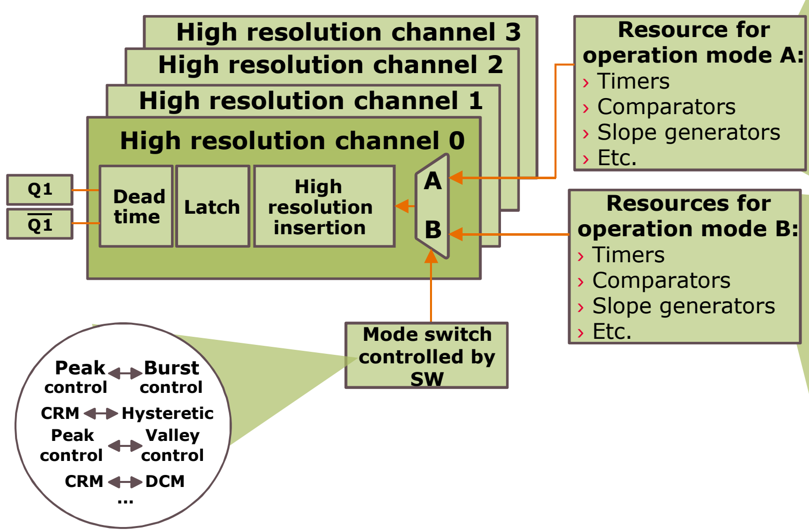


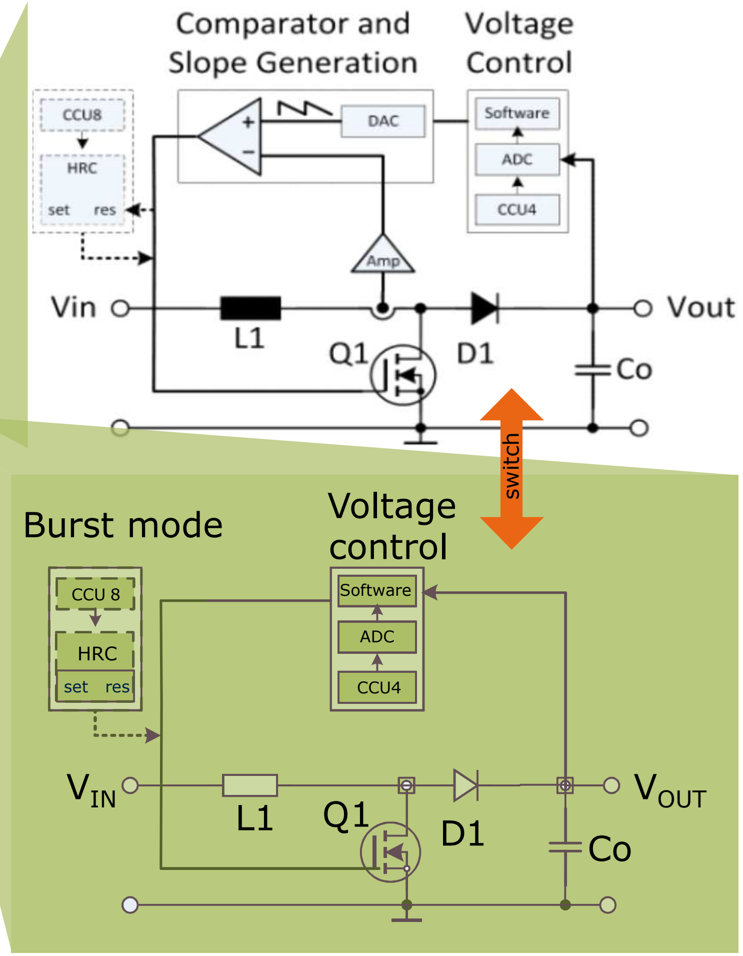


Application example resource optimization: block diagram

Application example
Multi-mode SMPS control

- **Switching between operation modes due to load or V_{IN}/V_{OUT} modifications can improve converter efficiency**
- Each HRC can operate with **two sets of resources**





- Each set of resources can be used to implement a different operation mode
- **Switch between the modes can be done on-the-fly via SW**

Application example multi-mode SMPS control: block diagram

Support material

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