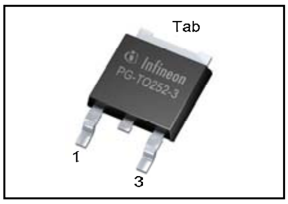
OptiMOS®-T2 Power-Transistor

Product Summary

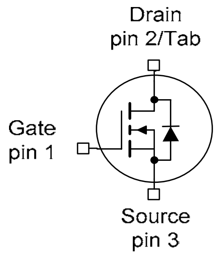
V_{DS}	60	V
$R_{DS(on),max}$	5.1	mΩ
I_D	90	A

PG-TO252-3-11



Features

- N-channel - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested
- Ultra Low R_{DSon}



Type	Package	Marking
IPD90N04S6-05	PG-TO252-3-11	4N0605

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25°C, V_{GS}=10V[1)]	90	A
		T_C=100°C, V_{GS}=10V[2)]	77	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25°C	360	
Avalanche energy, single pulse[2)]	E_{AS}	I_D=45A	135	mJ
Avalanche current, single pulse	I_{AS}	-	90	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25°C	107	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	–

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2)]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	1.4	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[3)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D= 1mA	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=60µA	2.0	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=60V, V_{GS}=0V, T_j=25°C	-	0.01	1	µA
		V_{DS}=60V, V_{GS}=0V, T_j=125°C[2)]	-	5	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=90A	-	4.2	5.1	mΩ

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	5000	6500	pF
Output capacitance	C_{oss}		-	1230	1600	
Reverse transfer capacitance	C_{rss}		-	50	100	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30V, V_{GS}=10V, I_D=90A, R_G=3.5Ω	-	20	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	35	-	
Fall time	t_f		-	8	-	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=48V, I_D=90A, V_{GS}=0 to 10V	-	28	36	nC
Gate to drain charge	Q_{gd}		-	7	14	
Gate charge total	Q_g		-	62	81	
Gate plateau voltage	$V_{plateau}$		-	5.6	-	V
Reverse Diode						
Diode continous forward current[2]	I_S	T_C=25°C	-	-	90	A
Diode pulse current[2]	$I_{S,pulse}$		-	-	360	
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=90A, T_j=25°C	0.6	0.95	1.3	V
Reverse recovery time[2]	t_{rr}	V_R=30V, I_F=90A, di_F/dt=100A/µs	-	36	-	ns
Reverse recovery charge[2]	Q_{rr}		-	41	-	nC

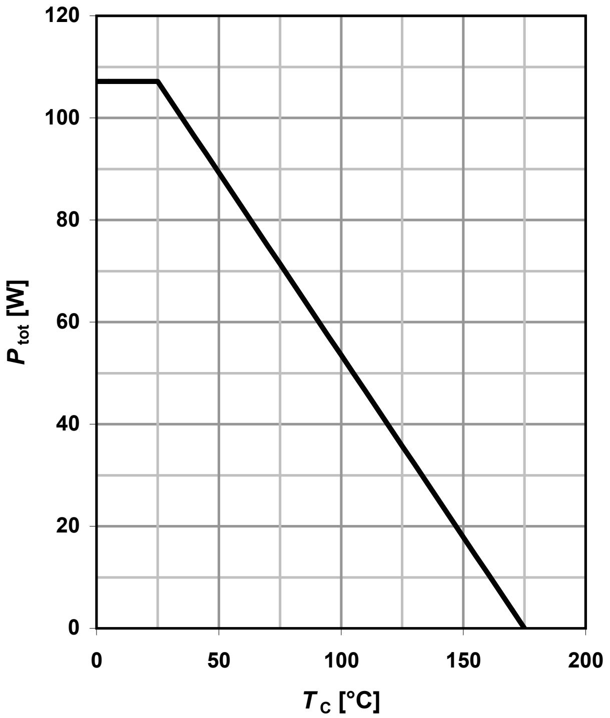
[1] Current is limited by bondwire; with an R_{thJC} = 1.4K/W the chip is able to carry A at 25°C.

[2] Specified by design. Not subject to production test.

[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

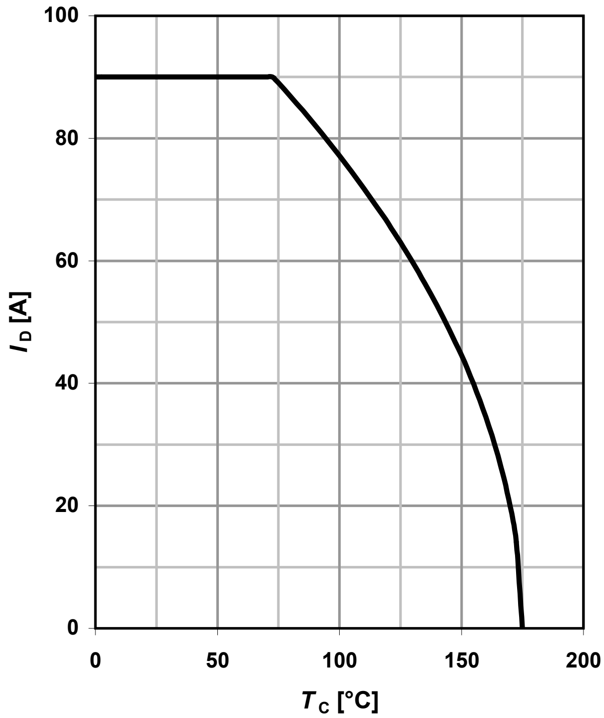
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



2 Drain current

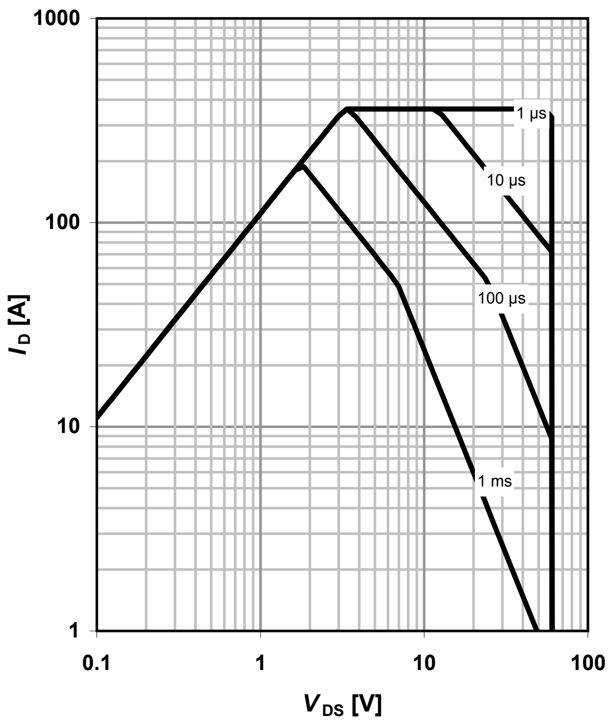
$I_D = f(T_C)$; $V_{GS} \geq 6$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

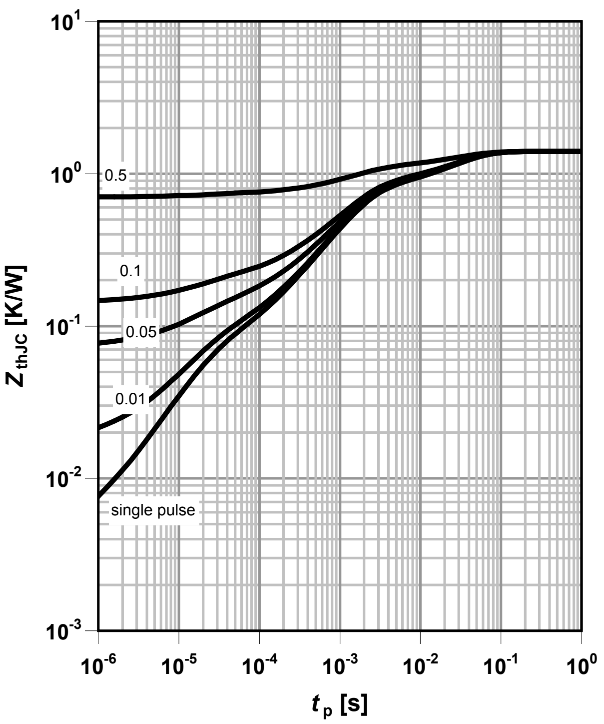
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

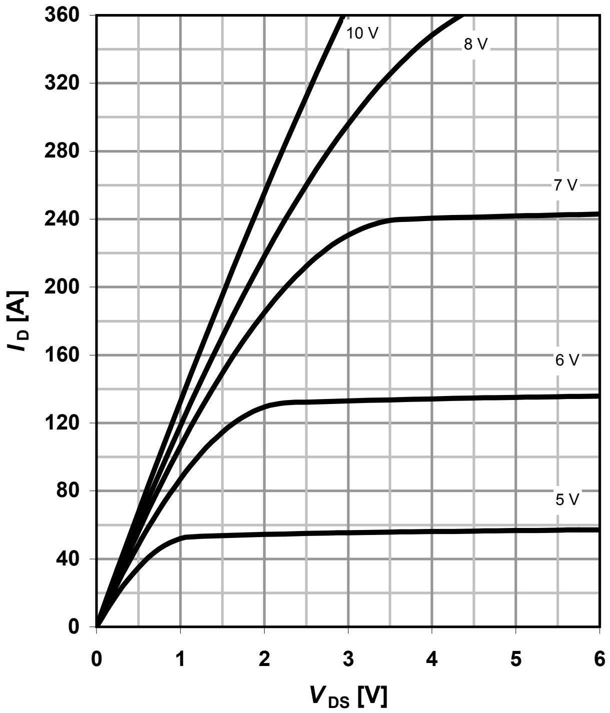
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25\ °C$

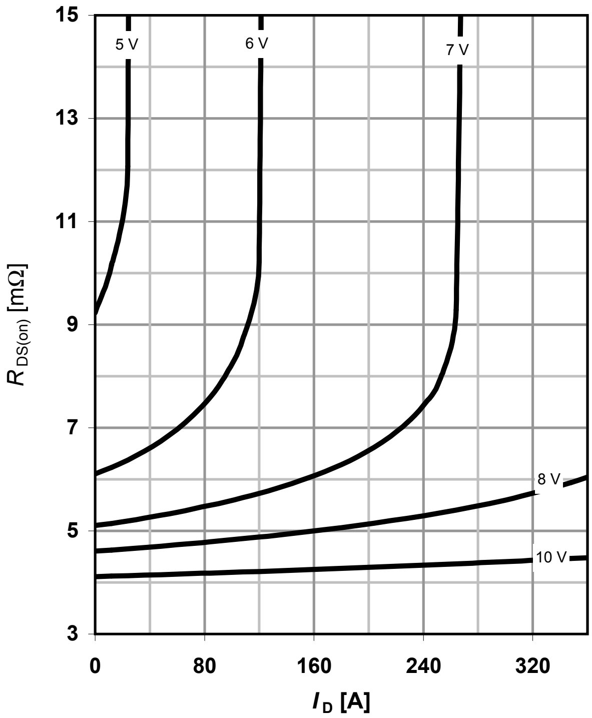
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25\ °C$

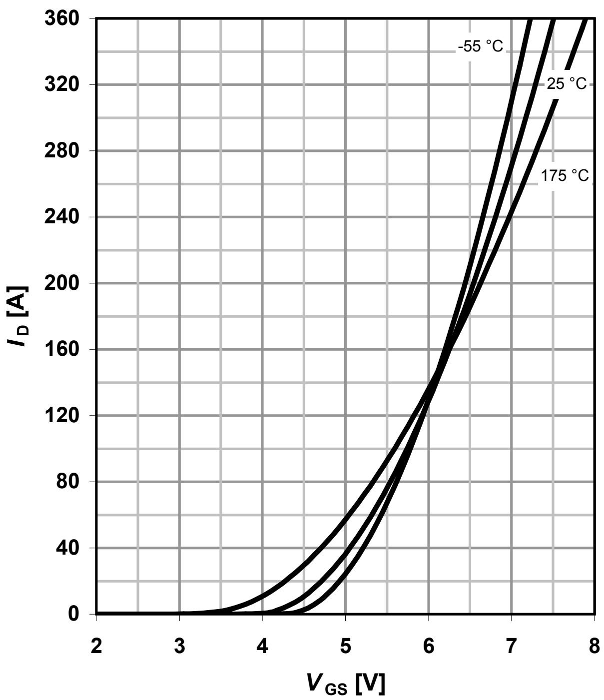
parameter: V_{GS}



7 Typ. transfer characteristics

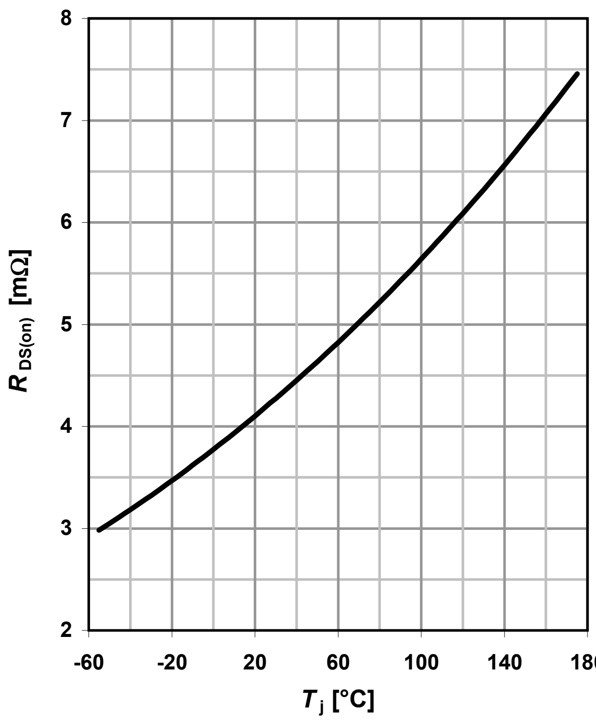
$I_D = f(V_{GS})$; $V_{DS} = 6V$

parameter: T_j



8 Typ. drain-source on-state resistance

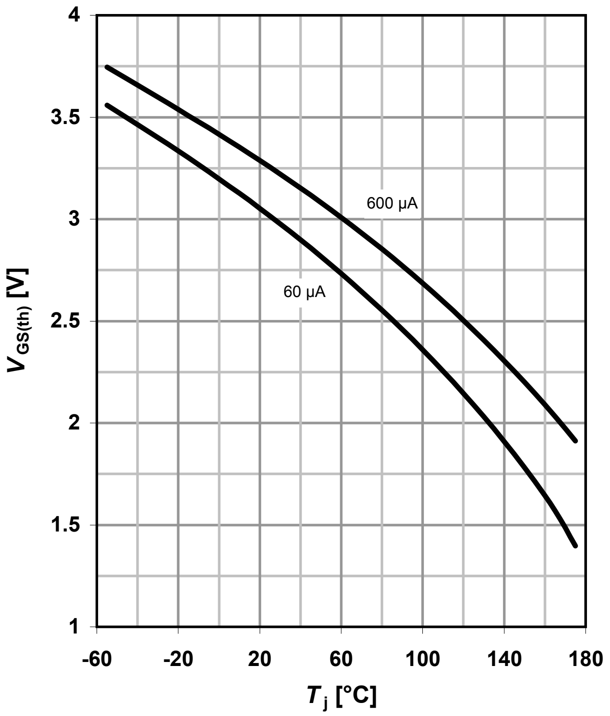
$R_{DS(on)} = f(T_j)$; $I_D = 90\ A$; $V_{GS} = 10\ V$



9 Typ. gate threshold voltage

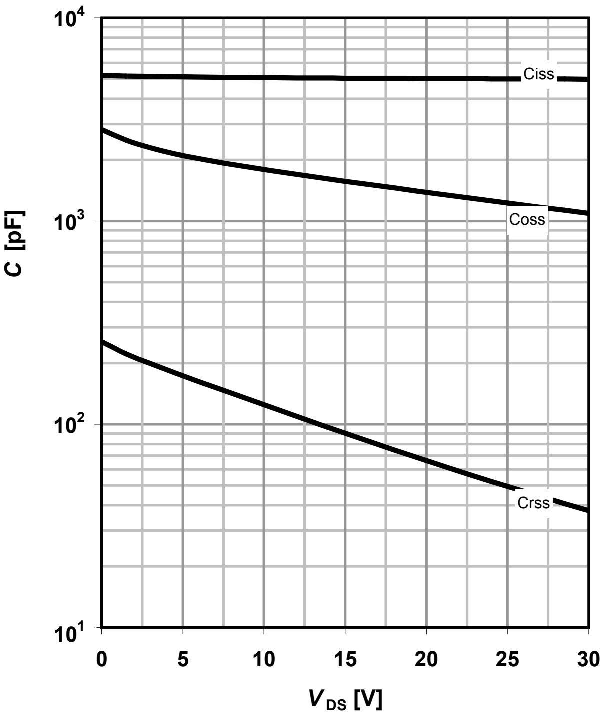
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

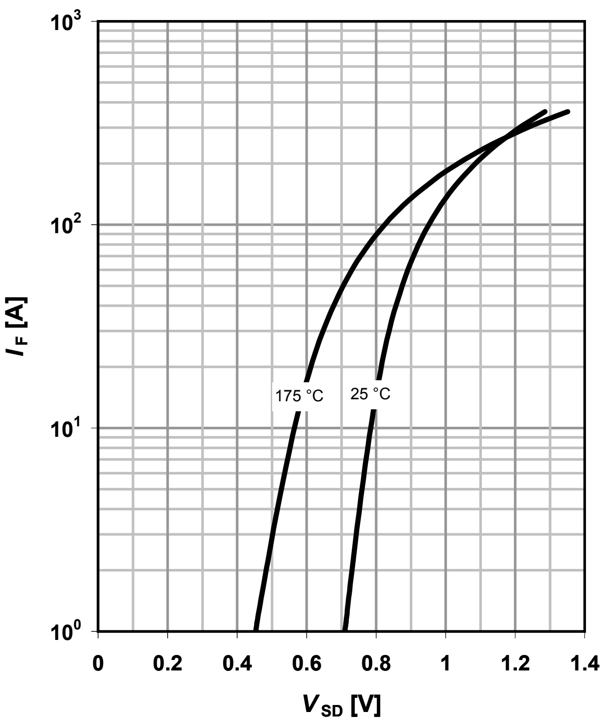
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

$IF = f(V_{SD})$

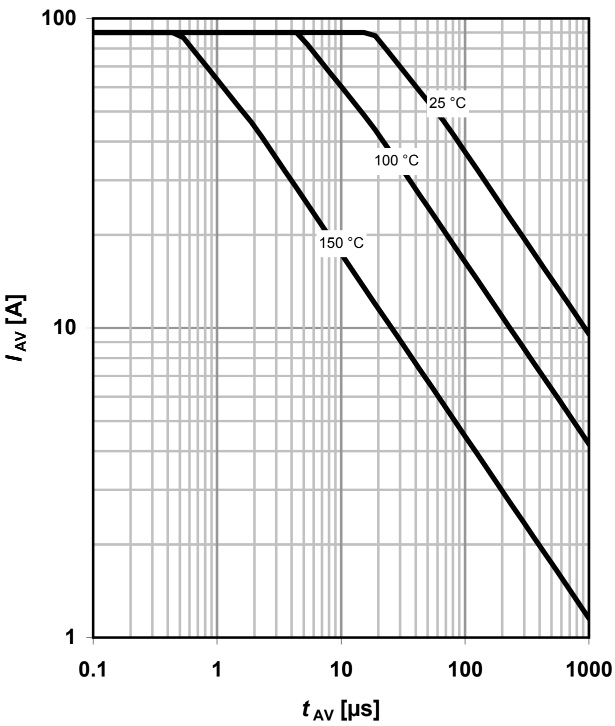
parameter: T_j



12 Avalanche characteristics

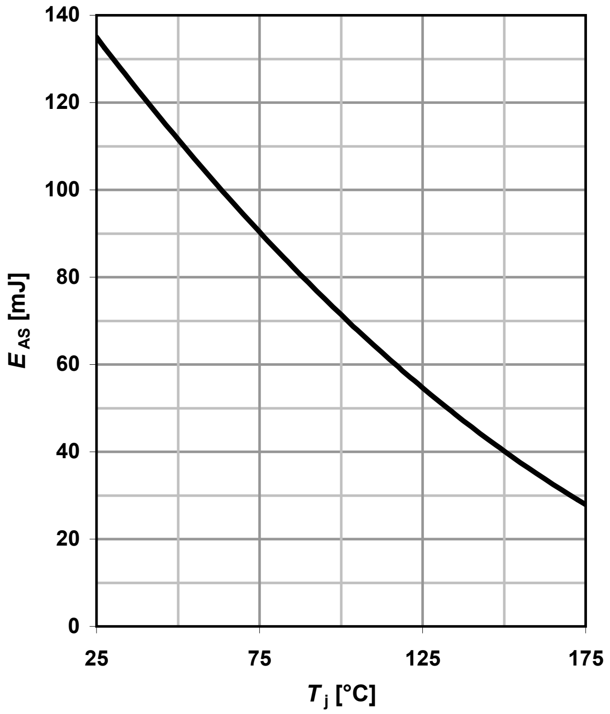
$I_{AS} = f(t_{AV})$

parameter: $T_{j(start)}$



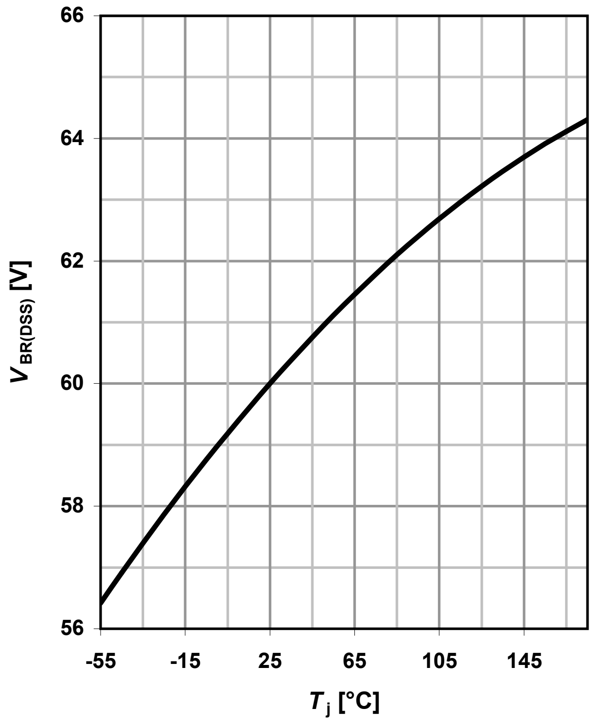
13 Avalanche energy

$E_{AS} = f(T_j)$; $I_D = 45$ A



14 Drain-source breakdown voltage

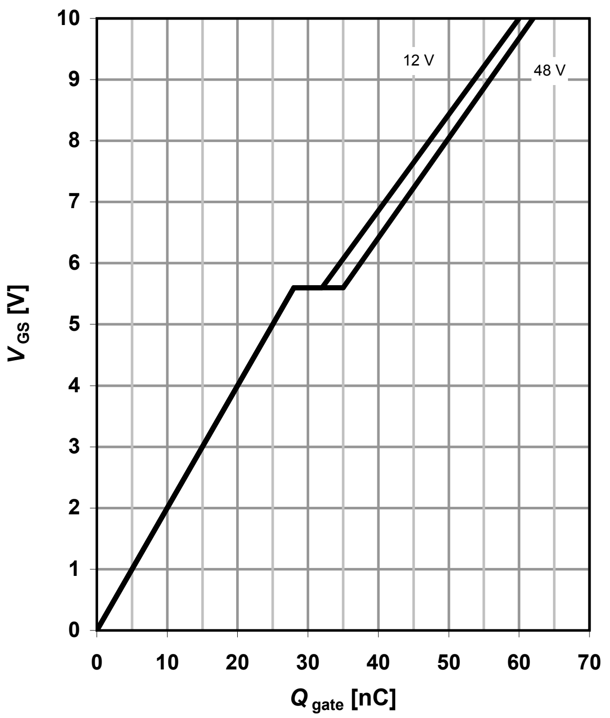
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



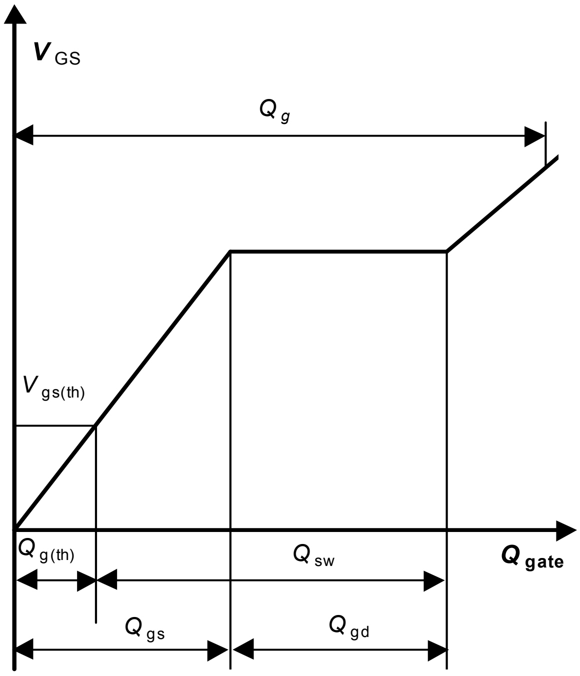
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 90$ A pulsed

parameter: V_{DD}



16 Gate charge waveforms



Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances.
For information on the types in question, please contact the nearest Infineon Technologies Office.
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life.
If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	24.03.2009	Final data sheet