

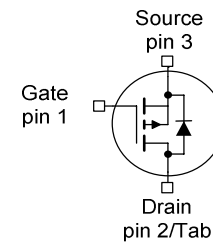
**OptiMOS<sup>®</sup>-P2 Power-Transistor**

**Features**

- P-channel - Normal Level - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- 100% Avalanche tested

**Product Summary**

$V_{DS}$	-40	V
$R_{DS(on)}$	8.9	mΩ
$I_D$	-73	A

**PG-TO252-3-313**


Type	Package	Marking
IPD70P04P4-09	PG-TO252-3-313	4P0409

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C=25\text{ °C}$ , $V_{GS}=-10\text{V}$	-73	A
		$T_C=100\text{ °C}$ , $V_{GS}=-10\text{V}^{1)}$	-52	
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	-292	
Avalanche energy, single pulse <sup>1)</sup>	$E_{AS}$	$I_D=-36\text{A}$	24	mJ
Avalanche current, single pulse	$I_{AS}$	-	-73	A
Gate source voltage	$V_{GS}$	-	±20	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	75	W
Operating and storage temperature	$T_j, T_{stg}$	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics<sup>1)</sup>**

Thermal resistance, junction - case	$R_{thJC}$	-	-	-	2	K/W
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	40	

**Electrical characteristics, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**

**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-1mA$	-40	-	-	V
Gate threshold voltage	$-V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-120\mu A$	2.0	3.0	4.0	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=-32V, V_{GS}=0V, T_j=25^\circ C$	-	-0.04	-1	$\mu A$
		$V_{DS}=-32V, V_{GS}=0V, T_j=125^\circ C^{2)}$	-	-20	-200	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=-20V, V_{DS}=0V$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-70A$	-	6.4	8.9	m $\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>1)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=-25V,$ $f=1MHz$	-	3700	4810	pF
Output capacitance	$C_{oss}$		-	1400	1820	
Reverse transfer capacitance	$C_{rss}$		-	40	80	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-20V,$ $V_{GS}=-10V, I_D=-73A,$ $R_G=3.5\Omega$	-	19	-	ns
Rise time	$t_r$		-	12	-	
Turn-off delay time	$t_{d(off)}$		-	24	-	
Fall time	$t_f$		-	31	-	

**Gate Charge Characteristics<sup>1)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=-32V, I_D=-70A,$ $V_{GS}=0 \text{ to } -10V$	-	20	26	nC
Gate to drain charge	$Q_{gd}$		-	10	20	
Gate charge total	$Q_g$		-	54	70	
Gate plateau voltage	$V_{plateau}$		-	-5.4	-	V

**Reverse Diode**

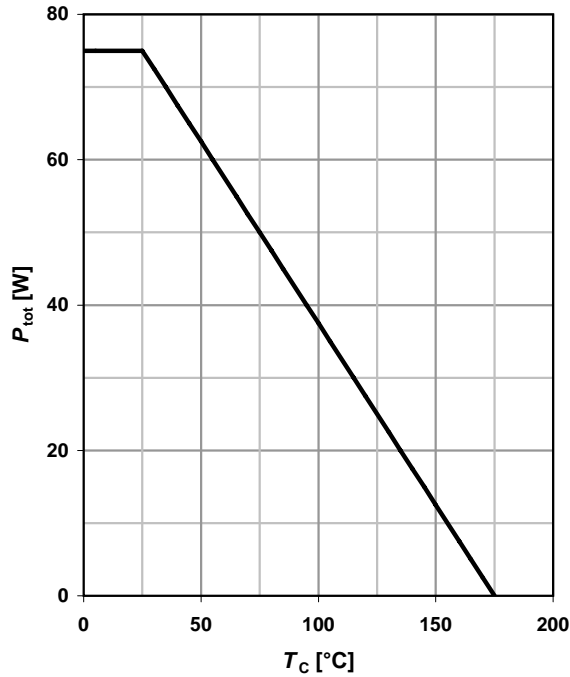
Diode continuous forward current <sup>1)</sup>	$I_S$	$T_C=25^\circ C$	-	-	-73	A
Diode pulse current <sup>1)</sup>	$I_{S,pulse}$		-	-	-292	
Diode forward voltage	$V_{SD}$	$V_{GS}=0V, I_F=-70A,$ $T_j=25^\circ C$	-	-1	-1.3	V
Reverse recovery time <sup>1)</sup>	$t_{rr}$	$V_R=-20V, I_F=-50A,$ $di_F/dt=-100A/\mu s$	-	50	-	ns
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$		-	50	-	nC

<sup>1)</sup> Defined by design. Not subject to production test.

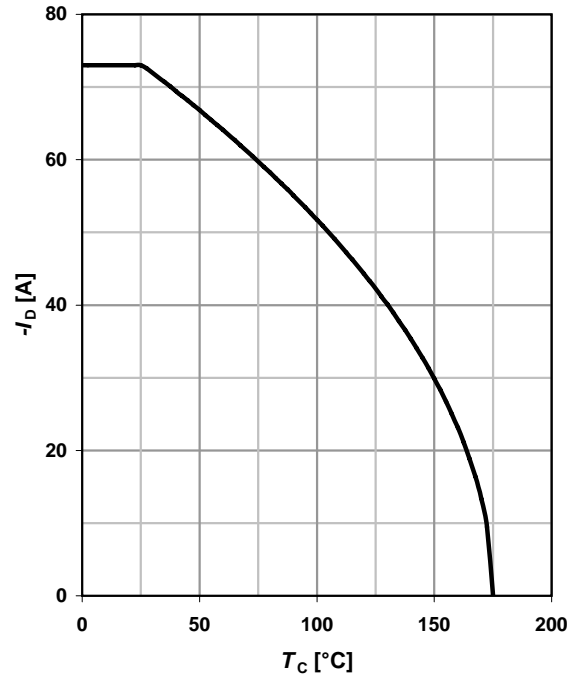
<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

**1 Power dissipation**

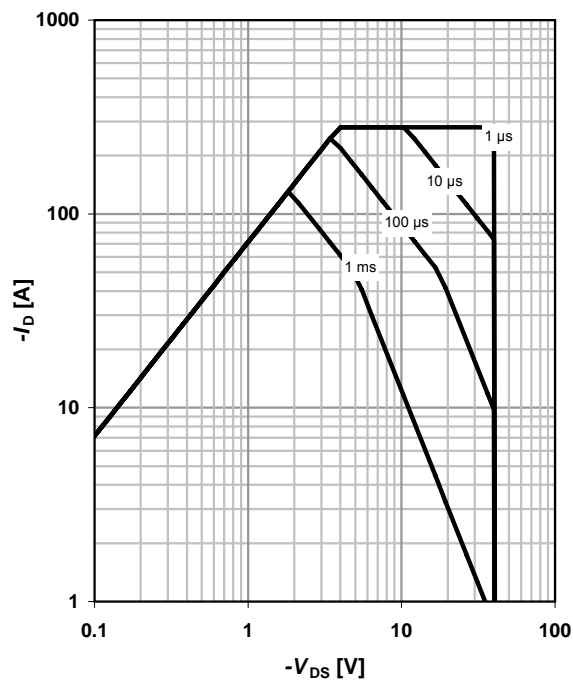
$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \leq -6\text{V}$$


**2 Drain current**

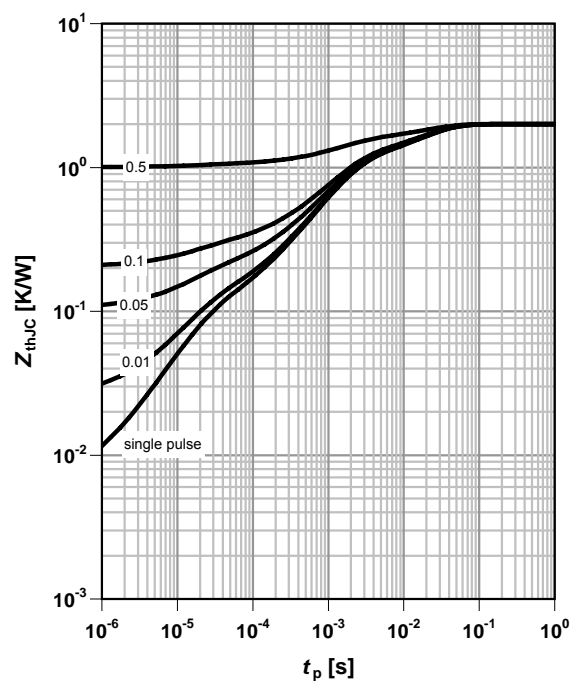
$$I_D = f(T_C); V_{\text{GS}} = -10\text{V}$$


**3 Safe operating area**

$$I_D = f(V_{\text{DS}}); T_C = 25\text{ °C}; D = 0, \text{ SMD}$$

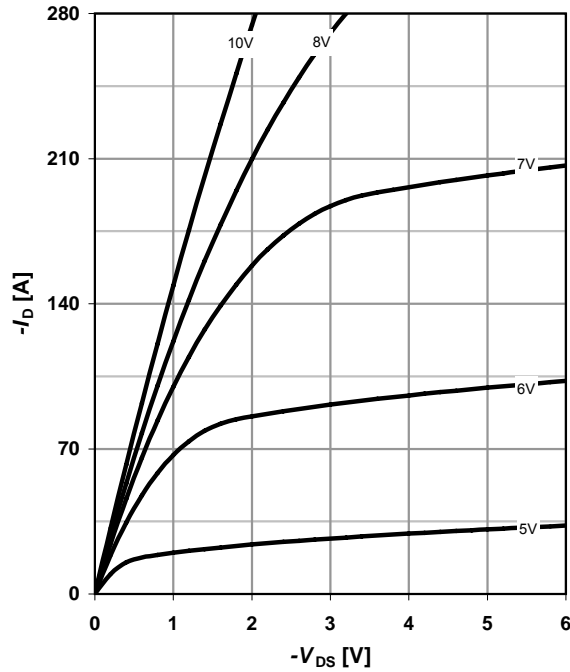
 parameter:  $t_p$ 

**4 Max. transient thermal impedance**

$$Z_{\text{thJC}} = f(t_p)$$

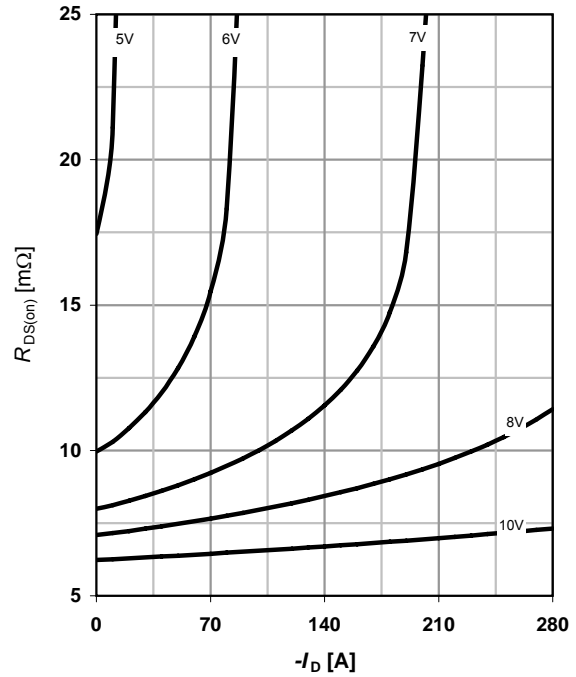
 parameter:  $D = t_p/T$ 


**5 Typ. output characteristics**

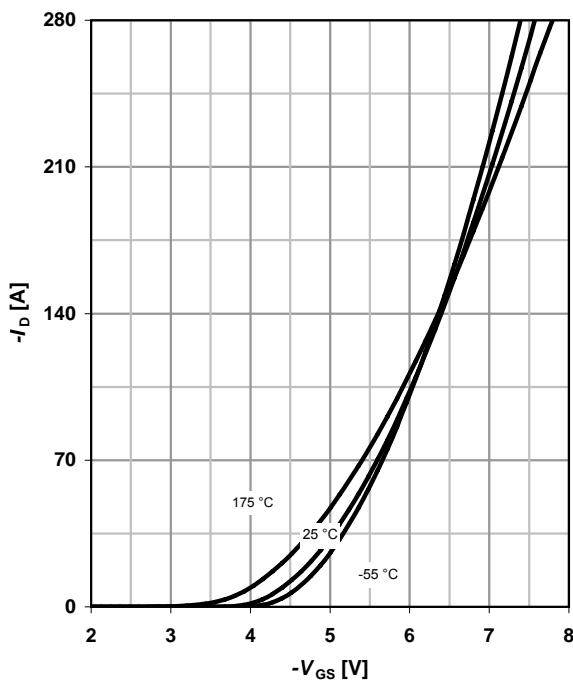
$$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$$

 parameter:  $-V_{GS}$ 

**6 Typ. drain-source on-state resistance**

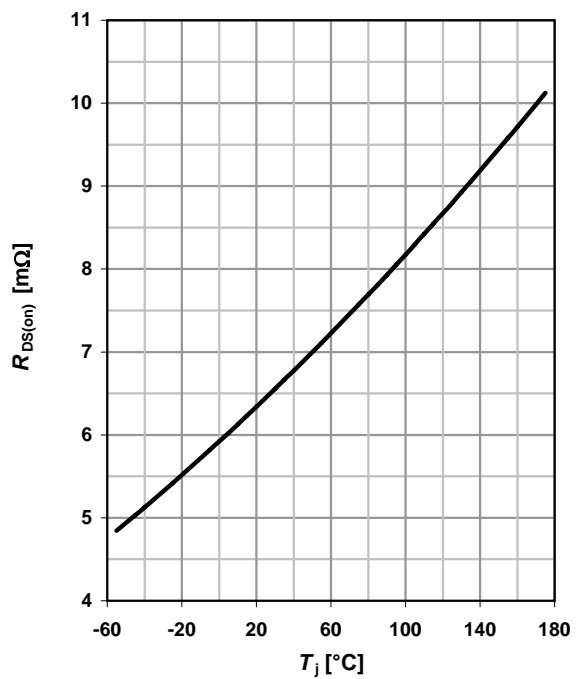
$$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$$

 parameter:  $V_{GS}$ 

**7 Typ. transfer characteristics**

$$I_D = f(V_{GS}); V_{DS} = -6\text{ V}$$

 parameter:  $T_j$ 

**8 Typ. drain-source on-state resistance**

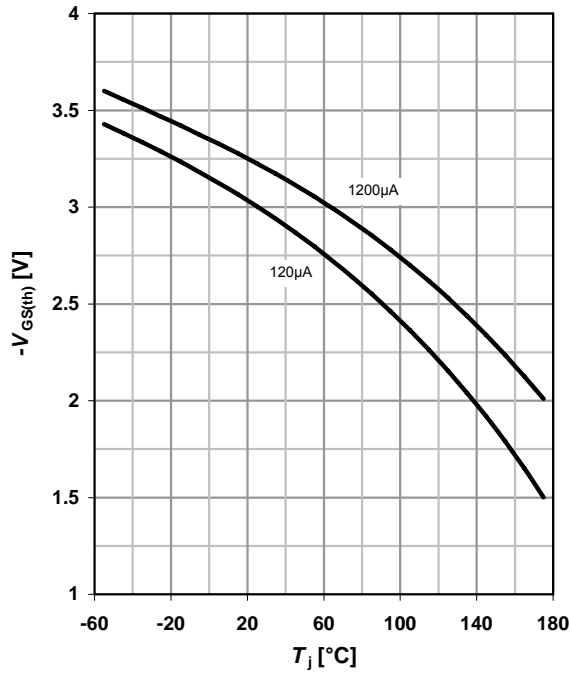
$$R_{DS(on)} = f(T_j); I_D = -70\text{ A}; V_{GS} = -10\text{ V}$$



**9 Typ. gate threshold voltage**

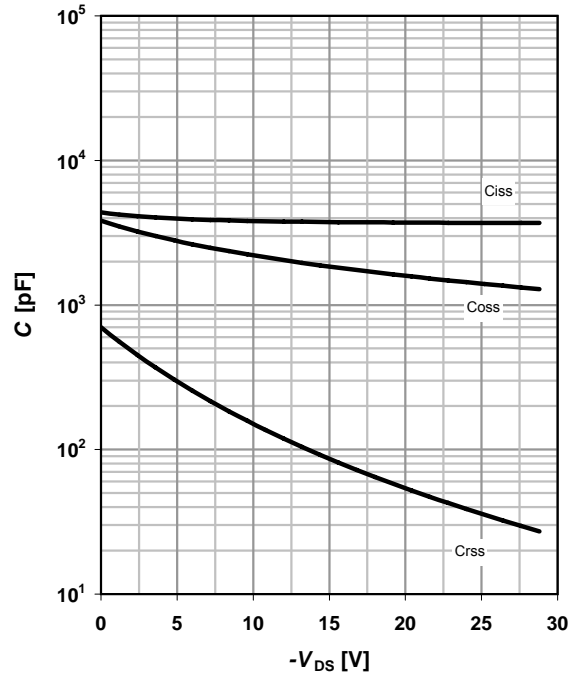
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter:  $-I_D$



**10 Typ. capacitances**

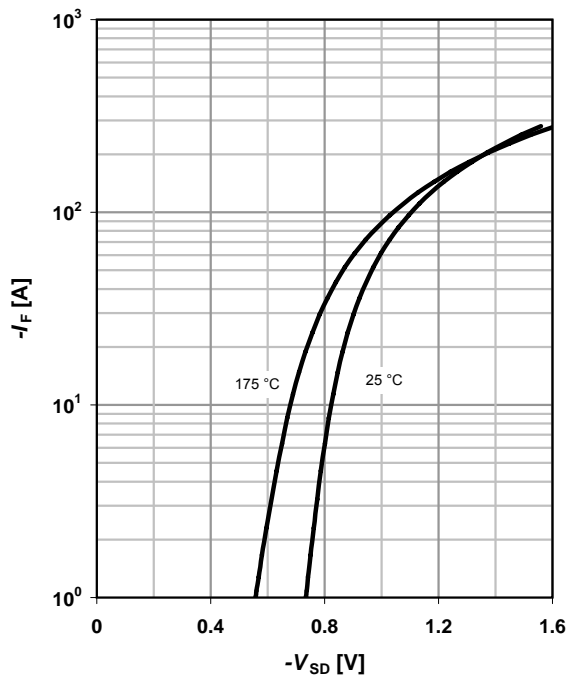
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



**11 Typical forward diode characteristics**

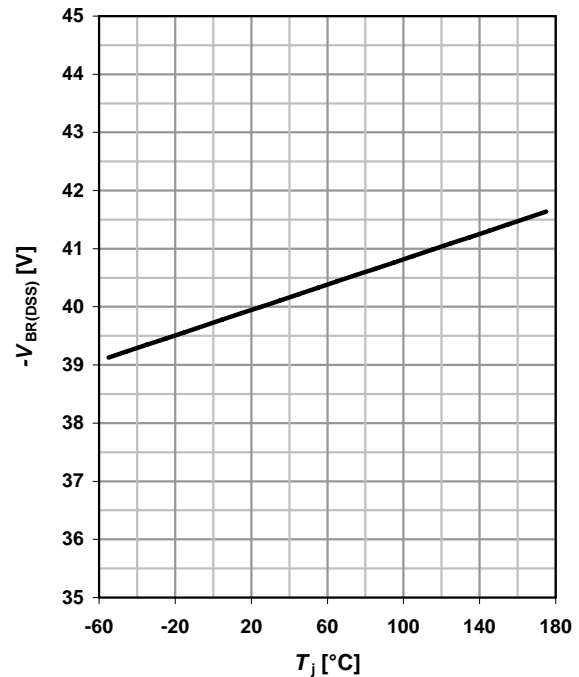
$$I_F = f(V_{SD})$$

parameter:  $T_j$



**12 Drain-source breakdown voltage**

$$V_{BR(DSS)} = f(T_j); I_D = -1 mA$$

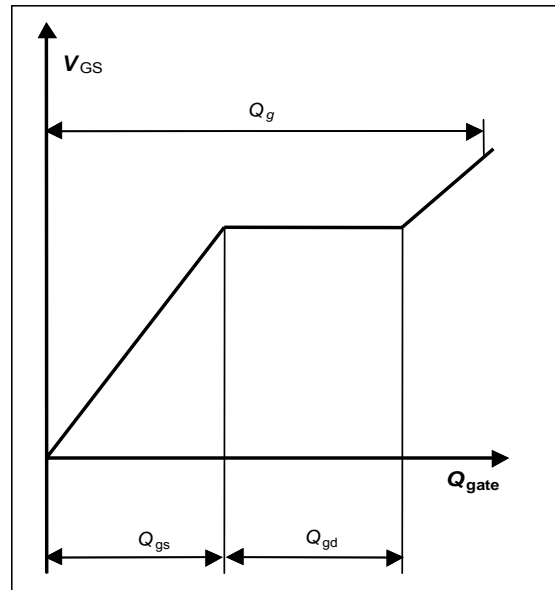
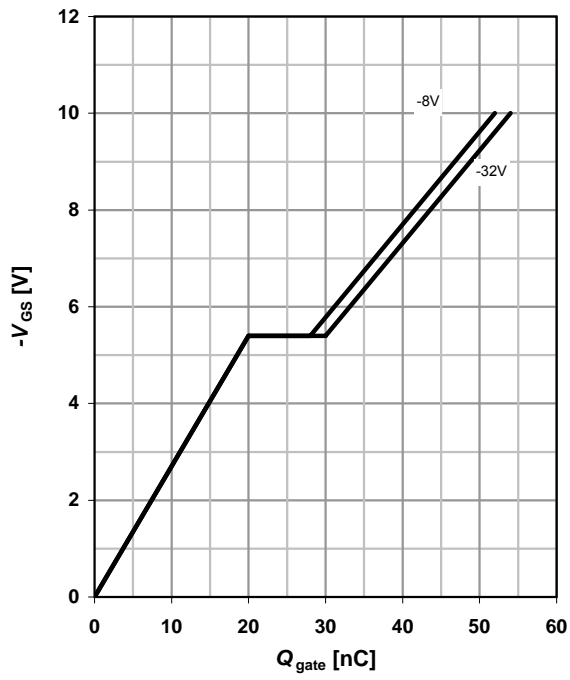


**13 Typ. gate charge**

$V_{GS} = f(Q_{gate}); I_D = -73 \text{ A pulsed}$

parameter:  $V_{DD}$

**14 Gate charge waveforms**



**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

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## Revision History

Version	Date	Changes
1.0	21.05.2010	Final Data Sheet